- **Commercial Operating Temperature Range 0°C to 70°C**
- **Military Operating Temperature Range –55°C to 125°C; QML Processing**
- **Highest Performance Floating-Point Digital Signal Processor (DSP)**
  - **Instruction Cycle Time of 40 ns**
    275 MOPS
    50 MFLOPS
    20 MIPS
    320 Mbytes/s
- **Six Communication Ports**
- **Six-Channel Direct Memory Access (DMA) Coprocessor**
- **Support for IEEE, 1/x, 1/$\sqrt{x}$**
- **Source-Code Compatible with TMP/SMJ320C30**
- **Validated Ada Compiler**
- **Single-Cycle 40-Bit Floating-Point, 32-Bit Integer Multipliers**
- **Twelve 40-Bit Registers, Eight Auxiliary Registers, 14 Control Registers, and Two Timers**
- **IEEE 1149.1† (JTAG) Boundary-Scan Compatible**
- **Two External Data and Address Buses Supporting Shared Memory Systems and High-Data Rate, Single-Cycle Transfers:**
  - **High Port-Data Rate of 80 Mbytes/s**
  - **4G-Word Continuous Program/Data/Peripheral Address Space**
  - **Memory-Access Request for Fast, Intelligent Bus Arbitration**
  - **Separate Address, Data, and Control-Enable Pins**
  - **Four Sets of Memory-Control Signals Support Different Speed Memories in Hardware**
- **Fabricated Using 0.8-μm Enhanced Performance Implanted CMOS (EPIC™) Technology by Texas Instruments (TI™)**
- **Separate Internal Program, Data, and DMA Coprocessor Buses for Support of Massive Concurrent Input/Output (I/O) of Program and Data Throughput, Maximizing Sustained CPU Performance**
- **On-Chip Program Cache and Dual-Access/Single-Cycle RAM for Increased Memory-Access Performance**
  - **128-Word Instruction Cache**
  - **2K-Words of Single-Cycle Dual Access Program or Data RAM**
  - **Boot Loader (ROM-Based) Supporting Program Bootup Via 8-, 16-, or 32-Bit Memories Over Any One of the Communication Ports**

description

The TMP/SMJ320C40KGD DSP is a 32-bit, floating-point processor manufactured in 0.8-μm, double-level metal CMOS technology. It is the fourth generation of DSPs from Texas Instruments, and it is the world's first DSP designed for parallel processing. The on-chip parallel processing capabilities of the 'C40 make the immense floating-point performance required by many applications achievable and cost-effective.

The TMP/SMJ320C40 is the first DSP with on-chip communication ports for processor-to-processor communication using simple communication software with no external hardware. This allows connectivity with no external glue logic. The communication ports remove input/output bottlenecks, and the independent smart-DMA coprocessor is able to handle the CPU input/output burden.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC and TI are trademarks of Texas Instruments Incorporated.
† IEEE Standard 1149.1–1990 Standard Test-Access Port and Boundary-Scan Architecture.

description (continued)

The features of the communication ports are:

- Six communication ports for direct interprocessor communication and processor I/O
- 20M-byte/s bidirectional interface on each communication port for high-speed and low-cost multiprocessor interface
- Separate input and output first-in, first-out (FIFO) buffers for processor-to-processor communication and I/O
- Automatic arbitration and handshaking for direct processor-to-processor connection

The DMA coprocessor allows concurrent I/O and CPU processing for the highest sustained CPU performance. The key features of the DMA coprocessor:

- Link pointers that allow DMA channels to auto-initialize
- Parallel CPU operation and DMA transfers
- Six DMA channels support communication-port-to-memory data transfers

The TMP/SMJ320C40KGD CPU is configured for high-speed internal parallelism for the highest sustained performance. The key features of the CPU are:

- Eight operations/cycle
  - 40-/32-bit floating-point/integer multiply
  - 40-/32-bit floating-point/integer arithmetic and logic unit (ALU) operation
  - Two data accesses
  - Two address-register updates
- IEEE floating-point conversion
- Division and square root support
- ’C30 assembly language compatibility
- Byte and halfword accessibility

A key factor in a parallel-processing implementation is the development tools available. The ’C40 is supported by a host of parallel-processing development tools for developing and simulating code easily and for debugging parallel-processing systems. The code generation tools include:

- Optimizing ANSI C compiler with a runtime library that supports use of communication ports and DMA
- SPOX by Spectron Microsystems Incorporated which provides parallel processing support as well as DMA and communication port drivers
- Assembler and linker with support for mapping program and data to parallel processors.

The simulation tools include:

- Parallel DSP system-level simulation by Logic Modeling Corporation (LMC) which includes a hardware verification (HV) model and full functional (FF) model
- TI software simulator with high-level language debugger interface for simulating a single processor

description (continued)

The hardware development and verification tools include:

- Parallel processor in-circuit emulator and high-level language debugger: XDS510
- Parallel processor development system with four TMS320C40s; local and global memory; and communication-port connections

known good die technology

Known good die (KGD) options are offered for use in multichip modules and chip-on-board (COB) applications. The current verification technology used to support KGD requirements for the TMP/SMJ320C40KGD is the removable tab (R-Tab).

The availability of selected DSP products in a tape-automated bond (TAB) configuration has made possible the use of a removable TAB technique. The TAB leadframe is attached to a gold-bumped die using nonoptimal bonding parameters. This technique allows easy removal of the tape after all needed 100% screens and parametric tests. The tape is removed from the tested part and the die is shipped in a conventional die container. The gold bumps remain on the bond pads which allow for subsequent attachment of gold-ball bonds.

electrical specifications

For military electrical and timing specifications please refer to the *SMJ320C40 Digital Signal Processor* data sheet, literature number SGUS017. For commercial electrical and timing specifications please refer to the *TMS320C4x User's Guide*, literature number SPRU063A.

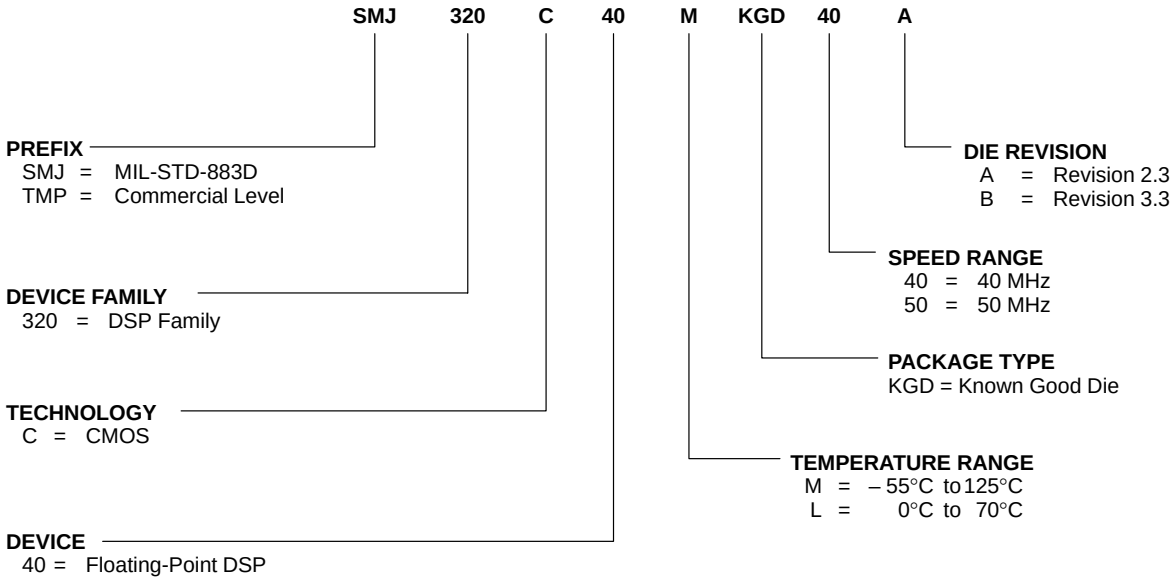

Figure 1. TMP/SMJ320C40KGD Device Nomenclature

JEDEC STANDARD

- Die thickness is approximately 15 mils.
- Backside surface finish is silicon.
- Maximum allowable die junction operating temperature is 175°C.
- Glassivation material is compressive nitride.
- Bond pad metal is composed of copper-doped aluminum.
- Percent defective allowed for burned-in die is 5.
- Life test data is available.
- Configuration control notification.
- Group A attribute summary is available (SMJ only).
- Suggested die-attach material is QMI 2569F.
- Suggested bond wire size is 1.0 to 1.25 mil.
- Suggested bonding method is gold-ball bonding.
- ESD rating is Class II.
- Maximum allowable peak process temperature for die-attach is 440°C.
- Saw curve is dependent on blade size used.
- Moisture-resistance data on die in plastic and TAB packages is available.

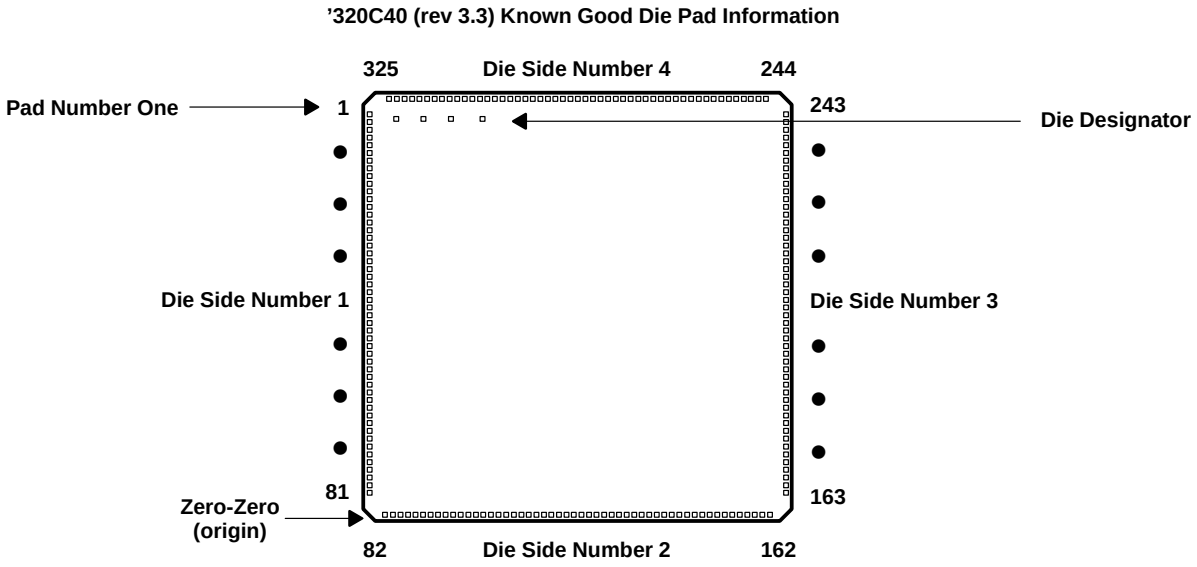

Figure 2. '320C40 Die Numbering Format (See Table 1)

Table 1 provides a reference for the following:

A. The 'C40 signal identities in relation to the pad numbers

B. The 'C40 X,Y coordinates, where bond pad 82 serves as the origin (0,0)

In addition, the following notes are significant:

C. X,Y coordinate data is in microns.

D. Coordinate origin is at (0,0) (center of bond pad 82).

E. The active silicon dimensions are 13805.40 μm × 13372.80 μm (543.52 mils × 526.49 mils).

F. The die size is approximately 13970.00 μm × 13538.2 μm (550.00 mils × 533.00 mils).

G. Bond pad dimensions are 120.00 μm × 120.00 μm (4.72 mils × 4.72 mils).

H. Gold bump dimensions are approximately 90 μm × 90 μm (3.54 mils × 3.54 mils).

I. Center of bond pad to edge of die ranges from 190 μm – 205 μm (7.5 mils – 8.1 mils). The range of 15 μm exists since the dicing process will result in some tolerance. Due to the consistency and precision of the bond pad locations in reference to each other, the center of bond pad 82 was chosen as the origin.

Table 1. ’320C40 Die Pad Information : rev 3.3 (0,8 μm)

DIE SIDE #1							
’C40 DIE BOND PAD LOCATIONS	DIE BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	’C40 DIE BOND PAD LOCATIONS	DIE BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD
1	D31		12631.60	42	$\overline{CV_{SS}}$		6776.80
2	D30		12491.60	43	LOCK		6636.80
3	D29		12351.60	44	V_{DDL}		6496.80
4	D28		12211.60	45	V_{SSL}		6356.80
5	D27		12071.60	46	$\overline{CE0}$		6183.00
6	D26		11931.60	47	$\overline{RDY0}$		5991.00
7	$GDDV_{DD}$		11791.60	48	$\overline{DE}$		5799.00
8	D25		11651.60	49	TCK		5607.00
9	D24		11511.60	50	TDO		5438.00
10	D23		11371.60	51	TDI		5264.20
11	D22		11231.60	52	$\overline{TMS}$		5072.20
12	D21		11091.60	53	$\overline{TRST}$		4880.20
13	D20		10951.60	54	EMU0		4711.20
14	D19		10811.60	55	EMU1		4571.20
15	D18		10671.60	56	DV_{SS}		4431.20
16	D17		10531.60	57	DV_{DD}		4291.20
17	D16		10391.60	58	PAGE1		4151.20
18	CV_{SS}		10251.60	59	$\overline{R/W1}$		4011.20
19	IV_{SS}		10111.60	60	$\overline{STRB1}$		3871.20
20	$GDDV_{DD}$		9971.60	61	STAT0		3731.20
21	DV_{SS}	– 477.20	9831.60	62	STAT1	– 477.20	3591.20
22	D15		9691.60	63	IV_{SS}		3451.20
23	D14		9551.60	64	STAT2		3311.20
24	D13		9411.60	65	STAT3		3171.20
25	D12		9271.60	66	PAGE0		3029.60
26	D11		9131.60	67	$\overline{R/W0}$		2889.60
27	D10		8991.60	68	$\overline{STRB0}$		2749.60
28	D9		8851.60	69	$\overline{AE}$		2575.80
29	D8		8711.60	70	RESETLOC1		2382.20
30	D7		8571.60	71	DV_{DD}		2213.20
31	D6		8431.60	72	RESETLOC0		2039.40
32	D5		8291.60	73	$\overline{RESET}$		1847.40
33	$GDDV_{DD}$		8151.60	74	$\overline{CRDY5}$		1678.40
34	D4		8011.60	75	$\overline{CSTRB5}$		1538.40
35	D3		7871.60	76	$\overline{CACK5}$		1398.40
36	D2		7731.60	77	$\overline{CREQ5}$		1258.40
37	D1		7591.60	78	$\overline{CRDY4}$		1118.40
38	$\overline{D0}$		7451.60	79	$\overline{CSTRB4}$		978.40
39	$\overline{CE1}$		7277.80	80	$\overline{CACK4}$		838.40
40	$\overline{RDY1}$		7085.80	81	$\overline{CREQ4}$		698.40
41	DV_{SS}		6916.80				

Table 1. ’320C40 Die Pad Information : rev 3.3 (0,8 μm) (Continued)

DIE SIDE #2							
’C40 DIE BOND PAD LOCATIONS	DIE BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	’C40 DIE BOND PAD LOCATIONS	DIE BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD
82	CV_{SS}	0.00		123	CV_{SS}	6780.00	
83	DV_{SS}	1180.00		124	DV_{SS}	6920.00	
84	DV_{DD}	1320.00		125	DV_{DD}	7060.00	
85	C5D7	1460.00		126	$\overline{CRDY3}$	7200.00	
86	C5D6	1600.00		127	$\overline{CSTRB3}$	7340.00	
87	C5D5	1740.00		128	$\overline{CACK3}$	7480.00	
88	C5D4	1880.00		129	CREQ3	7620.00	
89	C5D3	2020.00		130	V_{DDL}	7760.00	
90	C5D2	2160.00		131	V_{SSL}	7900.00	
91	C5D1	2300.00		132	$\overline{CRDY2}$	8040.00	
92	CD50	2440.00		133	$\overline{CSTRB2}$	8180.00	
93	DV_{DD}	2580.00		134	$\overline{CACK2}$	8320.00	
94	C4D7	2720.00		135	$\overline{CREQ2}$	8460.00	
95	C4D6	2860.00		136	DV_{DD}	8600.00	
96	C4D5	3000.00		137	$\overline{CRDY1}$	8740.00	
97	C4D4	3140.00		138	$\overline{CSTRB1}$	8880.00	
98	C4D3	3280.00		139	$\overline{CACK1}$	9020.00	
99	C4D2	3420.00		140	$\overline{CREQ1}$	9160.00	
100	C4D1	3560.00		141	$\overline{CRDY0}$	9300.00	
101	C4D0	3700.00		142	$\overline{CSTRB0}$	9440.00	
102	CV_{SS}	3840.00	0.00	143	$\overline{CACK0}$	9580.00	0.00
103	DV_{SS}	3980.00		144	$\overline{CREQ0}$	9720.00	
104	DV_{DD}	4120.00		145	CV_{SS}	9860.00	
105	C3D7	4260.00		146	DV_{SS}	10000.00	
106	C3D6	4400.00		147	IV_{SS}	10140.00	
107	C3D5	4540.00		148	DV_{DD}	10280.00	
108	C3D4	4680.00		149	C1D7	10420.00	
109	C3D3	4820.00		150	C1D6	10560.00	
110	C3D2	4960.00		151	C1D5	10700.00	
111	C3D1	5100.00		152	C1D4	10840.00	
112	C3D0	5240.00		153	C1D3	10980.00	
113	DV_{DD}	5380.00		154	C1D2	11120.00	
114	IV_{SS}	5520.00		155	C1D1	11260.00	
115	C2D7	5660.00		156	C1D0	11400.00	
116	C2D6	5800.00		157	DV_{DD}	11540.00	
117	C2D5	5940.00		158	C0D7	11680.00	
118	C2D4	6080.00		159	C0D6	11820.00	
119	C2D3	6220.00		160	C0D5	11960.00	
120	C2D2	6360.00		161	C0D4	12100.00	
121	C2D1	6500.00		162	C0D3	12240.00	
122	C2D0	6640.00					

Table 1. ’320C40 Die Pad Information : rev 3.3 (0,8 μm) (Continued)

DIE SIDE #3							
’C40 DIE BOND PAD LOCATIONS	DIE BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	’C40 DIE BOND PAD LOCATIONS	DIE BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD
163	C0D2		900.00	204	CV_{SS}		7216.00
164	C0D1		1040.00	205	DV_{DD}		7356.00
165	C0D0		1180.00	206	DV_{SS}		7496.00
166	CV_{SS}		1320.00	207	LA30		7637.60
167	DV_{DD}		1460.00	208	LA29		7777.60
168	ROMEN		1633.80	209	LA28		7917.60
169	$\overline{\text{IIOF0}}$		1803.20	210	LA27		8057.60
170	$\overline{DV_{SS}}$		1943.20	211	$LADV_{DD}$		8197.60
171	$\overline{\text{IIOF1}}$		2083.20	212	LA26		8337.60
172	$\overline{\text{IIOF2}}$		2223.20	213	LA25		8477.60
173	$\overline{\text{IIOF3}}$		2363.20	214	LA24		8617.60
174	$\overline{\text{NMI}}$		2537.00	215	LA23		8757.60
175	$\overline{\text{LSTRB0}}$		2706.00	216	LA22		8897.60
176	LR/$\overline{\text{W0}}$		2846.00	217	LA21		9037.60
177	LPAGE0		2986.00	218	LA20		9177.60
178	$\overline{\text{LRDY0}}$		3159.80	219	LA19		9317.60
179	$\overline{\text{LCE0}}$		3351.80	220	LA18		9457.60
180	$\overline{\text{LSTRB1}}$		3520.80	221	LA17		9597.60
181	LR/$\overline{\text{W1}}$		3660.80	222	LA16		9737.60
182	DV_{DD}		3800.80	223	$LADV_{DD}$		9877.60
183	CV_{SS}	13088.60	3940.80	224	CV_{SS}	13088.60	10017.60
184	LPAGE1		4080.80	225	DV_{SS}		10157.60
185	$\overline{\text{LRDY1}}$		4254.60	226	LA15		10297.60
186	$\overline{\text{LCE1}}$		4446.60	227	LA14		10437.60
187	$\overline{\text{LDE}}$		4638.60	228	LA13		10577.60
188	TCLK0		4807.60	229	LA12		10717.60
189	TCLK1		4947.60	230	LA11		10857.60
190	H3		5087.60	231	LA10		10997.60
191	$\overline{\text{H1}}$		5227.60	232	LA9		11137.60
192	$\overline{\text{LAE}}$		5401.40	233	LA8		11277.60
193	$\overline{IV_{SS}}$		5570.40	234	LA7		11417.60
194	$\overline{\text{LLOCK}}$		5710.40	235	LA6		11557.60
195	LSTAT0		5850.40	236	LA5		11697.60
196	LSTAT1		5990.40	237	LA4		11837.60
197	LSTAT2		6130.40	238	$LADV_{DD}$		11977.60
198	LSTAT3		6270.40	239	LA3		12117.60
199	$\overline{\text{IACK}}$		6412.00	240	LA2		12257.60
200	V_{DDL}		6552.00	241	LA1		12397.60
201	V_{SSL}		6692.00	242	LA0		12537.60
202	X1		6854.80	243	DV_{SS}		12766.40
203	X2/CLKIN		7029.20				

Table 1. ’320C40 Die Pad Information : rev 3.3 (0,8 μm) (Continued)

DIE SIDE #4							
’C40 DIE BOND PAD LOCATIONS	DIE BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	’C40 DIE BOND PAD LOCATIONS	DIE BOND PAD IDENTITY	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD
244	CV_{SS}	12170.80		285	CV_{SS}	6429.00	
245	LD31	12030.80		286	DV_{SS}	6289.00	
246	LD30	11890.80		287	A30	6149.00	
247	LD29	11750.80		288	A29	6009.00	
248	LD28	11610.80		289	A28	5869.00	
249	$LDDV_{DD}$	11470.80		290	$GADV_{DD}$	5729.00	
250	LD27	11330.80		291	A27	5589.00	
251	LD26	11190.80		292	A26	5449.00	
252	LD25	11050.80		293	A25	5309.00	
253	LD24	10910.80		294	A24	5169.00	
254	LD23	10770.80		295	A23	5029.00	
255	LD22	10630.80		296	A22	4889.00	
256	LD21	10490.80		297	A21	4749.00	
257	LD20	10350.80		298	A20	4609.00	
258	LD19	10210.80		299	A19	4469.00	
259	LD18	10070.80		300	A18	4329.00	
260	LD17	9930.80		301	A17	4189.00	
261	$LDDV_{DD}$	9790.80		302	$GADV_{DD}$	4049.00	
262	CV_{SS}	9650.80		303	CV_{SS}	3909.00	
263	DV_{SS}	9510.80		304	DV_{SS}	3769.00	
264	IV_{SS}	9370.80	13133.20	305	A16	3629.00	13133.20
265	LD16	9230.80		306	A15	3489.00	
266	LD15	9090.80		307	A14	3349.00	
267	LD14	8950.80		308	A13	3209.00	
268	LD13	8810.80		309	A12	3069.00	
269	LD12	8670.80		310	A11	2929.00	
270	LD11	8530.80		311	A10	2789.00	
271	LD10	8390.80		312	A9	2649.00	
272	LD9	8250.80		313	A8	2509.00	
273	LD8	8110.80		314	A7	2369.00	
274	LD7	7970.80		315	A6	2229.00	
275	LD6	7830.80		316	A5	2089.00	
276	LD5	7690.80		317	A4	1949.00	
277	$LDDV_{DD}$	7550.80		318	$GADV_{DD}$	1809.00	
278	LD4	7410.80		319	A3	1669.00	
279	LD3	7270.80		320	A2	1529.00	
280	LD2	7130.80		321	A1	1389.00	
281	LD1	6990.80		322	A0	1249.00	
282	LD0	6850.80		323	CV_{SS}	1109.00	
283	V_{DDL}	6709.00		324	DV_{SS}	489.00	
284	V_{SSL}	6569.00		325	SUBS	– 211.00	

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.