- **Based Upon the T320C2xLP Core CPU**
- **16-Bit Fixed-Point DSP Architecture**
  - **Six Internal Buses for Increased Parallelism and Performance**
  - **32-Bit ALU/Accumulator**
  - **16 × 16-Bit Single-Cycle Multiplier With a 32-Bit Product**
  - **Block Moves for Data, Program, I/O Space**
  - **Hardware Repeat Instruction**
- **Instruction Cycle Time**

’C203	’C209	’LC203
50 ns @ 5 V	50 ns @ 5 V	50 ns @ 3.3 V
35 ns @ 5 V	35 ns @ 5 V	
25 ns @ 5 V		

- **Source Code Compatible With TMS320C25**
- **Upwardly Code-Compatible With TMS320C5x Devices**
- **Four External Interrupts**
- **Boot-Loader Option (’C203 Only)**
- **TMS320C2xx Integrated Memory:**
  - **544 × 16 Words of On-Chip Dual-Access Data RAM**
  - **4K × 16 Words of On-Chip Single-Access Program/Data RAM (’C209 only)**
  - **4K × 16 Words of On-Chip Program ROM (’C209 Only)**
- **224K × 16-Bit Total Addressable External Memory Space**
  - **64K Program**
  - **64K Data**
  - **64K I/O**
  - **32K Global**
- **TMS320C2xx Peripherals:**
  - **PLL With Various Clock Options**
    - **×1, ×2, ×4, ÷2 (’C203)**
    - **×2, ÷2 (’C209)**
  - **On-Chip Oscillator**
  - **One Wait State Software-Programmable to Each Space (’C209 Only)**
  - **0 – 7 Wait States Software-Programmable to Each Space (’C203 Only)**
  - **Six General-Purpose I/O Pins**
  - **On-Chip 16-Bit Timer**
  - **Full-Duplex Asynchronous Serial Port (UART) (’C203 Only)**
  - **One Synchronous Serial Port With Four-Level-Deep FIFOs (’C203 Only)**
- **Supports Hardware Wait States**
- **Designed for Low-Power Consumption**
  - **Fully Static CMOS Technology**
  - **Power-Down IDLE Mode**
- **1.1 mA/MIPS at 3.3 V**
- **’C203 is Pin-Compatible With TMS320F206 Flash DSP**
- **Up to 40-MIPS Performance at 5 V (’C203)**
- **20-MIPS Performance at 3.3 V**
- **HOLD Mode for Multiprocessor Applications**
- **IEEE-1149.1† -Compatible Scan-Based Emulation**
- **Small Thin Quad Flat Packages (TQFPs)**

ADVANCE INFORMATION

description

The TMS320C2xx generation of digital signal processors (DSPs) combines strong performance and great flexibility to meet the needs of signal processing and control applications. The T320C2xLP core CPU that is the basis of all ’C2xx devices has been optimized for high speed, small size, and low-power, making it ideal for demanding applications in many markets. The CPU has an advanced, modified Harvard architecture with six internal buses that permits tremendous parallelism and data throughput. The powerful ’C2xx instruction set makes software development easy. And because the ’C2xx is code-compatible with the TMS320C2x and ’C5x generations, your code investment is preserved. Around this core, ’C2xx-generation devices feature various combinations of on-chip memory and peripherals. The serial ports provide easy communication with external devices such as codecs, A/D converters, and other processors. Other peripherals that facilitate the control of external devices include general-purpose I/O pins, a 16-bit timer, and a wait-state generator.

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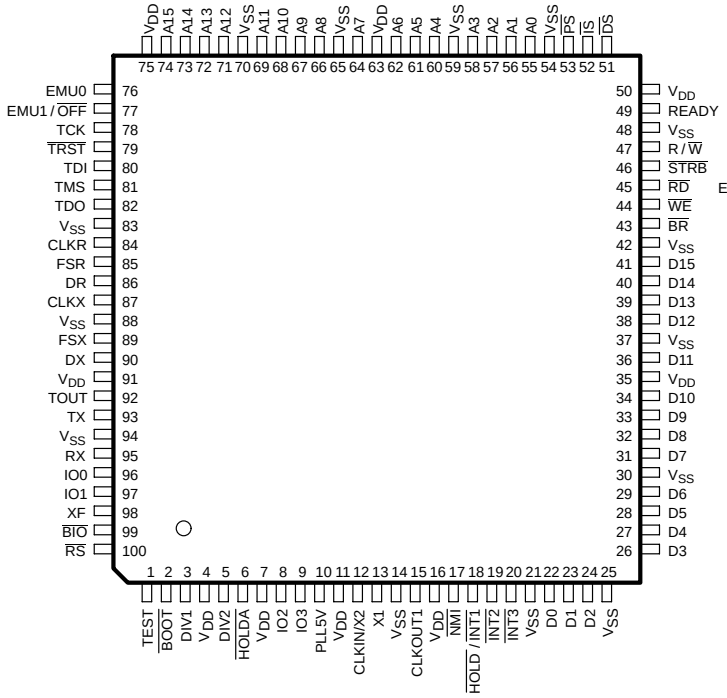
† IEEE Standard 1149.1-1990, IEEE Standard Test-Access Port.

ADVANCE INFORMATION

description (continued)

Because of their strong performance, low cost, and easy-to-use development environment, ’C2xx-generation DSPs are an ideal choice for applications such as smart phones, digital cameras, modems, remote metering, and security systems.

PZ PACKAGE
(TOP VIEW)



PN PACKAGE
(TOP VIEW)

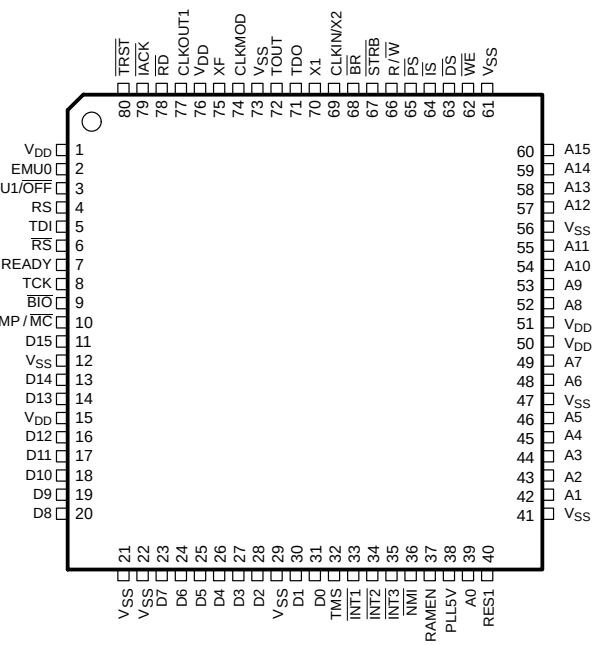


Table 2 provides a comparison of the devices in the ’C2xx generation. It shows the capacity of on-chip RAM and ROM, the number of serial and parallel I/O ports, the execution time of one machine cycle, and the type of package with total pin count.

Table 1. Low Power Dissipation†

POWER	TMS320C203	TMS320C209
3.3 V	1.1 mA/MIPS	N/A
5 V	1.9 mA/MIPS	1.9 mA/MIPS

† Core power dissipation. For complete details, see *Calculation of TMS320C2xx Power Dissipation* (literature number SPRA088).

Table 2. Characteristics of the TMS320C2xx Processors

TMS320C2xx DEVICES	ON-CHIP MEMORY			I/O PORTS		POWER SUPPLY (V)	CYCLE TIME (ns)	PACKAGE TYPE WITH PIN COUNT
	RAM		ROM					
	DATA	DATA/ PROG	PROG	SERIAL	PARALLEL			
TMS320C203	288	256	–	2	64K	5	50/35/25	100-pin TQFP
TMS320C209	288	4K + 256	4K	–	64K	5	50/35	80-pin TQFP
TM320LC203	288	256	–	2	64K	3.3	50	100-pin TQFP

TMS320C203 and TMS320LC203 Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE†	DESCRIPTION
DATA AND ADDRESS BUSES			
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	41 40 39 38 36 34 33 32 31 29 28 27 26 24 23 22	I/O/Z	Parallel data bus D15 [most significant bit (MSB)] through D0 [least significant bit (LSB)]. D15–D0 are multiplexed to transfer data between the TMS320C2xx and external data/program memory or I/O devices. Placed in the high-impedance state when not outputting (R/$\overline{W}$ high) or $\overline{RS}$ when asserted. They go into the high-impedance state when $\overline{OFF}$ is active low.
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	74 73 72 71 69 68 67 66 64 62 61 60 58 57 56 55	O/Z	Parallel address bus A15 (MSB) through A0 (LSB). A15–A0 are multiplexed to address external data/program memory or I/O devices. These signals go into the high-impedance state when $\overline{OFF}$ is active low.
MEMORY CONTROL SIGNALS			
$\overline{PS}$	53	O/Z	Program-select signal. $\overline{PS}$ is always high unless low-level asserted for communicating to off-chip program space. $\overline{PS}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{DS}$	51	O/Z	Data-select signal. $\overline{DS}$ is always high unless low-level asserted for communicating to off-chip program space. $\overline{DS}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{IS}$	52	O/Z	I/O space-select signal. $\overline{IS}$ is always high unless low-level asserted for communicating to I/O ports. $\overline{IS}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
READY	49	I	Data-ready input. READY indicates that an external device is prepared for the bus transaction to be completed. If the external device is not ready (READY low), the TMS320C203 waits one cycle and checks READY again. If READY is not used, it should be pulled high.
R/$\overline{W}$	47	O/Z	Read/write signal. R/$\overline{W}$ indicates transfer direction when communicating to an external device. R/$\overline{W}$ is normally in read mode (high), unless low level is asserted for performing a write operation. R/$\overline{W}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{RD}$	45	O/Z	Read-select indicates an active, external read cycle and can connect directly to the output enable ($\overline{OE}$) of external devices. $\overline{RD}$ is active on all external program, data, and I/O reads. $\overline{RD}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{WE}$	44	O/Z	Write enable. The falling edge of $\overline{WE}$ indicates that the device is driving the external data bus (D15–D0). Data can be latched by an external device on the rising edge of $\overline{WE}$. $\overline{WE}$ is active on all external program, data, and I/O writes. $\overline{WE}$ goes into the high-impedance state when $\overline{OFF}$ is active low.

† I = input, O = output, Z = high impedance, PWR = power, GND = ground

ADVANCE INFORMATION

TMS320C203 and TMS320LC203 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	TYPE†	DESCRIPTION
MEMORY CONTROL SIGNALS (CONTINUED)			
$\overline{\text{STRB}}$	46	O/Z	Strobe signal. $\overline{\text{STRB}}$ is always high unless asserted low to indicate an external bus cycle. $\overline{\text{STRB}}$ goes into the high-impedance state when $\overline{\text{OFF}}$ is active low.
MULTI-PROCESSING SIGNALS			
$\overline{\text{BR}}$	43	O/Z	Bus-request signal. $\overline{\text{BR}}$ is asserted when a global data-memory access is initiated. $\overline{\text{BR}}$ goes into the high-impedance state when $\overline{\text{OFF}}$ is active low.
$\overline{\text{HOLDA}}$	6	O/Z	Hold-acknowledge signal. $\overline{\text{HOLDA}}$ indicates to the external circuitry that the processor is in a hold state and that the address, data, and memory control lines are in the high-impedance state so that they are available to the external circuitry for access of local memory. $\overline{\text{HOLDA}}$ goes into the high-impedance state when $\overline{\text{OFF}}$ is active low.
XF	98	O/Z	External flag output (latched software-programmable signal). XF is used for signalling other processors in multiprocessing configurations or as a general-purpose output pin. XF goes into the high-impedance state when $\overline{\text{OFF}}$ is active low.
$\overline{\text{BIO}}$	99	I	Branch control input. When polled by the BIOZ instruction, if $\overline{\text{BIO}}$ is low, the TMS320C203 executes a branch. If $\overline{\text{BIO}}$ is not used, it should be pulled high.
IO0 IO1 IO2 IO3	96 97 8 9	I/O/Z	Software-controlled input/output pins by way of the asynchronous serial-port control register (ASPCR). At reset, IO0–IO3 are configured as inputs. These pins can be used as general-purpose input/output pins or as handshake control for the UART. IO0–IO3 go into the high-impedance state when $\overline{\text{OFF}}$ is active low.
INITIALIZATION, INTERRUPTS, AND RESET OPERATIONS			
$\overline{\text{RS}}$	100	I	Reset input. $\overline{\text{RS}}$ causes the TMS320C203 to terminate execution and forces the program counter to zero. When $\overline{\text{RS}}$ is brought high, execution begins at location 0 of program memory after 16 cycles. $\overline{\text{RS}}$ affects various registers and status bits.
TEST	1	I	Reserved input pin. TEST is connected to V_{SS} for normal operation.
$\overline{\text{BOOT}}$	2	I	Microprocessor-mode-select pin. When $\overline{\text{BOOT}}$ is high, the device accesses off-chip memory. If $\overline{\text{BOOT}}$ is low, the on-chip boot-loader transfers data from external global data space to external RAM program space.
$\overline{\text{NMI}}$	17	I	Nonmaskable interrupt. $\overline{\text{NMI}}$ is an external interrupt that cannot be masked by way of the interrupt-mode bit (INTM) or the interrupt-mask register (IMR). When $\overline{\text{NMI}}$ is activated, the processor traps to the appropriate vector location. If $\overline{\text{NMI}}$ is not used, it should be pulled high.
$\overline{\text{HOLD}}$/$\overline{\text{INT1}}$	18	I	$\overline{\text{HOLD}}$ and $\overline{\text{INT1}}$ share the same pin. Both are treated as interrupt signals. If the MODE bit is 0 in the ICR register, hold logic can be implemented in combination with the IDLE instruction in software. At reset, the MODE bit in ICR is zero, enabling the HOLD mode for the pin.
$\overline{\text{INT2}}$ $\overline{\text{INT3}}$	19 20	I	External user interrupts. $\overline{\text{INT2}}$ and $\overline{\text{INT3}}$ are prioritized and maskable by the IMR and the INTM. $\overline{\text{INT2}}$ and $\overline{\text{INT3}}$ can be polled and reset by way of the interrupt flag register (IFR). If these signals are not used, they should be pulled high.
OSCILLATOR, PLL, AND TIMER SIGNALS			
TOUT	92	O	Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT1-cycle wide. TOUT goes into the high-impedance state when $\overline{\text{OFF}}$ is active low.
CLKOUT1	15	O/Z	Master clock ouput signal. The CLKOUT1 high pulse signifies the logic phase while the low pulse signifies the latch phase.
CLKIN/X2 X1	12 13	I O	Input clock. CLKIN/X2 is the input clock to the device. As CLKIN, the pin operates as the external oscillator clock input and as X2, the pin operates as the internal oscillator input with X1 being the internal oscillator output.
DIV1 DIV2	3 5	I	DIV1 and DIV2 provide clock-mode inputs. DIV1–DIV2 should not be changed unless the $\overline{\text{RS}}$ signal is active.

† I = input, O = output, Z = high impedance, PWR = power, GND = ground

TMS320C203 and TMS320LC203 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	TYPE†	DESCRIPTION
OSCILLATOR, PLL, AND TIMER SIGNALS (CONTINUED)			
PLL5V	10	I	PLL operating at 5 V. When the device is operating at 5 V, PLL5V should be tied high. When the device is operating at 3.3 V, PLL5V should be tied low.
SERIAL PORT AND UART SIGNALS			
CLKX	87	I/O	Transmit clock. CLKX is a clock signal for clocking data from the DX (data-receive register) to the DX data-transmit pin. The CLKX can be an input if the MCM bit in the synchronous serial-port control register (SSPCR) is set to 0. CLKX can also be driven by the device at one-half of the CLKOUT1 frequency when MCM = 1. If the serial port is not being used, CLKX goes into the high-impedance state when OFF is active low. Value at reset is as an input.
CLKR	84	I	Receive-clock input. External clock signal for clocking data from the DR (data-receive) pin into the serial-port shift register (RSR). CLKR must be present during serial-port transfers. If the serial port is not being used, CLKR can be sampled as an input by IN0 bit of the SSPCR.
FSR	85	I	Frame synchronization pulse for receive input. The falling edge of the FSR pulse initiates the data-receive process, beginning the clocking of the RSR. FSR goes into the high-impedance state when $\overline{\text{OFF}}$ is active low.
FSX	89	I/O	Frame synchronization pulse for transmit input/ouput. The falling edge of the FSR pulse initiates the data-transmit process, beginning the clocking of the RSR. Following reset, FSX is an input. FSX can be selected by software to be an output when the TXM bit in the serial control register, SSPCR, is set to 1. FSX goes into the high-impedance state when $\overline{\text{OFF}}$ is active low.
DR	86	I	Serial-data receive input. Serial data is received in the receive shift register (RSR) through the DR pin.
DX	90	O	Serial-port transmit output. Serial data is transmitted from the transmit shift register (XSR) through the DX pin. DX is in the high-impedance state when $\overline{\text{OFF}}$ is active low.
TX	93	O	Asynchronous transmit pin
RX	95	I	Asynchronous receive pin
TEST SIGNALS			
$\overline{\text{TRST}}$	79	I	IEEE Standard 1149.1 (JTAG) test reset. $\overline{\text{TRST}}$, when active high, gives the scan system control of the operations of the device. If $\overline{\text{TRST}}$ is not connected or driven low, the device operates in its functional mode, and the test signals are ignored.
TCK	78	I	JTAG test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on the test-access port (TAP) input signals (TMS and TDI) are clocked into the TAP controller, instruction register, or selected test-data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TMS	81	I	JTAG test-mode select. TMS is clocked into the TAP controller on the rising edge of TCK.
TDI	80	I	JTAG test-data input. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	82	O/Z	JTAG test-data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when the scanning of data is in progress.
EMU0	76	I/O/Z	Emulator pin 0. When $\overline{\text{TRST}}$ is driven low, EMU0 must be high for activation of the $\overline{\text{OFF}}$ condition. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as an input/output through the JTAG scan.
EMU1/$\overline{\text{OFF}}$	77	I/O/Z	Emulator pin 1. Emulator pin 1 disables all outputs. When $\overline{\text{TRST}}$ is driven high, EMU1/$\overline{\text{OFF}}$ is used as an interrupt to or from the emulator system and is defined as an input/output through the JTAG scan. When $\overline{\text{TRST}}$ is driven low, this pin is configured as $\overline{\text{OFF}}$. EMU1/$\overline{\text{OFF}}$, when active low, puts all output drivers in the high-impedance state. Note that $\overline{\text{OFF}}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications). Therefore, for the $\overline{\text{OFF}}$ condition, the following apply: $\overline{\text{TRST}}$ = 0 EMU0 = 1 EMU/$\overline{\text{OFF}}$ = 0

† I = input, O = output, Z = high impedance, PWR = power, GND = ground

ADVANCE INFORMATION

TMS320C203 and TMS320LC203 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	TYPE†	DESCRIPTION
SUPPLY PINS			
V_{DD}	4 7 11 16 35 50 63 75 91	PWR	Power
V_{SS}	14 21 25 30 37 42 48 54 59 65 70 83 88 94	GND	Ground

† I = input, O = output, Z = high impedance, PWR = power, GND = ground

ADVANCE INFORMATION

TMS320C209 Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE†	DESCRIPTION
ADDRESS AND DATA BUSES			
D15	11	I/O/Z	Parallel data bus D15 (MSB) through D0 (LSB). D15–D0 are multiplexed to transfer data between the core CPU and external data/program memory or I/O devices. D15–D0 are placed in the high-impedance state when not outputting or when $\overline{RS}$ is asserted. They also go into the high-impedance state when $\overline{OFF}$ is active low.
D14	13		
D13	14		
D12	16		
D11	17		
D10	18		
D9	19		
D8	20		
D7	23		
D6	24		
D5	25		
D4	26		
D3	27		
D2	28		
D1	30		
D0	31		
A15	60	O/Z	Parallel address bus A15 (MSB) through A0 (LSB). A15–A0 are multiplexed to address external data/program memory or I/O devices. These signals go into the high-impedance state when $\overline{OFF}$ is active low.
A14	59		
A13	58		
A12	57		
A11	55		
A10	54		
A9	53		
A8	52		
A7	49		
A6	48		
A5	46		
A4	45		
A3	44		
A2	43		
A1	42		
A0	39		
MEMORY CONTROL SIGNALS			
$\overline{PS}$	65	O/Z	Program-select signal. $\overline{PS}$ is always high unless low-level asserted for communicating to off-chip program space. $\overline{PS}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{DS}$	63	O/Z	Data-select signal. $\overline{DS}$ is always high unless low-level asserted for communicating to off-chip program space. $\overline{DS}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{IS}$‡	64	O/Z	I/O-space-select signal. $\overline{IS}$ is always high unless low-level asserted for communicating to I/O ports. $\overline{IS}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
READY	7	I	Data-ready input. READY indicates that an external device is prepared for the bus transaction to be completed. If READY is low, the TMS320C209 waits one cycle and checks READY again. If READY is not used, it should be pulled high.
R/$\overline{W}$‡	66	O/Z	Read/write signal. R/$\overline{W}$ indicates transfer direction when communicating to an external device. R/$\overline{W}$ is normally in read mode (high), unless low level is asserted for performing a write operation. R/$\overline{W}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{STRB}$	67	O/Z	Strobe signal. $\overline{STRB}$ is always high unless asserted low to indicate an external bus cycle. $\overline{STRB}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{RD}$	78	O/Z	Read-select. $\overline{RD}$ indicates an active, external read cycle and can connect directly to the output enable ($\overline{OE}$) of external devices. $\overline{RD}$ is active on all external program, data, and I/O reads. $\overline{RD}$ goes into the high-impedance state when $\overline{OFF}$ is active low.

† I = input, O = output, Z = high impedance, PWR = power, GND = ground
‡ $\overline{IS}$, R/$\overline{W}$, and the data bus are visible at the pins, while accessing internal I/O-mapped registers (for ’C209 devices only).

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ADVANCE INFORMATION

TMS320C209 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	TYPE†	DESCRIPTION
MEMORY CONTROL SIGNALS (CONTINUED)			
$\overline{WE}$	62	O/Z	Write enable. The falling edge of $\overline{WE}$ indicates that the device is driving the external data bus (D15–D0). Data can be latched by an external device on the rising edge of $\overline{WE}$. $\overline{WE}$ is active on all external program, data, and I/O writes. $\overline{WE}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
RAMEN	37	I	RAM enable. RAMEN enables the 4K × 16 words of on-chip RAM.
MULTIPROCESSING SIGNALS			
$\overline{BR}$	68	O/Z	Bus-request signal. $\overline{BR}$ is asserted during access of external global data-memory space. $\overline{BR}$ can be used to extend the data memory address space by up to 32K words. $\overline{BR}$ goes into the high-impedance state when $\overline{OFF}$ is active low.
$\overline{BIO}$	9	I	Branch control input. $\overline{BIO}$ is polled by BIOZ instruction. If $\overline{BIO}$ is low, the TMS320C209 executes a branch. If $\overline{BIO}$ is not used, it should be pulled high.
XF	75	O/Z	External flag output (latched software-programmable signal). XF is used for signaling other processors in multiprocessing configurations or as a general-purpose output pin.
$\overline{IACK}$	79	O/Z	Interrupt-acknowledge signal. $\overline{IACK}$ indicates receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15–A0. $\overline{IACK}$ also goes into the high-impedance state when $\overline{OFF}$ is active low.
INITIALIZATION, INTERRUPT, AND RESET OPERATIONS			
$\overline{INT1}$ $\overline{INT2}$ $\overline{INT3}$	33 34 35	I	External-user interrupts. $\overline{INT1}$–$\overline{INT3}$ are prioritized and maskable by the interrupt-mask register and the interrupt-mode bit. If $\overline{INT1}$–$\overline{INT3}$ are not used, they should be pulled high.
$\overline{NMI}$	36	I	Nonmaskable interrupt. $\overline{NMI}$ is an external interrupt that cannot be masked through the INTM or the IMR. When $\overline{NMI}$ is activated, the processor traps to the appropriate vector location. If $\overline{NMI}$ is not used, it should be pulled high.
RS $\overline{RS}$	4 6	I	Reset input. $\overline{RS}$ and RS cause the TMS320C209 to terminate execution and force the program counter to 0. When $\overline{RS}$ is brought high, execution begins at location 0 of program memory after 16 cycles. $\overline{RS}$ affects various registers and status bits.
MP/$\overline{MC}$	10	I	Microprocessor/microcontroller-mode-select pin. If MP/$\overline{MC}$ is low, the on-chip ROM is mapped into program space. When MP/$\overline{MC}$ is high, the device accesses off-chip memory.
OSCILLATOR/TIMER SIGNALS CLKIN1/2			
CLKOUT1	77	O/Z	Master clock output signal. CLKOUT1 cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the rising edges of CLKOUT1. CLKOUT1 goes into the high-impedance state when $\overline{OFF}$ is active low.
CLKMOD	74	I	Clock-input mode. CLKMOD (when high) enables the clock doubler and phase-locked loop (PLL) on the clock input signal. If the internal oscillator is not used, X1 should be left unconnected.
CLKIN/X2 X1	69 70	I O	Input clock. CLKIN/X2 is the input clock to the device. As CLKIN, the pin operates as the external oscillator clock input and as X2, the pin operates as the internal oscillator input with X1 being the internal oscillator output.
TOUT	72	O	Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT1-cycle wide.
PLL5V	38	I	PLL operating at 5 V. When PLL5V is operating at 5 V, PLL5V should be strapped high.
RES1	40	I	Reserved input pin. **Do not connect to RES1.**

† I = input, O = output, Z = high impedance, PWR = power, GND = ground

TMS320C209 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	TYPE†	DESCRIPTION
TEST SIGNALS			
TCK	8	I	JTAG test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on test-access port (TAP) input signals (TMS and TDI) are clocked into the TAP controller, instruction register, or selected test-data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	5	I	JTAG test data input. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	71	O/Z	JTAG test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when scanning of data is in progress. TDO goes into the high-impedance state when $\overline{\text{OFF}}$ is active low.
TMS	32	I	JTAG test mode-select. TMS is clocked into the TAP controller on the rising edge of TCK.
$\overline{\text{TRST}}$	80	I	JTAG test reset. $\overline{\text{TRST}}$, when active high, gives the JTAG scan system control of the operations of the device. If $\overline{\text{TRST}}$ is not connected or driven low, the device operates in its functional mode, and the JTAG signals are ignored.
EMU0 EMU1/$\overline{\text{OFF}}$	2 3	I/O/Z	Emulator pin 0. When $\overline{\text{TRST}}$ is driven low, EMU0 must be high for activation of the $\overline{\text{OFF}}$ condition. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as an input/output through the JTAG scan. Emulator pin 1. EMU1 disables all outputs. When $\overline{\text{TRST}}$ is driven high, EMU1/$\overline{\text{OFF}}$ is used as an interrupt to or from the emulator system and is defined as input/output by way of JTAG scan. When $\overline{\text{TRST}}$ is driven low, this pin is configured as $\overline{\text{OFF}}$. EMU1/$\overline{\text{OFF}}$, when active low, puts all output drivers in the high-impedance state.
SUPPLY PINS			
V_{DD}	1 15 50 51 76	PWR	Power
V_{SS}	12 21 22 29 41 47 56 61 73	GND	Ground

† I = input, O = output, Z = high impedance, PWR = power, GND = ground

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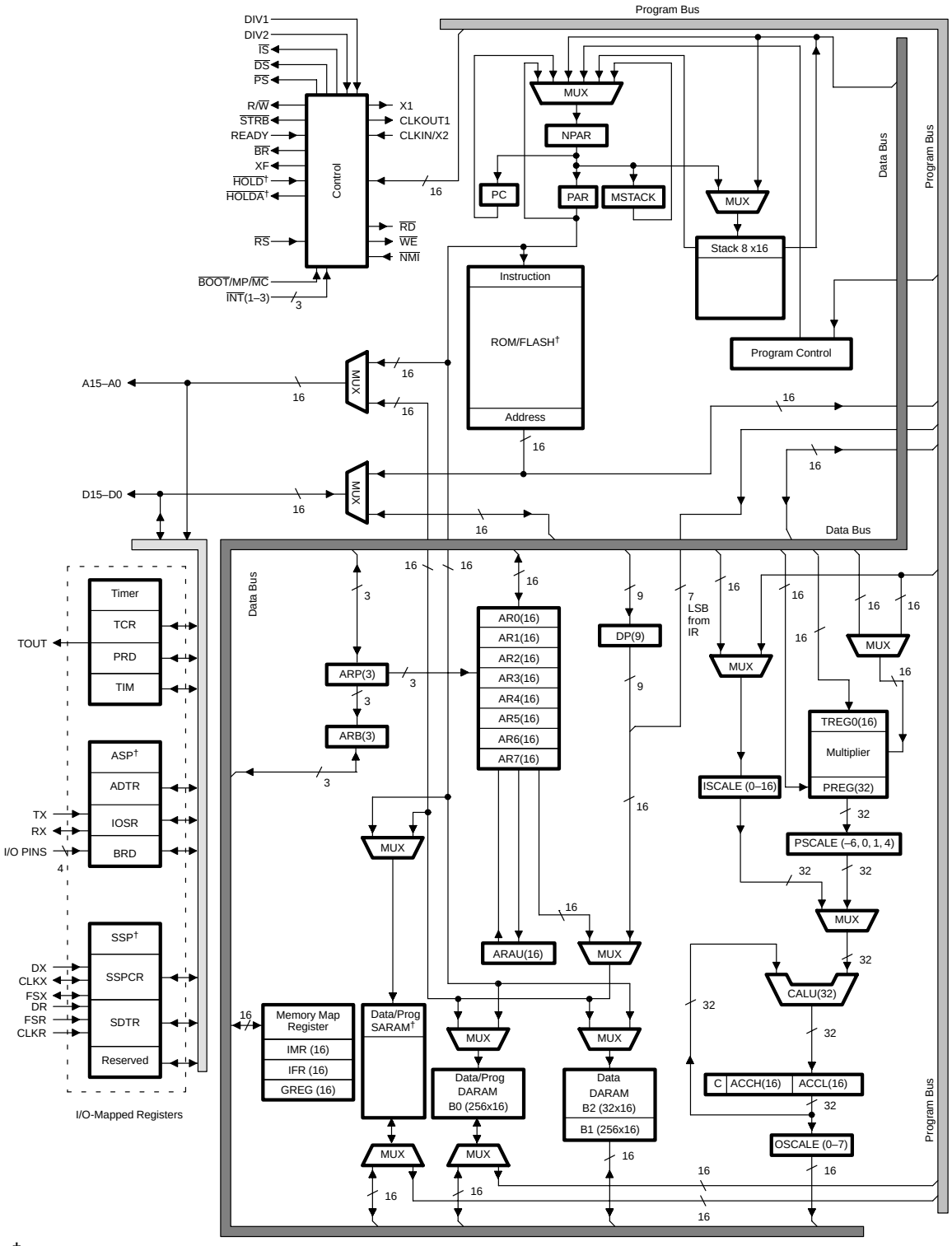
functional block diagram of the ’C2xx internal hardware



† Not available on all devices (see Table 2).
NOTE A: Symbol descriptions appear in Table 3.

Table 3. Legend for the ’C2xx Internal Hardware Functional Block Diagram

SYMBOL	NAME	DESCRIPTION
ACC	Accumulator	32-bit register that stores the results and provides input for subsequent CALU operations. Also includes shift and rotate capabilities
ARAU	Auxiliary Register Arithmetic Unit	An unsigned, 16-bit arithmetic unit used to calculate indirect addresses using the auxiliary registers as inputs and outputs
AUX REGS	Auxiliary Registers 0–7	These 16-bit registers are used as pointers to anywhere within the data space address range. They are operated upon by the ARAU and are selected by the auxiliary register pointer (ARP). AR0 can also be used as an index value for AR updates of more than one and as a compare value to AR.
$\overline{\text{BR}}$	Bus Register Signal	$\overline{\text{BR}}$ is asserted during access of the external global data memory space. READY is asserted to the device when the global data memory is available for the bus transaction. $\overline{\text{BR}}$ can be used to extend the data memory address space by up to 32K words.
C	Carry	Register carry output from CALU. C is fed back into the CALU for extended arithmetic operation. The C bit resides in status register 1 (ST1), and can be tested in conditional instructions. C is also used in accumulator shifts and rotates.
CALU	Central Arithmetic Logic Unit	32-bit-wide main arithmetic logic unit for the TMS320C2xx core. The CALU executes 32-bit operations in a single machine cycle. CALU operates on data coming from ISCALE or PSCALE with data from ACC, and provides status results to PCTRL.
CNF	On-Chip RAM Configuration Control Bit	If set to 0, the reconfigurable data dual-access RAM (DARAM) blocks are mapped to data space; otherwise, they are mapped to program space.
DRAB	Data-Read Address Bus	16-bit bus that provides the address for data-read operations. DRAB is driven by the TMS320C2xx core.
DRDB	Data-Read Bus	16-bit bus for data-space read data. DRDB is driven by memories or by the logic interface.
DWAB	Data-Write Bus	16-bit bus that provides the address for data-write operations. DWAB is driven by the TMS320C2xx core.
DWEB	Data-Write Bus	16-bit bus for data-space write data. DWEB is driven by the TMS320C2xx core.
GREG	Global Memory Allocation Register	GREG specifies the size of the global data memory space.
IMR	Interrupt Mask Register	IMR individually masks or enables the seven interrupts.
IFR	Interrupt Flag Register	The 7-bit IFR indicates that the TMS320C2xx has latched an interrupt from one of the seven maskable interrupts.
INTM	Interrupt-Mode Bit	When INTM is set to 0, all unmasked interrupts are enabled. When INTM is set to 1, all maskable interrupts are disabled.
INT#	Interrupt Traps	A total of 32 interrupts by way of hardware and/or software are available.
ISCALE	Input Data-Scaling Shifter	16 to 32-bit barrel left-shifter. ISCALE (ISFL) shifts incoming 16-bit data 0 to16 positions left, relative to the 32-bit output within the fetch cycle; therefore, no cycle overhead is required for input scaling operations.
MPY	Multiplier	16 × 16-bit multiplier to a 32-bit product. MPY executes multiplication in a single cycle. MPY operates either signed or unsigned 2s-complement arithmetic multiply.
MSTACK	Micro Stack	MSTACK provides temporary storage for the address of the next instruction to be fetched when program address-generation logic is used to generate sequential addresses in data space.
MUX	Multiplexer	Multiplexes buses to a common input
NPAR	Next Program Address	NPAR holds the program address to be driven out on the PAB on the next cycle.
OSCALE	Output Data-Scaling Shifter	32-bit to 16-bit barrel left shifter. OSCALE (OSFL) shifts the 32-bit accumulator output 0 to 7 bits left for quantization management and outputs either the 16-bit high- or low-half of the shifted 32-bit data to DWEB.
PAB	Program Address Bus	16-bit bus that provides the address for program-space reads and writes. PAB is driven by the TMS320C2xx core.
PAR	Program Address	PAR holds the address currently being driven on PAB for as many cycles as it takes to complete all memory operations scheduled for the current machine cycle.

Table 3. Legend for the ’C2xx Internal Hardware Functional Block Diagram (Continued)

SYMBOL	NAME	DESCRIPTION
PC	Program Counter	PC increments the value from NPAR to provide sequential addresses for instruction-fetching and sequential data-transfer operations
PCTRL	Program Controller	PCTRL decodes instruction, manages the pipeline, stores status, and decodes conditional operations.
PM	Product Shift-Mode Register Bits	These two bits identify which of the four product-shift modes (–6, 0, 1, 4) will be used by PSCALE. PM resides in ST1. See Table 5.
PRDB	Program-Read Data Bus	16-bit bus for program space read data. PRDB is driven by the memories or the logic interface.
PREG	Product Register	32-bit register holds results of 16 × 16 multiply.
PSCALE	Product-Scaling Shifter	0-, 1- or 4-bit left shift or 6-bit right shift of multiplier product. The left-shift options are used to manage the additional sign bits resulting from the 2s-complement multiply. The right-shift option is used to scale down the number to manage overflow of product accumulation in the CALU. PSCALE (PSFL) resides in the path from the 32-bit product shifter and from either the CALU or the DWEB, and requires no cycle overhead.
TREG	Temporary Register	16-bit register holds one of the operands for the multiply operations. TREG holds the dynamic shift count for the LACT, ADDT, and SUBT instructions. TREG holds the dynamic bit position for the BITT instruction.
SSPCR	Synchronous Serial-Port Control Register	SSPCR is the control register for selecting the serial port’s mode of operation.
SDTR	Synchronous Serial-Port Transmit and Receive Register	SDTR is the data-transmit and data-receive register
TCR	Timer-Control Register	TCR contains the control bits that define the divide-down ratio, start/stop the timer, and reloads the period. Also contained in TCR is the current count in the prescaler. Reset initializes the timer-divide-down ratio to 0 and starts the timer.
PRD	Timer-Period Register	PRD contains the 16-bit period that is loaded into the timer counter when the counter borrows or when the reload bit is activated. Reset initializes the PRD to 0xFFFF.
TIM	Timer-Counter Register	TIM contains the current 16-bit count of the timer. Reset initializes the TIM to 0xFFFF.
UART	Universal Asynchronous Receive/Transmit	UART is the asynchronous serial port
ASPCR	Asynchronous Serial-Port Control Register	ASPCR controls the asynchronous serial-port operation.
ADTR	Asynchronous data register	Asynchronous data-transmit and data-receive register
IOSR	I/O Status Register	IOSR detects current levels (and changes with inputs) on pins IO0–IO3 and the status of UART.
BRD	Baud-Rate Divisor	Used to set the baud rate of the UART
ST0 ST1	Status Register	ST0 and ST1 contain the status of various conditions and modes. These registers can be stored in and loaded from data memory, thereby allowing the status of the machine to be saved and restored.
IMR	Interrupt Mask Registers	IMR individually masks or enables the seven interrupts.
IFR	Interrupt Flag Register	IFR indicates that the T320C2xLP core has latched an interrupt pulse from one of the maskable interrupts.
STACK	Stack	STACK is a block of memory used for storing return addresses for subroutines and interrupt-service routines, or for storing data. The ’C2xx stack is 16-bit wide and eight-level deep.

architectural overview

The ’C2xx advanced Harvard-type architecture maximizes the processing power by maintaining two separate memory bus structures—program and data—for full-speed execution. This multiple bus structure allows both data and instructions to be read simultaneously. Instructions to be read support data transfers between the two spaces. This architecture permits coefficients that are stored in program memory to be read in RAM, thereby, eliminating the need for a separate coefficient ROM. This, coupled with a four-deep pipeline, allows the TMS320C2xx to execute most instructions in a single cycle.

status and control registers

Two status registers, ST0 and ST1, contain the status of various conditions and modes. These registers can be stored in data memory and loaded from data memory, thereby, allowing the status of the machine to be saved and restored for subroutines.

The load-status-register instruction (LST) is used to write to ST0 and ST1. The store-status-register instruction (SST) is used to read from ST0 and ST1, except for the INTM bit, which is not affected by the LST instruction. The individual bits of these registers can be set or cleared when using the SETC and CLRC instructions. Figure 1 shows the organization of status registers ST0 and ST1, indicating all status bits contained in each. Several bits in the status registers are reserved and read as logic 1s. Refer to Table 4 for the status register field definitions.

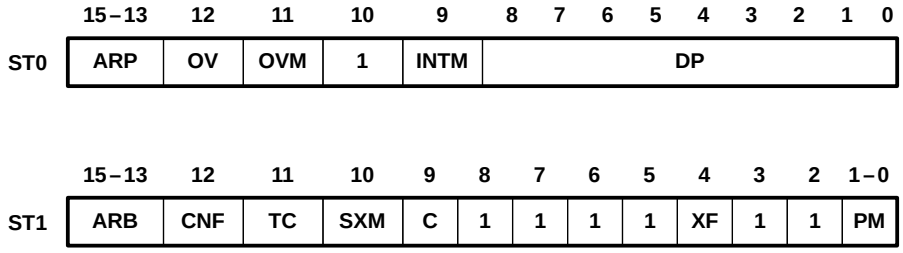


Figure 1. Status and Control Register Organization

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status and control registers (continued)

Table 4. Status Register Field Definitions†

FIELD	FUNCTION
ARB	Auxiliary register pointer buffer. Whenever the ARP is loaded, the old ARP value is copied to the ARB, except during an LST instruction. When the ARB is loaded by way of an LST #1 instruction, the same value is also copied to the ARP.
ARP	Auxiliary register pointer. ARP selects the AR to be used in indirect addressing. When the ARP is loaded, the old ARP value is copied to the ARB register. ARP can be modified by memory-reference instructions when using indirect addressing, and by the LARP, MAR, and LST instructions. The ARP is also loaded with the same value as ARB when an LST #1 instruction is executed.
C	Carry bit. C is set to 1 if the result of an addition generates a carry; it is reset to 0 if the result of a subtraction generates a borrow. Otherwise, C is reset after an addition or set after a subtraction, except when the instruction is ADD or SUB with a 16-bit shift. In these cases, the ADD can only set and the SUB can only reset the carry bit, but cannot affect it otherwise. The single-bit shift and rotate instructions also affect C, as well as the SETC, CLRC, and LST #1 instructions. Branch instructions have been provided to branch on the status of C. C is set to 1 on a reset.
CNF	On-chip RAM configuration control bit. If CNF is set to 0, the reconfigurable data dual-access RAM blocks are mapped to data space; otherwise, they are mapped to program space. The CNF can be modified by the SETC CNF, CLRC CNF, and LST #1 instructions. $\overline{RS}$ sets the CNF to 0.
DP	Data-memory page pointer. The 9-bit DP register is concatenated with the seven LSBs of an instruction word to form a direct memory address of 16 bits. DP can be modified by the LST and LDP instructions.
INTM	Interrupt-mode bit. When INTM is set to 0, all unmasked interrupts are enabled. When INTM is set to 1, all maskable interrupts are disabled. INTM is set and reset by the SETC INTM and CLRC INTM instructions. $\overline{RS}$ and $\overline{IACK}$ also set INTM. INTM has no effect on the unmaskable $\overline{RS}$ and $\overline{NMI}$ interrupts. Note that INTM is unaffected by the LST instruction. This bit is set to 1 by reset. It is also set to 1 when a maskable interrupt trap is taken.
OV	Overflow-flag bit. As a latched overflow signal, OV is set to 1 when overflow occurs in the ALU. Once an overflow occurs, the OV remains set until a reset, BCND/D on OV/NOV, or LST instruction clears OV.
OVM	Overflow-mode bit. When OVM is set to 0, overflowed results overflow normally in the accumulator. When OVM is set to 1, the accumulator is set to either its most positive or negative value upon encountering an overflow. The SETC and CLRC instructions set and reset this bit, respectively. LST can also be used to modify the OVM.
PM	Product-shift-mode bits. If these two bits are 00, the multiplier's 32-bit product is loaded into the ALU with no shift. If PM = 01, the product register (PREG) output is left-shifted one place and loaded into the ALU, with the LSB zero-filled. If PM = 10, the PREG output is left-shifted by 4 bits and loaded into the ALU, with the LSBs zero-filled. PM = 11 produces a right shift of 6 bits, sign-extended. Note that the PREG contents remain unchanged. The shift takes place when transferring the contents of the PREG to the ALU. PM is loaded by the SPM and LST #1 instructions. PM is cleared by $\overline{RS}$.
SXM	Sign-extension mode bit. SXM = 1 produces sign-extension on data as it is passed into the accumulator through the scaling shifter. SXM = 0 suppresses sign-extension. SXM does not affect the definitions of certain instructions; for example, the ADDS instruction suppresses sign-extension regardless of SXM. SXM is set by the SETC SXM instruction, reset by the CLRC SXM instruction, and can be loaded by the LST #1 instruction. SXM is set to 1 by reset.
TC	Test/control flag bit. TC is affected by the BIT, BITT, CMPR, LST #1, and NORM instructions. TC is set to a 1 if a bit tested by BIT or BITT is a 1, if a compare condition tested by CMPR exists between AR (ARP) and AR0, or if the exclusive-OR function of the two MSBs of the accumulator is true when tested by a NORM instruction. The conditional branch, call, and return instructions can execute based on the condition of TC.
XF	XF pin status bit. XF indicates the state of the XF pin, a general-purpose output pin. XF is set by the SETC XF and reset by the CLRC XF instructions. XF is set to 1 by reset.

† See Table 3 for definitions of acronyms and Table 16 for descriptions of opcode instructions.

central processing unit

The TMS320C2xx central processing unit (CPU) contains a 16-bit scaling shifter, a 16 × 16-bit parallel multiplier, a 32-bit central arithmetic logic unit (CALU), a 32-bit accumulator, and additional shifters at the outputs of both the accumulator and the multiplier. This section describes the CPU components and their functions. The functional block diagram shows the components of the CPU.

input scaling shifter

The TMS320C2xx provides a scaling shifter with a 16-bit input connected to the data bus and a 32-bit output connected to the CALU. This shifter operates as part of the path of data coming from program or data space to the CALU and requires no cycle overhead. It is used to align the 16-bit data coming from memory to the 32-bit CALU. This is necessary for scaling arithmetic as well as aligning masks for logical operations.

The scaling shifter produces a left shift of 0 to 16 on the input data. The LSBs of the output are filled with zeros; the MSBs can be either filled with zeros or sign-extended, depending upon the value of the SXM bit (sign-extension mode) of status register ST1. The shift count is specified by a constant embedded in the instruction word or by a value in the temporary register (TREG). The shift count in the instruction allows for specific scaling or alignment operations specific to that point in the code. The TREG base shift allows the scaling factor to be adaptable to the system's performance.

multiplier

The TMS320C2xx uses a 16 × 16-bit hardware multiplier that is capable of computing a signed or an unsigned 32-bit product in a single machine cycle. All multiply instructions, except the MPYU (multiply unsigned) instruction, perform a signed multiply operation. That is, two numbers being multiplied are treated as 2s-complement numbers, and the result is a 32-bit 2s-complement number. There are two registers associated with the multiplier: a 16-bit temporary register (TREG) that holds one of the operands for the multiplier, and a 32-bit product register (PREG) that holds the product.

Four product-shift modes (PM) are available at the PREG's output (PSCALE). These shift modes are useful for performing multiply/accumulate operations, performing fractional arithmetic, or justifying fractional products. The PM field of status register ST1 specifies the PM shift mode, as shown in Table 5.

Table 5. PSCALE Product-Shift Modes

PM	SHIFT	DESCRIPTION
00	no shift	Product feed to CALU or data bus with no shift
01	left 1	Removes the extra sign bit generated in a 2s-complement multiply to produce a Q31 product
10	left 4	Removes the extra four sign bits generated in a 16 × 13 2s-complement multiply to a produce a Q31 product when using the multiply by a 13-bit constant
11	right 6	Scales the product to allow up to 128 product accumulations without the possibility of accumulator overflow

The product can be shifted one bit to compensate for the extra sign bit gained in multiplying two 16-bit 2s-complement numbers (MPY). A 4-bit shift is used in conjunction with the MPY instruction with a short immediate value (13 bits or less) to eliminate the four extra sign bits gained in multiplying a 16-bit number by a 13-bit number. Finally, the output of PREG can be right-shifted 6 bits to enable the execution of up to 128 consecutive multiply/accumulates without the possibility of overflow.

The LT (load TREG) instruction normally loads TREG to provide one operand (from the data bus), and the MPY (multiply) instruction provides the section operand (also from the data bus). A multiplication can also be performed with a 13-bit immediate operand when using the MPY instruction. A product is then obtained every two cycles. When the code is executing multiple multiplies and product sums, the CPU supports the pipelining of the TREG load operations with CALU operations using the previous product. These pipeline operations that run in parallel with loading the TREG include: load ACC with PREG (LTP); add PREG to ACC (LTA); add PREG to ACC and shift TREG input data (DMOV) to next address in data memory (LTD); and subtract PREG from ACC (LTS).

multiplier (continued)

Two multiply/accumulate instructions (MAC and MACD) fully utilize the computational bandwidth of the multiplier, allowing both operands to be processed simultaneously. The data for these operations can be transferred to the multiplier each cycle by way of the program and data buses. This facilitates single-cycle multiply/accumulates when used with the repeat (RPT) instruction. In these instructions, the coefficient addresses are generated by program-address generation (PAGEN), while the data addresses are generated by data-address generation (DAGEN). This allows the repeated instruction to sequentially access the values from the coefficient table and step through the data in any of the indirect addressing modes.

The MACD instruction, when repeated, supports filter constructs (weighted running averages) so that as the sum-of-products is executed, the sample data is shifted in memory to make room for the next sample and to throw away the oldest sample.

The MPYU instruction performs an unsigned multiplication, which greatly facilitates extended-precision arithmetic operations. The unsigned contents of TREG are multiplied by the unsigned contents of the addressed data memory location, with the result placed in PREG. This allows the operands of greater than 16 bits to be broken down into 16-bit words and processed separately to generate products of greater than 32 bits. The SQRA (square/add) and SQRS (square/subtract) instructions pass the same value to both inputs of the multiplier for squaring a data-memory value.

After the multiplication of two 16-bit numbers, the 32-bit product is loaded into the 32-bit product register (PREG). The product from PREG can be transferred to the CALU or to data memory by way of the SPH (store product-high register) and the SPL (store product-low register) instructions. Note: the transfer of PREG to either the CALU or data bus passes through the product-scaling shifter (PSCALE) and is therefore affected by the product-shift mode defined by PM. This is important when saving PREG in an interrupt-service-routine-context save as the PSCALE shift effects cannot be modeled in the restore operation. PREG can be cleared by executing the MPY #0 instruction. The product register can be restored by loading the saved low half into TREG and executing the MPY #1 instruction. The high half is then loaded using the LPH instruction.

central arithmetic logic unit

The TMS320C2xx central arithmetic logic unit (CALU) implements a wide range of arithmetic and logical functions, the majority of which execute in a single clock cycle. This arithmetic logic unit (ALU) is referred to as central to differentiate it from a second ALU used for indirect-address-generation, called the auxiliary register arithmetic unit (ARAU). Once an operation is performed in the CALU, the result is transferred to the accumulator (ACC), where additional operations, such as shifting, can occur. Data that is input to the CALU can be scaled by the input data-scaling shifter (ISCALE) when coming from one of the data buses (DRDB or PRDB) or scaled by PSCALE when coming from the multiplier.

The CALU is a general-purpose arithmetic/logic unit that operates on 16-bit words taken from data memory or derived from immediate instructions. In addition to the usual arithmetic instructions, the CALU can perform Boolean operations, facilitating the bit manipulation ability required for a high-speed controller. One input to the CALU is always provided from the accumulator, and the other input can be provided from the product register (PREG) of the multiplier or the output of the scaling shifter (that has been read from data memory or from the ACC). After the CALU has performed the arithmetic or logical operation, the result is stored in the accumulator.

The TMS320C2xx supports floating-point operations for applications requiring a large dynamic range. The NORM (normalization) instruction is used to normalize fixed-point numbers contained in the accumulator by performing left shifts. The four bits of the TREG define a variable shift through the scaling shifter for the LACT/ADDT/SUBT (load/add to /subtract from accumulator with shift specified by TREG) instructions. These instructions are useful in floating-point arithmetic where a number needs to be denormalized—that is, floating-point to fixed-point conversion. They are also useful in the execution of an automatic gain control (AGC) going into a filter. The BITT (bit-test) instruction provides testing of a single bit of a word in data memory based on the value contained in the four LSBs of TREG.

central arithmetic logic unit (continued)

The CALU overflow-saturation mode can be enabled/disabled by setting/resetting the overflow mode (OVM) bit of ST0. When the CALU is in the overflow-saturation mode and an overflow occurs, the overflow flag is set and the accumulator is loaded with either the most positive or the most negative value representable in the accumulator, depending upon the direction of the overflow. The value of the accumulator upon saturation is 07FFFFFFh (positive) or 080000000h (negative). If the OVM status register bit is reset and an overflow occurs, the overflowed results are loaded into the accumulator with modification. (Note that logical operations cannot result in overflow.)

The CALU can execute a variety of branch instructions that depend on the status of the CALU and the accumulator. These instructions can be executed conditionally, based on any meaningful combination of these status bits. For overflow management, these conditions include the OV (branch on overflow) and EQ (branch on accumulator equal to zero). In addition, the BACC (branch to address in accumulator) instruction provides the ability to branch to an address specified by the accumulator (computed goto). Bit-test instructions (BIT and BITT), which do not affect the accumulator, allow the testing of a specified bit of a word in data memory.

The CALU also has an associated carry bit that is set or reset depending on various operations within the device. The carry bit allows more efficient computation of extended-precision products and additions or subtractions. It is also useful in overflow management. The carry bit is affected by most arithmetic instructions as well as the single-bit shift and rotate instructions. It is not affected by accumulator loads, logical operations, or other such non-arithmetic or control instructions.

The ADDC (add to accumulator with carry) and SUBB (subtract from accumulator with borrow) instructions provide the use of the previous value of carry in their addition/subtraction operation.

The one exception to the operation of the carry bit is in the use of ADD with a shift count of 16 (add to high accumulator) and SUB with a shift count of 16 (subtract from high accumulator) instructions. This case of the ADD instruction can set the carry bit only if a carry is generated, and this case of the SUB instruction can reset the carry bit only if a borrow is generated; otherwise, neither instruction affects it.

Two conditional operands, C and NC, are provided for branching, calling, returning, and conditionally executing based upon the status of the carry bit. The SETC, CLRC, and LST #1 instructions also can be used to load the carry bit. The carry bit is set to one on a hardware reset.

accumulator

The 32-bit accumulator is the registered output of the CALU. It can be split into two 16-bit segments for storage in data memory. Shifters at the output of the accumulator provide a left-shift of 0 to 7 places. This shift is performed while the data is being transferred to the data bus for storage. The contents of the accumulator remain unchanged. When the post-scaling shifter is used on the high word of the accumulator (bits 16–31), the MSBs are lost and the LSBs are filled with bits shifted in from the low word (bits 0–15). When the post-scaling shifter is used on the low word, the LSBs are zero-filled.

The SFL and SFR (in-place one-bit shift to the left/right) instructions and the ROL and ROR (rotate to the left/right) instructions implement shifting or rotating of the contents of the accumulator through the carry bit. The SXM status register bit affects the definition of the SFR (shift accumulator right) instruction. When SXM = 1, SFR performs an arithmetic right shift, maintaining the sign of the accumulator data. When SXM = 0, SFR performs a logical shift, shifting out the LSBs and shifting in a zero for the MSB. The SFL (shift accumulator left) instruction is not affected by the SXM bit and behaves the same in both cases, shifting out the MSB and shifting in a zero. RPT (repeat) instructions can be used with the shift and rotate instructions for multiple-bit shifts.

auxiliary registers and auxiliary-register arithmetic unit (ARAU)

The ’C2xx provides a register file containing eight auxiliary registers (AR0–AR7). The auxiliary registers are used for indirect addressing of the data memory or for temporary data storage. Indirect auxiliary-register addressing allows placement of the data memory address of an instruction operand into one of the auxiliary registers. These registers are referenced with a 3-bit auxiliary register pointer (ARP) that is loaded with a value from 0 through 7, designated AR0 through AR7, respectively. The auxiliary registers and the ARP can be loaded from data memory, the ACC, the product register, or by an immediate operand defined in the instruction. The contents of these registers can also be stored in data memory or used as inputs to the CALU.

The auxiliary register file is connected to the ARAU. The ARAU can autoindex the current auxiliary register while the data memory location is being addressed. Indexing either by ±1 or by the contents of AR0 can be performed. As a result, accessing tables of information does not require the CALU for address manipulation; therefore, the CALU is free for other operations in parallel.

memory

The ’C2xx implements three separate address spaces for program memory, data memory, and I/O. Each space accommodates a total of 64K 16-bit words. Within the 64K words of data space, the 256 to 32K words at the top of the address range can be defined to be external global memory in increments of powers of two, as specified by the contents of the global memory allocation register. Access to global memory is arbitrated using the global memory bus request ($\overline{BR}$) signal.

On the ’C2xx, the first 96 (0–5Fh) data memory locations are allocated for memory-mapped registers or are reserved. This memory-mapped register space contains various control and status registers including those for the CPU.

When using on-chip RAM, or high-speed external memory, the ’C2xx runs at full speed with no wait states. The ability of the DARAM to allow two accesses to be performed in one cycle, coupled with the parallel nature of the ’C2xx architecture, enables the device to perform three concurrent memory accesses in any given machine cycle. Externally, the READY line can be used to interface the ’C2xx to slower, less expensive external memory. Downloading programs from slow off-chip memory to on-chip RAM can speed processing while cutting system costs.

The ’C2xx DARAM allows writes to and reads from the RAM in the same cycle without the address restrictions of the SARAM. The DARAM is configured in three blocks: block 0 (B0), block 1 (B1), and block 2 (B2). Block 1 consists of 256 words in data memory and block 2 consists of 32 words in data memory. Block 0 is a 256-word block that can be configured as data or program memory. The SETC CNF (configure B0 as program memory) and CLRC CNF (configure B0 as data memory) instructions allow dynamic configuration of the memory maps through software. When using Block 0 as program memory, instructions can be downloaded from external program memory into on-chip RAM and then executed.

TMS320C209 (only)

The mask-programmable ROM is located in program memory space. Customers can arrange to have this ROM programmed with contents unique to any particular application. The ROM is enabled or disabled by the state of the MP/$\overline{MC}$ control input upon resetting the device. The ROM occupies the lowest block of program memory when enabled. When disabled, these addresses are located in the device’s external program memory space.

The ’C209 devices provide two types of RAM: single-access RAM (SARAM) and dual-access RAM (DARAM). The SARAM requires a full machine cycle to perform a read or a write. However, this is not one large RAM block in which only one access per cycle is allowed. It is made up of 2K-word size-independent RAM blocks and each one allows one CPU access per cycle. The CPU can read or write one block while accessing another block at the same time. The ’C209 processor supports multiple accesses to its SARAM in one cycle as long as they go to different RAM blocks. With an understanding of this structure, code and data can be appropriately arranged to improve code performance.

memory (continued)

The TMS320C203 includes three registers mapped to internal data space and peripheral registers mapped to internal I/O space. Figure 2, Table 6, and Table 7 describe these registers and show their respective addresses. They also show the effects of the memory-control pin $\overline{\text{BOOT}}$ and control bit CNF on the mapping of the respective memory spaces to on-chip or off-chip memory.

Both of the TMS320C2xx devices include 544 × 16 words of dual-access RAM. The ’C209 device includes 4K × 16 words of single-access RAM and 4K × 16 words of ROM integrated with CPU. Figure 2, Table 6, and Table 7 show the mapping of the memory blocks and the appropriate control bits and pins for the ’C203. For the ’C209 devices, Figure 3, Table 8, and Table 9, show the effects of the memory-control pins MP/$\overline{\text{MC}}$ and RAMEN, and control bit CNF on the mapping of the respective memory spaces to on-chip or off-chip memory.

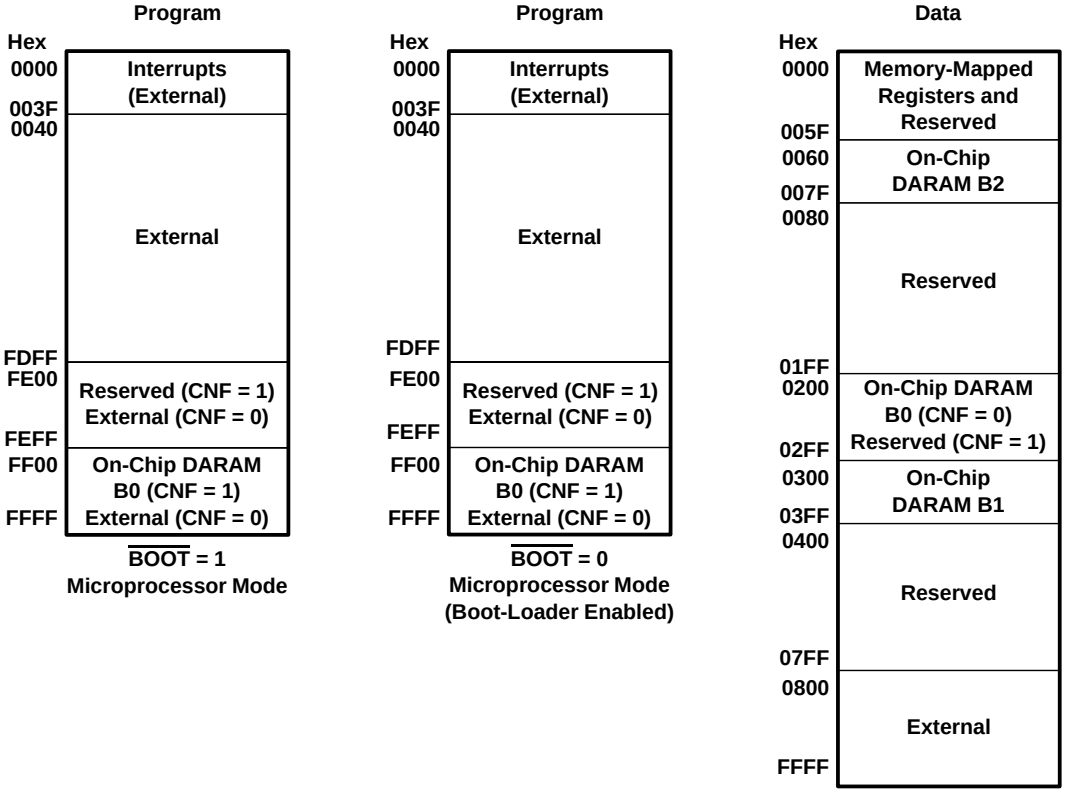

Figure 2. TMS320C203 Memory Map

Table 6. TMS320C203 Memory Map Configurations†

$\overline{\text{BOOT}}$	CNF	ON-CHIP MEMORY			OFF-CHIP MEMORY		
		PROGRAM	DATA	I/O	PROGRAM	DATA	I/O‡
0	0	—	0–7FF	FF00–FFFF	0000–FFFF	800–FFFF	0–FEFF
0	1	FE00–FFFF§	0–7FF	FF00–FFFF	0000–FDFF	800–FFFF	0–FEFF
1	0	—	0–7FF	FF00–FFFF	0000–FFFF	800–FFFF	0–FEFF
1	1	FE00–FFFF	0–7FF	FF00–FFFF	0000–FDFF	800–FFFF	0–FEFF

† Internal I/O locations 0FFE0h–0FFFFh are dedicated to the timer, serial-port control, wait-state generator registers, and reserved space.
‡ FF00–FF0F are reserved for test purposes and should not be used.
§ When $\overline{\text{BOOT}}$ = 0, the on-chip boot-loader at 0xFF00h is enabled. During boot time, memory address FE00–FFFF is reserved.

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memory (continued)

Table 7. TMS320C203 On-Chip Memory Map

DESCRIPTION OF MEMORY BLOCK	DATA ADDRS	PROG ADDRS	$\overline{\text{BOOT}}$	CNF BIT
On-chip boot-loader		0	low	
256 × 16 words dual-access RAM (B0)	0x100† 0x200†			0
256 × 16 words dual-access RAM (B0)		0xFE00† 0xFF00†		1
256 × 16 words dual-access RAM (B1)	0x300† 0x400†			
32 × 16 words dual-access RAM (B2)	0x60			

† Both of the addresses in each of these address pairs point to the same block of memory.

memory (continued)

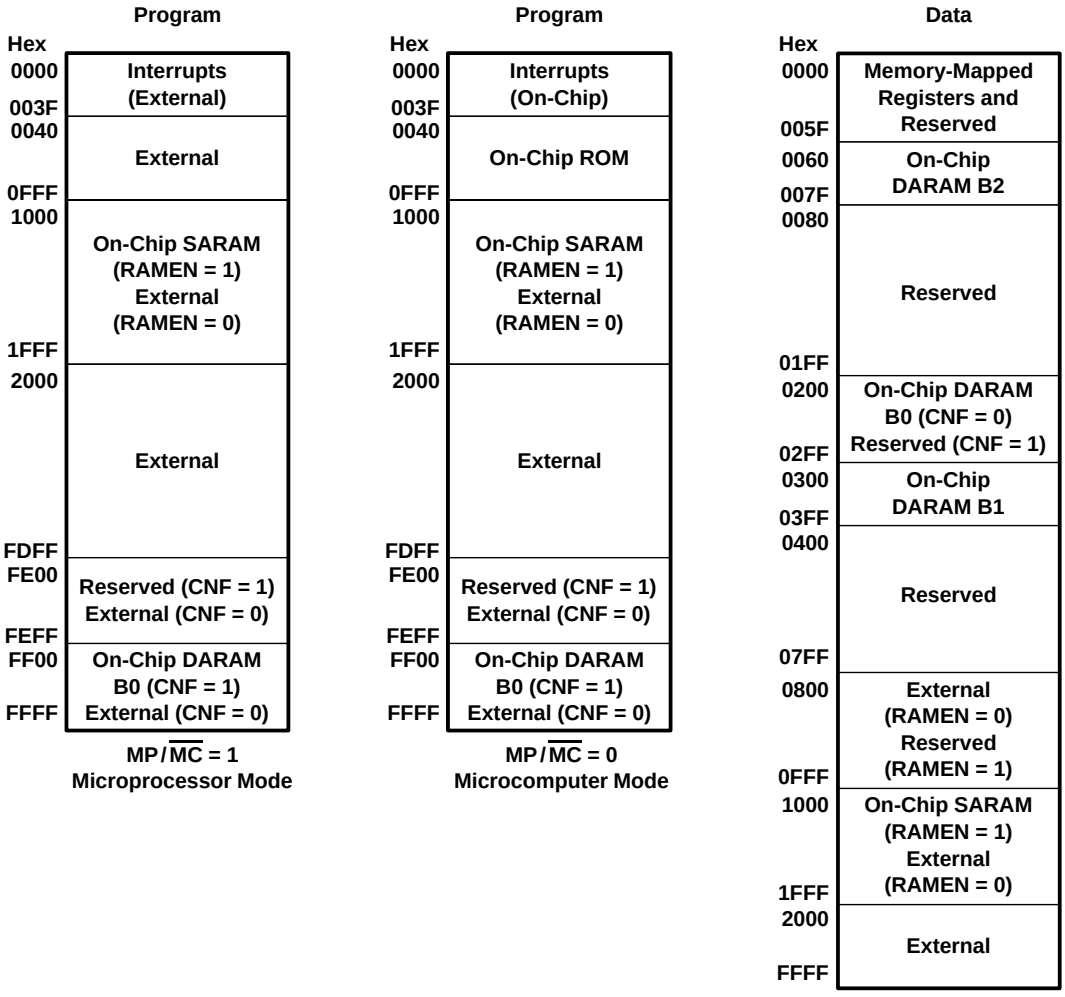

Figure 3. TMS320C209 Memory Map

ADVANCE INFORMATION

memory (continued)

Table 8. TMS320C209 Memory Map Configurations†

MP/$\overline{MC}$	RAMEN	CNF	ON-CHIP			OFF-CHIP		
			PROGRAM	DATA	I/O	PROGRAM	DATA	I/O‡
0	1	0	0–1FFF	0–1FFF	FFF0–FFFF	2000–FFFF	2000–FFFF	0–FFEF
0	1	1	0–1FFF FE00–FFFF	0–1FFF	FFF0–FFFF	2000–FDFF	2000–FFFF	0–FFEF
0	0	0	0–0FFF	0–07FF	FFF0–FFFF	1000–FFFF	0800–FFFF	0–FFEF
0	0	1	0–0FFF FE00–FFFF	0–07FF	FFF0–FFFF	1000–FDFF	0800–FFFF	0–FFEF
1	1	0	1000–1FFF	0–1FFF	FFF0–FFFF	0–FFF 2000–FFFF	2000–FFFF	0–FFEF
1	1	1	1000–1FFF FE00–FFFF	0–1FFF	FFF0–FFFF	0–FFF 2000–FDFF	2000–FFFF	0–FFEF
1	0	0		0–07FF	FFF0–FFFF	0–FFFF	0800–FFFF	0–FFEF
1	0	1	FE00–FFFF	0–07FF	FFF0–FFFF	0–FDFF	0800–FFFF	0–FFEF

† Internal I/O locations 0FFF0h–0FFFFh are dedicated to the timer, wait-state generator registers, and reserved space.
‡ FF00–FF0F are reserved for test purposes and should not be used.

Table 9. TMS320C209 On-Chip Memory Map

DESCRIPTION OF MEMORY BLOCK	DATA ADDRS	PROG ADDRS	MP/$\overline{MC}$	CNF BIT	RAMEN
4K × 16 words of factory-masked ROM		0	low		
256 × 16 words dual-access RAM (B0)	0x100§ 0x200§			0	
256 × 16 words dual-access RAM (B0)		0xFE00§ 0xFF00§		1	
256 × 16 words dual-access RAM (B1)	0x300§ 0x400§				
32 × 16 words dual-access RAM (B2)	0x60				
4096 × 16 words dual-access RAM	0x1000	0x1000			high

§ Both of the addresses in each of these address pairs point to the same block of memory.

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memory (continued)

Table 10 shows the names, addresses, and functional descriptions of the TMS320C203 memory and I/O internally mapped registers.

Table 10. TMS320C203 Memory and I/O Internally Mapped Registers†

NAME	ADDRESS	DESCRIPTION
IMR	DS@0004	Interrupt-mask register. IMR individually masks or enables the seven interrupts. Bit 0 shares the external interrupt pins INT1 and HOLD. INT2 and INT3 share bit 1. Bit 2 ties to the timer interrupt, TINT. Bits 3 and 4, RINT and XINT, respectively, are for the synchronous serial port, SSP. Bit 5, TXRXINT, shares the transmit and receive interrupts for the asynchronous serial port, ASP. Bit 6 is reserved for monitor mode emulation operations and should always be set to 0 except in conjunction with emulation monitor operations. Bits 7–15 are not used in the TMS320C203. IMR is set to 0 at reset.
GREG	DS@0005	Global memory allocation register. GREG specifies the size of the global memory space. GREG is set to 0 at reset.
IFR	DS@0006	Interrupt-flag register. IFR indicates that the TMS320C203 has latched an interrupt from one of the seven maskable interrupts. Bit 0 shares the external interrupt INT1 and HOLD. INT2 and INT3 share bit 1. Bit 2 ties to the timer interrupt, TINT. Bits 3 and 4, RINT and XINT, respectively, are for the synchronous serial port, SSP. Bit 5, TXRXINT, shares the transmit- and receive-interrupts for the asynchronous serial port, ASP. Bit 6 is reserved for monitor mode emulation operations and should always be set to 0 except in conjunction with emulation monitor operations. Writing a 1 to the respective interrupt bit clears an active flag and the respective pending interrupt. Writing a 1 to an inactive flag has no effect. Bits 7–15 are not used in the TMS320C203. IMR is set to 0 at reset.
CLK	IS@FFE8	CLKOUT1 on or off. At reset, CLKOUT1 is configured as a zero for the pin to be active (on). If CLKOUT1 is a 1, the CLKOUT1 pin is turned off.
ICR	IS@FFEC	Interrupt-control register. ICR is used to determine which interrupt is active since INT1 and HOLD share an interrupt vector as do INT1 and INT3. A portion of this register is for mask/unmask (similar to IMR) and another portion is for pending interrupts (similar to IFR). At reset, all bits are zeroed, enabling HOLD mode. The MODE bit is used by the hold-generating circuit to determine if a HOLD or INT1 is active.
SDTR	IS@FFF0	Synchronous serial-port (SSP) transmit and receive register
SSPCR	IS@FFF1	Synchronous serial-port control register
ADTR	IS@FFF4	Asynchronous serial-port (ASP) transmit and receive register
ASPCR	IS@FFF5	Asynchronous serial-port control register. ASPCR controls the asynchronous serial port operation.
IOSR	IS@FFF6	I/O status register. IOSR detects current levels (and changes with inputs) on pins IO0–IO3 and status of UART.
BRD	IS@FFF7	Baud-rate divisor. Used to set baud rate of UART
TCR	IS@FFF8	Timer-control register. TCR contains the control bits that define the divide-down ratio, start/stop the timer, and reload the period. Also contained in TCR is the current count in the prescaler. Reset initializes the timer divide-down ratio to 0 and starts the timer.
PRD	IS@FFF9	Timer-period register. PRD contains the 16-bit period that is loaded into the timer counter when the counter borrows or when the reload bit is activated. Reset initializes the PRD to 0xFFFF.
TIM	IS@FFFA	Timer-counter register. TIM contains the current 16-bit count of the timer. Reset initializes the TIM to 0xFFFF.
WSGR	IS@FFFC	Wait-state-generator register. WSGR contains 12 control bits to enable 0, . . . ,7 wait states to program, data, and I/O space. Reset initializes the WSGR to 0x0FFFh.

† During on-chip I/O access, IS, RD, and WR are not visible at the pins ('C203 only).

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memory (continued)

Table 11 shows the names, addresses, and functional descriptions of the TMS320C209 memory-mapped registers.

Table 11. TMS320C209 Memory-Mapped Registers

NAME	ADDRESS	DESCRIPTION
IMR	DS@0004	Interrupt-mask register. IMR individually masks or enables the seven interrupts. The lower three bits align to the three external interrupt pins (bit 0 ties to INT1, bit 1 to INT2, and bit 2 to INT3). Bit 3 ties to the timer interrupt. Bits 4 and 5 are not used in the TMS320C209. Bit 6 is reserved for monitor mode emulation operations and should always be set to 0 except in conjunction with emulation monitor operations. Bits 7–15 are not used in the TMS320C209. IMR is set to 0 at reset.
GREG	DS@0005	Global memory allocation register. GREG specifies the size of the global memory space. GREG is set to 0 at reset.
IFR	DS@0006	Interrupt-flag register. IFR indicates that the 'C2xx core has latched an interrupt pulse from one of the maskable interrupts. The lower three bits align to the three external interrupt pins (bit 0 ties to INT1, bit 1 to INT2, and bit 2 to INT3). Bit 3 ties to the timer interrupt. Bits 4–15 are reserved for monitor mode emulation operations and should always be set to 0 except in conjunction with emulation monitor operations. A 1 indicates an active interrupt in the respective interrupt location. Writing a 1 to the respective interrupt bit clears an active flag and the respective pending interrupt. Writing a 1 to an inactive flag has no affect. IFR is set to 0 at reset.
TCR	IS@FFFC	Timer-control register. TCR contains the control bits that define the divide-down ratio, start/stop the timer, and reload the period. Also contained in TCR is the current count in the prescaler. Reset initializes the timer divide-down ratio to 0 and starts the timer.
PRD	IS@FFFD	Timer-period register. PRD contains the 16-bit period that is loaded into the timer counter when the counter borrows or when the reload bit is activated. Reset initializes the PRD to 0xFFFF.
TIM	IS@FFFE	Timer-counter register. TIM contains the current 16-bit count of the timer. Reset initializes the TIM to 0xFFFF.
WSGR	IS@FFFF	Wait-state generator register. WSGR contains the three control bits to enable a single wait state each of program, data, and I/O space as well as the address-visibility-enable bit. Reset initializes WSGR to 0xF.

external interface

The TMS320C2xx can address up to 64K × 16 words of memory or registers in each of the program, data, and I/O spaces. On-chip memory, when enabled, removes some of this off-chip range. In data space, the high 32K words can be dynamically mapped either locally or globally using the GREG register as described in the *TMS320C2xx User's Guide* (literature number SPRU127). A data-memory access mapped as global asserts $\overline{BR}$ low (with timing similar to the address bus) (see Table 9).

The CPU of the TMS320C2xx schedules a program-fetch, data-read, and data-write on the same machine cycle. This is because from on-chip memory, the CPU can execute all three of these operations in the same cycle. However, the external interface multiplexes the internal buses to one address bus and one data bus. The external interface sequences these operations to complete first the data-write, then the data-read, and finally the program-read.

The 'C2xx supports a wide range of system-interfacing requirements. Program, data, and I/O address spaces provide interface to memory and I/O, thereby maximizing system throughput. The full 16-bit address and data bus, along with the $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ space-select signals, allow addressing of 64K 16-bit words in each of the three spaces.

I/O design is simplified by having I/O treated the same way as memory. I/O devices are mapped into the I/O address space using the processor's external address and data buses in the same manner as memory-mapped devices.

external interface (continued)

The ’C2xx external parallel interface provides various control signals to facilitate interfacing to the device. The R/$\overline{W}$ output signal is provided to indicate whether the current cycle is a read or a write. The $\overline{STRB}$ output signal provides a timing reference for all external cycles. For convenience, the device also provides the $\overline{RD}$ and the $\overline{WE}$ output signals, which indicate a read and a write cycle, respectively, along with timing information for those cycles. The availability of these signals minimizes external gating necessary for interfacing external devices to the ’C2xx.

Interface to memory and I/O devices of varying speeds is accomplished by using the READY line. When transactions are made with slower devices, the ’C2xx processor waits until the other device completes its function and signals the processor by way of the READY line. Once a ready indication is provided back to the ’C2xx from the external device, execution continues. **On the ’C209 device, the READY line is required (active high) to complete reads or writes to internal I/O-mapped registers. On the ’C203 devices, the READY line is required to be active high during boot time.**

The bus-request ($\overline{BR}$) signal is used in conjunction with the other ’C2xx interface signals to arbitrate external global-memory accesses. Global memory is external data-memory space in which the $\overline{BR}$ signal is asserted at the beginning of the access. When an external global-memory device receives the bus request, it responds by asserting the READY signal after the global memory access is arbitrated and the global access is completed.

The TMS320C2xx supports zero-wait-state reads on the external interface. However, to avoid bus conflicts, writes take two cycles. This allows the TMS320C2xx to buffer the transition of the data bus from input to output (or output to input) by a half cycle. In most systems, TMS320C2xx ratio of reads to writes is significantly large to minimize the overhead of the extra cycle on writes.

Wait states can be generated when accessing slower external resources. The wait states operate on machine-cycle boundaries and are initiated either by using READY or by using the software wait-state generator. READY can be used to generate any number of wait states.

interrupts and subroutines

The ’C2xx implements three general-purpose interrupts, $\overline{INT3}$–$\overline{INT1}$, along with reset ($\overline{RS}$) and the nonmaskable interrupt ($\overline{NMI}$), which are available for external devices to request the attention of the processor. Internal interrupts are generated by the synchronous serial port (RINT and XINT) (’C203 only), the asynchronous serial port (TXRXINT) (’C203 only), the timer (TINT), the UART, and the software-interrupt (TRAP, INTR and NMI) instructions. Interrupts are prioritized with $\overline{RS}$ having the highest priority, followed by $\overline{NMI}$, and timer (TINT) (for ’C209) or UART (for ’C203) having the lowest priority. Additionally, any interrupt, except $\overline{RS}$ and $\overline{NMI}$, can be individually masked with a dedicated bit in the interrupt mask register (IMR) and can be cleared, set, or tested using its own dedicated bit in the interrupt flag register (IFR). The reset and NMI functions are not maskable.

All interrupt vector locations are on two-word boundaries so that branch instructions can be accommodated in those locations if desired.

A built-in mechanism protects multicycle instructions from interrupts. If an interrupt occurs during a multicycle instruction, the interrupt is not processed until the instruction completes execution. This mechanism applies to instructions that are repeated (using the RPT instruction) and to instructions that become multicycle because of wait states.

Each time an interrupt is serviced or a subroutine is entered, the program counter (PC) is pushed onto an internal hardware stack, providing a mechanism for returning to the previous context. The stack contains eight locations, allowing interrupts or subroutines to be nested up to eight-levels deep.

reset

The TMS320C203 provides an active-low reset ($\overline{RS}$) only, while the TMS320C209 provides both an RS and an $\overline{RS}$.

RS and $\overline{RS}$, the TMS320C209 resets, are not synchronized. A minimum pulse duration of six cycles ensures that an asynchronous reset signal resets the device. Either RS or $\overline{RS}$ can reset the device with RS being active high and $\overline{RS}$ being active low. The TMS320C2xx fetches its first instruction approximately sixteen cycles after the rising edge of $\overline{RS}$ (either 'C203 or 'C209) or falling edge of RS ('C209 only).

Please note that the reset action halts all operations whether they are completed or not. Therefore, the state of the system and its data cannot be maintained through the reset operation. For example, if the device is writing to an external resource when the reset is initiated, the write is aborted. This can and will corrupt data in system resources. It is, therefore, necessary to reinitialize the system after a reset.

power-down modes

The 'C2xx implements several power-down modes in which the 'C2xx core enters a dormant state and dissipates considerably less power. A power-down mode is invoked either by executing the IDLE instruction or by driving the $\overline{HOLD}$ ('C203 only) input low and executing HOLD mode. When the $\overline{HOLD}$ signal initiates the power-down mode, on-chip peripherals continue to operate; this power-down mode is terminated when $\overline{HOLD}$ goes inactive ('C203 only).

While the 'C2xx is in a power-down mode, all of its internal contents are maintained; this allows operation to continue unaltered when the power-down mode is terminated. All CPU activities are halted when the IDLE instruction is executed, but the CLKOUT1 pin remains active depending on the status of the interrupt-control (IC) register ('C203 only). The peripheral circuits continue to operate, allowing peripherals such as serial ports and timers to take the CPU out of its powered-down state. A power-down mode, when initiated by an IDLE instruction, is terminated upon receipt of an interrupt.

software-controlled wait-state generator

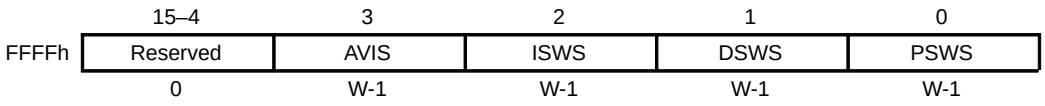
Due to the fast cycle time of the TMS320C2xx devices, it is often necessary to operate with wait states to interface with external logic and memory. For many systems, one wait state is adequate.

TMS320C209

When operating the TMS320C209 at full speed, it is difficult to respond fast enough to provide a READY-based wait state for the first cycle. For this reason, the TMS320C209 includes a simple software-controlled wait-state generator to provide the first wait state.

The software-controlled wait-state generator can be programmed to generate the first wait state for a given external space. The wait-state generator (WSGR) has four wait-state bits: AVIS, DATA (DSWS), PROG (PSWS), and I/O (ISWS). The wait-state generator inserts a wait state to a given memory space if the respective bit is set to 1, regardless of the condition of the READY signal. Then, READY can be used to further extend the wait states. The AVIS bit differs from the other WSGR bits because it does not generate a wait state but enables the address-visibility mode of the 'C209. This mode allows the internal program address to be presented to the address bus when this bus is not used for an external access. The WSGR bits are initially set to 1 by reset so that the device can operate from slow memory. After initialization, the AVIS bit should be set to 0 for production systems to reduce power and noise. The WSGR register (shown in Figure 4 and Table 12) resides at I/O port 0xFFFFh.

software-controlled wait-state generator (continued)



	15–4	3	2	1	0
FFFFh	Reserved	AVIS	ISWS	DSWS	PSWS
	0	W-1	W-1	W-1	W-1

LEGEND:
0 = Always read as zeros; W = Write access; -n = Value after reset

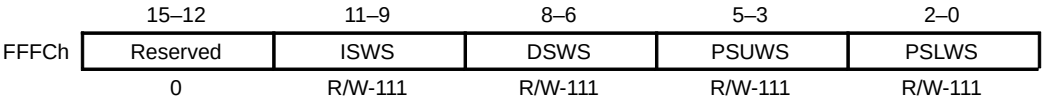
Figure 4. TMS320C209 Wait-State Generator Control Register (WSGR)

Table 12. Bit Functions of the TMS320C209 Wait-State Generator Control Register (WSGR)

BIT NO.	BIT NAME	DESCRIPTION
0	PSWS	External program-space wait-state bit on. When active, PSWS = 1 applies one wait state to all reads to off-chip program space (writes always take at least two cycles regardless of PSWS or READY). The memory cycle can be further extended using the READY signal. However, the READY signal does not override the wait state generated by PSWS. This bit is set to 1 (active) by reset (RS or $\overline{RS}$).
1	DSWS	External data-space wait-state bit on. When active, DSWS = 1 applies one wait state to all reads to off-chip data space (writes always take at least two cycles regardless of DSWS or READY). The memory cycle can be further extended using the READY signal. However, the READY signal does not override the wait state generated by DSWS. This bit is set to 1 (active) by reset (RS or $\overline{RS}$).
2	ISWS	External input-/output-space wait-state bit on. When active, ISWS = 1 applies one wait state to all reads to off-chip I/O space (writes always take at least two cycles regardless of ISWS or READY). The memory cycle can be further extended using the READY signal. However, the READY signal does not override the wait state generated by ISWS. This bit is set to 1 (active) by reset (RS or $\overline{RS}$).
3	AVIS	Address visibility mode. When active high, AVIS presents the internal program address out of the logic-interface address bus if the bus is not currently used in an external memory operation. The internal address is presented to provide a trace mechanism of internal code operation. Therefore, the memory-control signals are not active. AVIS is set to 1 (active) by reset (RS or $\overline{RS}$). AVIS should be deactivated in production systems to reduce system power and noise.
15–4	Reserved	Always read as zeros.

TMS320C203

The software wait-state generator can be programmed to generate between zero and seven wait states for a given space. The WSGR has 12 bits: three DATA, six PROGRAM, and three I/O. The wait-state generator inserts a wait state(s) to a given memory space based on the value of the three bits, regardless of the condition of the READY signal. The READY signal can be used to extend the wait state further. All bits are set to 1 at reset so that the device can operate from slow memory from reset. The WSGR register (shown in Figure 5, Table 13 and Table 14) resides at I/O port 0xFFFCh.



	15–12	11–9	8–6	5–3	2–0
FFFCh	Reserved	ISWS	DSWS	PSUWS	PSLWS
	0	R/W-111	R/W-111	R/W-111	R/W-111

LEGEND:
0 = Always read as zeros; R = Read access; W = Write access; -n = Value after reset

Figure 5. TMS320C203 Wait-State Generator Control Register (WSGR)

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TMS320C203 (continued)

Table 13. Bit Functions of the TMS320C203 Wait-State Generator Control Register (WSGR)

BITS	NAME	DESCRIPTION
2–0	PSLWS	External program-space wait states (lower). PSLWS determines that between 0–7 wait states are applied to all reads and writes to off-chip lower-program-space address (0h–7FFFh). The memory cycle can be further extended using the READY signal. The READY signal does not override the wait states generated by PSLWS. Bits 2–0 are set to 1 (active) by reset ($\overline{RS}$).
5–3	PSUWS	External program-space wait states (upper). PSUWS determines that between 0–7 wait states are applied to all reads and writes to off-chip upper-program-space address (8000h–0FFFFh). The memory cycle can be further extended using the READY signal. The READY signal does not override the wait states generated by PSUWS. Bits 5–3 are set to 1 (active) by reset ($\overline{RS}$).
8–6	DSWS	External data-space wait states. DSWS determines that between 0–7 wait states are applied to all reads and writes to off-chip data space. The memory cycle can be further extended using the READY signal. The READY signal does not override the wait states generated by DSWS. Bits 8–6 are set to 1 (active) by reset ($\overline{RS}$).
11–9	ISWS	External input / output-space wait state. ISWS determines that between 0–7 wait states are applied to all reads and writes to off-chip I / O space. The memory cycle can be further extended using the READY signal. The READY signal does not override the wait states generated by ISWS. Bits 11–9 are set to 1 (active) by reset ($\overline{RS}$).
15–12	Reserved	Always read as zeros.

Table 14. Bit Settings for TMS320C203 Wait-State(s) Programming

BITS 11, 8, 5, 2	BITS 10, 7, 4, 1	BITS 9, 6, 3, 0	WAIT STATES FOR PROGRAM, DATA, AND I/O
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

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timer

The ’C2xx features a 16-bit timing circuit with a 4-bit prescaler. This timer clocks between one-half and one thirty-second the machine rate of the device itself, depending upon the programmable timer’s divide-down ratio. This timer can be stopped, restarted, reset, or disabled by specific status bits.

The timer can be used to generate CPU interrupts periodically. The timer is decremented by one at every CLKOUT1 cycle. A timer interrupt (TINT) and a pulse equal to the duration of a CLKOUT1 cycle on the external TOUT pin are generated each time the counter decrements to zero. The timer, therefore, provides a convenient mean of performing periodic I/O or other functions.

TMS320C209 input clock options

The TMS320C209 includes two clock options. The first option (÷2) operates the CPU at half the input clock rate. The second option (×2) doubles the input clock and phase-locks the output clock with the input clock. The ÷2 mode is enabled by tying the CLKMOD pin low. The ×2 mode is enabled by tying the CLKMOD pin high.

The clock-doubler option of the ’C209 uses an internal phase-locked loop (PLL). The PLL requires approximately 2500 cycles to lock. The rising edge of $\overline{RS}$ (or falling edge of RS) must be delayed until at least three cycles after the PLL has stabilized. Accordingly, a switch from ÷2 to ×2 mode should not be made while the processor is running because the internal clock generator can generate minimum clock pulse width specification violations. The $\overline{RS}$ or RS signals should be in their active state if the CLKMOD pin is changed.

TMS320C203 input clock options

The TMS320C203 provides multiple clock modes of: ÷2, ×1, ×2, ×4. The clock-mode configuration cannot be dynamically changed without executing another reset. The operation of the PLL circuit is affected by the operating voltage of the device. If the device is operating at 5 V, then the PLL5V signal should be tied high. For 3.3-V operation, PLL5V should be tied low.

synchronous serial port (TMS320C203 only)

A full-duplex, bidirectional, 16-bit on-chip synchronous serial port provides direct communication with serial devices such as CODECs, serial analog-to-digital converters (A/Ds), and other serial systems. The interface signals are compatible with CODECs and many other serial devices. The serial port can also be used for intercommunication between processors in multiprocessing applications.

Both receive and transmit operations have a four-deep first-in-first-out (FIFO). The advantage of having a FIFO is to alleviate the CPU from being loaded with the task of servicing a transmit-data or receive-data on every interrupt, thereby, allowing a continuous communications stream of 16-bit data packets. The continuous mode provides operation that once initiated, requires no further frame synchronization pulses when transmitting at maximum packet frequency. The maximum transmission rate for both transmit and receive operations is CPU speed divided by two or CLKOUT1(frequency)/2. Therefore, the maximum rate is 20 Mbps at 25 ns and 14.28 Mbps at 35 ns. The serial port is fully static and functions at arbitrarily low clocking frequencies. When the serial ports are in reset, the device can be configured to shut off the serial port internal clocks, allowing the device to run in a lower-power mode of operation.

Three signals are necessary to connect the transmit pins of the transmitting device with the receive pins of the receiving device for data transmission. The transmit-serial-data signal (DX) sends the actual data. The transmit-frame-synchronization signal (FSX) initiates the transfer (at the beginning of the packet), and the transmit-clock signal (CLKX) clocks the bit transfer. The corresponding pins on the receiving device are DR, FSR and CLKR, respectively.

asynchronous serial port (TMS320C203 only)

The universal asynchronous serial port (UART) is full-duplex, and transmits and receives 8-bit data only. For transmit and receive, there is one start bit and one or two configurable stop bits by way of the asynchronous serial-port control register (ASPCR). Double-buffering or transmit/receive data is used in all modes. Baud-rate generation uses the BRD (baud-rate divisor) register to obtain the baud rate. The maximum baud rate is 2.5 Mbps at 250000 characters per second (at 25-ns instruction cycle time).

The asynchronous serial port contains an autobaud-detection feature that allows it to automatically lock to the incoming data rate. Autobaud detection is enabled by setting the CAD bit in the ASPCR to 1 and the ADC bit in the I/O status register (IOSR) to 0. See the *TMS320C2xx User's Guide* (literature number SPRU127) for details.

TMS320C2xx scan-based emulation

TMS320C2xx devices use scan-based emulation for code-development and hardware-development support. Scan-based emulation allows the emulator to control the processor in the system without the use of intrusive cables to the full pinout of the device. The '2xx devices do not support boundary-scan logic for board interconnect testing.

multiprocessing (TMS320C203 only)

The flexibility of the ’C2xx allows configurations to satisfy a wide range of system requirements; the device can be used in a variety of system configurations, including but not limited to the following:

- A standalone processor
- A multiprocessor with devices in parallel
- A slave/host multiprocessor with global memory space
- A peripheral processor interfaced by way of processor-controlled signals to another device

For multiprocessing applications, the ’C2xx has the capability of allocating global memory space and communicating with that space by way of the $\overline{BR}$ and READY control signals. Global memory is data memory shared by more than one device. Global-memory access must be arbitrated. The 8-bit memory-mapped global-memory-allocation register (GREG) specifies part of the ’C2xx’s data memory as global external memory. The contents of the register determine the size of the global memory space. If the current instruction addresses an operand within that space, $\overline{BR}$ is asserted to request control of the bus. The length of the memory cycle is controlled by the READY line.

The ’C203 supports direct-memory access (DMA) to its external program, data, and I/O spaces using the $\overline{HOLD}$ and $\overline{HOLDA}$ signals. Another device can take complete control of the ’C2xx’s external memory interface by asserting $\overline{HOLD}$ low and executing HOLD mode. This causes the ’C2xx to place its address, data, and memory-control signals in the high-impedance state and assert $\overline{HOLDA}$.

In ’C203, HOLD logic is not activated by hardware only. It is a combination of hardware interrupt (INT1 in MODE 0) and software instruction IDLE. See the *TMS320C2xx User’s Guide* (literature number SPRU127) for details.

instruction set

The ’C2xx microprocessor implements a comprehensive instruction set that supports both numeric-intensive signal-processing operations and general-purpose applications, such as multiprocessing and high-speed control. Source code for the ’C1x and ’C2x DSPs is upward-compatible with the ’C2xx.

For maximum throughput, the next instruction is prefetched while the current one is being executed. Because the same data lines are used to communicate to external data, program, or I/O space, the number of cycles an instruction requires to execute varies depending upon whether the next data-operand fetch is from internal or external memory. Highest throughput is achieved by maintaining data memory on chip and using either internal or fast external program memory.

addressing modes

The ’C2xx instruction set provides four basic memory-addressing modes: direct, indirect, immediate and register.

For direct addressing, the instruction word contains the lower seven bits of the data-memory address. This field is concatenated with the nine bits of the data-memory page pointer (DP) to form the 16-bit data-memory address. Therefore, in the direct-addressing mode, data memory is effectively paged with a total of 512 pages, with each page containing 128 words.

Indirect addressing accesses data memory through the auxiliary registers. In this addressing mode, the address of the instruction operand is contained in the currently selected auxiliary register. Eight auxiliary registers (AR0–AR7) provide flexible and powerful method of indirect addressing. To select a specific auxiliary register, the auxiliary register pointer (ARP) is loaded with a value from 0 to 7 for AR0 through AR7, respectively.

addressing modes (continued)

There are seven types of indirect addressing: autoincrement or autodecrement, postindexing by either adding or subtracting the contents of AR0, single indirect addressing with no increment or decrement, and bit-reversed addressing [used in fast Fourier transforms (FFTs)] with increment or decrement. All operations are performed on the current auxiliary register in the same cycle as the original instruction, following which the current auxiliary register and ARP can be modified.

In immediate addressing, the actual operand data is provided in a portion of the instruction word or words. There are two types of immediate addressing: long and short. In short immediate addressing, the data is contained in a portion of the bits in a single-word instruction. In long immediate addressing, the data is contained in the second word of a two-word instruction. The immediate-addressing mode is useful for data that does not need to be stored or used more than once during the course of program execution, such as initialization of values, constants, and so forth.

The register-addressing mode uses operands in CPU registers either explicitly, such as with a direct reference to a specific register, or implicitly, with instructions that intrinsically reference certain registers. In either case, operand reference is simplified because 16-bit values can be used without specifying a full 16-bit operand address or immediate value.

repeat feature

The repeat function can be used with instructions (as defined in Table 16) such as multiply/accumulate (MAC and MACD), block move (BLDD and BLPD), I/O transfer (IN/OUT), and table read/write (TBLR/TBLW). These instructions, although normally multicycled, are pipelined when the repeat feature is used, and they effectively become single-cycle instructions. For example, the table-read (TBLR) instruction may take three or more cycles to execute, but when the instruction is repeated, a table location can be read every cycle.

The repeat counter (RPTC) is loaded with the addressed data memory location if direct or indirect addressing mode is used, and with an 8-bit immediate value if short immediate addressing is used. The RPTC register is loaded by the RPT instruction. This results in a maximum of N + 1 executions of a given instruction. RPTC is cleared by reset. Once an RPT instruction is decoded, all interrupts including NMI (excluding reset) are masked until the completion of the repeat loop.

instruction set summary

This section summarizes the opcodes of the instruction set for the TMS320C2xx DSP devices. This instruction set is a superset of the ’C1x and ’C2x instruction sets. The instructions are alphabetized by the mnemonic. The symbols in Table 15 are used in the instruction set summary table (Table 16). The Texas Instruments ’C2xx assembler accepts ’C1x and ’C2x instructions.

For detailed information on instruction operation (that is, mnemonic syntax, words, cycles, and opcodes), see the *TMS320C2xx User’s Guide* (literature number SPRU127).

instruction set summary (continued)

Table 15. Opcode Symbols

SYMBOL	DESCRIPTION
A	Address
ACC	Accumulator
ACCB	Accumulator buffer
ARx	Auxiliary register value (0–7)
BITx	4-bit field specifies which bit to test for the BIT instruction
BMAR	Block-move address register
DBMR	Dynamic bit-manipulation register
I	Addressing-mode bit
II...II	Immediate operand value
INTM	Interrupt-mode flag bit
INTR#	Interrupt vector number
K	Constant
PREG	Product register
PROG	Program memory
RPTC	Repeat counter
SHF, SHFT	3/4-bit shift value
TC	Test-control bit
T P	Two bits used by the conditional execution instructions to represent the conditions TC, NTC, and BIO. T P Meaning 0 0 $\overline{\text{BIO}}$ low 0 1 TC = 1 1 0 TC = 0 1 1 None of the above conditions
TREGn	Temporary register n (n = 0, 1, or 2)
Z L V C	4-bit field representing the following conditions: Z: ACC = 0 L: ACC < 0 V: Overflow C: Carry A conditional instruction contains two of these 4-bit fields. The 4-LSB field of the instruction is a 4-bit mask field. A 1 in the corresponding mask bit indicates that the condition is being tested. The second 4-bit field (bits 4–7) indicates the state of the conditions designated by the mask bits as being tested. For example, to test for ACC ≥ 0, the Z and L fields are set while the V and C fields are not set. The next 4-bit field contains the state of the conditions to test. The Z field is set to indicate testing of the condition ACC = 0, and the L field is reset to indicate testing of the condition ACC ≥ 0. The conditions possible with these 8 bits are shown in the BCND and CC instructions. To determine if the conditions are met, the 4-LSB bit mask is ANDed with the conditions. If any bits are set, the conditions are met.

instruction set summary (continued)

Table 16. TMS320C2xx Instruction Set Summary

C2xx MNEMONIC	DESCRIPTION	WORDS/ CYCLES	OPCODE MSB			LSB
ABS	Absolute value of accumulator	1/1	1011	1110	0000	0000
ADD	Add to accumulator with shift	1/1	0010	SHFT	IADD	RESS
	Add to high accumulator	1/1	0110	0001	IADD	RESS
	Add to accumulator short immediate	1/1	1011	1000	KKKK	KKKK
	Add to accumulator long immediate with shift	2/2	1011	1111	1001	SHFT
ADDC	Add to accumulator with carry	1/1	0110	0000	IADD	RESS
ADDS	Add to low accumulator with sign extension suppressed	1/1	0110	0010	IADD	RESS
ADDT	Add to accumulator with shift specified by T register	1/1	0110	0011	IADD	RESS
ADRK	Add to auxiliary register short immediate	1/1	0111	1000	KKKK	KKKK
AND	AND with accumulator	1/1	0110	1110	IADD	RESS
	AND immediate with accumulator with shift	2/2	1011	1111	1011	SHFT 16-Bit Constant
	AND immediate with accumulator with shift of 16	2/2	1011	1110	1000	0001 16-Bit Constant
APAC	Add P register to accumulator	1/1	1011	1110	0000	0100
B	Branch unconditionally	2/4	0111	1001	IADD	RESS Branch Address
BACC	Branch to address specified by accumulator	1/4	1011	1110	0010	0000
BANZ	Branch on auxiliary register not zero	2/4/2	0111	1011	IADD	RESS Branch Address
BCND	Branch if TC bit ≠ 0	2/4/2	1110	0001	0000	0000 Branch Address
	Branch if TC bit = 0	2/4/2	1110	0010	0000	0000 Branch Address
	Branch on carry	2/4/2	1110	0011	0001	0001 Branch Address
	Branch if accumulator ≥ 0	2/4/2	1110	0011	1000	1100 Branch Address
	Branch if accumulator > 0	2/4/2	1110	0011	0000	0100 Branch Address
	Branch on I/O status low	2/4/3	1110	0000	0000	0000 Branch Address
	Branch if accumulator ≤ 0	2/4/2	1110	0011	1100	1100 Branch Address
	Branch if accumulator < 0	2/4/2	1110	0011	0100	0100 Branch Address
	Branch on no carry	2/4/2	1110	0011	0000	0001 Branch Address
	Branch if no overflow	2/4/2	1110	0011	0000	0010 Branch Address

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instruction set summary (continued)

Table 16. TMS320C2xx Instruction Set Summary (Continued)

C2xx MNEMONIC	DESCRIPTION	WORDS/ CYCLES	OPCODE			
			MSB			LSB
BCND	Branch if accumulator ≠ 0	2/4/2	1110	0011	0000	1000
			Branch Address			
	Branch on overflow	2/4/2	1110	0011	0010	0010
			Branch Address			
	Branch if accumulator = 0	2/4/2	1110	0011	1000	1000
			Branch Address			
BIT	Test bit	1/1	0100	BITx	IADD	RESS
BITT	Test bit specified by TREG	1/1	0110	1111	IADD	RESS
BLDD†	Block move from data memory to data memory source immediate	2/3	1010	1000	IADD	RESS
			Branch Address			
	Block move from data memory to data memory destination immediate	2/3	1010	1001	IADD	RESS
			Branch Address			
BLPD	Block move from program memory to data memory	2/3	1010	0101	IADD	RESS
			Branch Address			
CALA	Call subroutine indirect	1/4	1011	1110	0011	0000
CALL	Call subroutine	2/4	0111	1010	IADD	RESS
			Routine Address			
CC	Conditional call subroutine	2/4/2	1110	10TP	ZLVC	ZLVC
			Routine Address			
CLRC	Configure block as data memory	1/1	1011	1110	0100	0100
	Enable interrupt	1/1	1011	1110	0100	0000
	Reset carry bit	1/1	1011	1110	0100	1110
	Reset overflow mode	1/1	1011	1110	0100	0010
	Reset sign-extension mode	1/1	1011	1110	0100	0110
	Reset test/control flag	1/1	1011	1110	0100	1010
	Reset external flag	1/1	1011	1110	0100	1100
CMPL	Complement accumulator	1/1	1011	1110	0000	0001
CMPR	Compare auxiliary register with auxiliary register AR0	1/1	1011	1111	0100	01CM
DMOV	Data move in data memory	1/1	0111	0111	IADD	RESS
IDLE	Idle until interrupt	1/1	1011	1110	0010	0010
IN	Input data from port	2/2	1010	1111	IADD	RESS
			16BIT	I/O	PORT	ADRS
INTR	Software-interrupt	1/4	1011	1110	011K	KKKK
LACC	Load accumulator with shift	1/1	0001	SHFT	IADD	RESS
	Load accumulator long immediate with shift	2/2	1011	1111	1000	SHFT
			16-Bit Constant			
	Zero low accumulator and load high accumulator	1/1	0110	1010	IADD	RESS

† In ’C2xx devices, the BLDD instruction does not work with memory-mapped registers IMR, IFR, and GREG.

instruction set summary (continued)

Table 16. TMS320C2xx Instruction Set Summary (Continued)

C2xx MNEMONIC	DESCRIPTION	WORDS/ CYCLES	OPCODE			
			MSB			LSB
LACL	Load accumulator immediate short	1/1	1011	1001	KKKK	KKKK
	Zero accumulator	1/1	1011	1001	0000	0000
	Zero low accumulator and load high accumulator	1/1	0110	1010	IADD	RESS
	Zero low accumulator and load low accumulator with no sign extension	1/1	0110	1001	IADD	RESS
LACT	Load accumulator with shift specified by T register	1/1	0110	1011	IADD	RESS
LAR	Load auxiliary register	1/2	0000	0ARx	IADD	RESS
	Load auxiliary register short immediate	1/2	1011	0ARx	KKKK	KKKK
	Load auxiliary register long immediate	2/2	1011	1111	0000	1ARx
			16-Bit Constant			
LDP	Load data-memory page pointer	1/2	0000	1101	IADD	RESS
	Load data-memory page pointer immediate	1/2	1011	110P	AGEP	OINT
LPH	Load high-P register	1/1	0111	0101	IADD	RESS
LST	Load status register ST0	1/2	0000	1110	IADD	RESS
	Load status register ST1	1/2	0000	1111	IADD	RESS
LT	Load TREG	1/1	0111	0011	IADD	RESS
LTA	Load TREG and accumulate previous product	1/1	0111	0000	IADD	RESS
LTD	Load TREG, accumulate previous product, and move data	1/1	0111	0010	IADD	RESS
LTP	Load TREG and store P register in accumulator	1/1	0111	0001	IADD	RESS
LTS	Load TREG and subtract previous product	1/1	0111	0100	IADD	RESS
MAC	Multiply and accumulate	2/3	1010	0010	IADD	RESS
			16-Bit Constant			
MACD	Multiply and accumulate with data move	2/3	1010	0011	IADD	RESS
			16-Bit Constant			
MAR	Load auxiliary register pointer	1/1	1000	1011	1000	1ARx
	Modify auxiliary register	1/1	1000	1011	IADD	RESS
MPY	Multiply (with TREG, store product in P register)	1/1	0101	0100	IADD	RESS
	Multiply immediate	1/1	110C	KKKK	KKKK	KKKK
MPYA	Multiply and accumulate previous product	1/1	0101	0000	IADD	RESS
MPYS	Multiply and subtract previous product	1/1	0101	0001	IADD	RESS
MPYU	Multiply unsigned	1/1	0101	0101	IADD	RESS
NEG	Negate accumulator	1/1	1011	1110	0000	0010
NMI	Nonmaskable interrupt	1/4	1011	1110	0101	0010
NOP	No operation	1/1	1000	1011	0000	0000
NORM	Normalize contents of accumulator	1/1	1010	0000	IADD	RESS
OR	OR with accumulator	1/1	0110	1101	IADD	RESS
	OR immediate with accumulator with shift	2/2	1011	1111	1100	SHFT
			16-Bit Constant			
	OR immediate with accumulator with shift of 16	2/2	1011	1110	1000	0010
			16-Bit Constant			
OUT	Output data to port	2/3	0000 16BIT	1100 I/O	IADD PORT	RESS ADRS
PAC	Load accumulator with P register	1/1	1011	1110	0000	0011

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instruction set summary (continued)

Table 16. TMS320C2xx Instruction Set Summary (Continued)

C2xx MNEMONIC	DESCRIPTION	WORDS/ CYCLES	OPCODE			
			MSB			LSB
POP	Pop top of stack to low accumulator	1/1	1011	1110	0011	0010
POPD	Pop top of stack to data memory	1/1	1000	1010	IADD	RESS
PSHD	Push data-memory value onto stack	1/1	0111	0110	IADD	RESS
PUSH	Push low accumulator onto stack	1/1	1011	1110	0011	1100
RET	Return from subroutine	1/4	1110	1111	0000	0000
RETC	Conditional return from subroutine	1/4/2	1110	11TP	ZLVC	ZLVC
ROL	Rotate accumulator left	1/1	1011	1110	0000	1100
ROR	Rotate accumulator right	1/1	1011	1110	0000	1101
RPT	Repeat instruction as specified by data-memory value	1/1	0000	1011	IADD	RESS
	Repeat instruction as specified by immediate value	1/1	1011	1011	KKKK	KKKK
SACH	Store high accumulator with shift	1/1	1001	1SHF	IADD	RESS
SACL	Store low accumulator with shift	1/1	1001	0SHF	IADD	RESS
SAR	Store auxiliary register	1/1	1000	0ARx	IADD	RESS
SBRK	Subtract from auxiliary register short immediate	1/1	0111	1100	KKKK	KKKK
SETC	Set carry bit	1/1	1011	1110	0100	1111
	Configure block as program memory	1/1	1011	1110	0100	0101
	Disable interrupt	1/1	1011	1110	0100	0001
	Set overflow mode	1/1	1011	1110	0100	0011
	Set test/control flag	1/1	1011	1110	0100	1011
	Set external flag XF	1/1	1011	1110	0100	1101
	Set sign-extension mode	1/1	1011	1110	0100	0111
SFL	Shift accumulator left	1/1	1011	1110	0000	1001
SFR	Shift accumulator right	1/1	1011	1110	0000	1010
SPAC	Subtract P register from accumulator	1/1	1011	1110	0000	0101
SPH	Store high-P register	1/1	1000	1101	IADD	RESS
SPL	Store low-P register	1/1	1000	1100	IADD	RESS
SPM	Set P register output shift mode	1/1	1011	1111	IADD	RESS
SQRA	Square and accumulate	1/1	0101	0010	IADD	RESS
SQRS	Square and subtract previous product from accumulator	1/1	0101	0011	IADD	RESS
SST	Store status register ST0	1/1	1000	1110	IADD	RESS
	Store status register ST1	1/1	1000	1111	IADD	RESS
SPLK	Store long immediate to data memory	2/2	1010	1110	IADD	RESS
			16-Bit Constant			
SUB	Subtract from accumulator long immediate with shift	2/2	1011	1111	1010	SHFT
			16-Bit Constant			
	Subtract from accumulator with shift	1/1	0011	SHFT	IADD	RESS
	Subtract from high accumulator	1/1	0110	0101	IADD	RESS
	Subtract from accumulator short immediate	1/1	1011	1010	KKKK	KKKK

instruction set summary (continued)

Table 16. TMS320C2xx Instruction Set Summary (Continued)

C2xx MNEMONIC	DESCRIPTION	WORDS/ CYCLES	OPCODE			
			MSB			LSB
SUBB	Subtract from accumulator with borrow	1/1	0110	0100	IADD	RESS
SUBC	Conditional subtract	1/1	0000	1010	IADD	RESS
SUBS	Subtract from low accumulator with sign extension suppressed	1/1	0110	0110	IADD	RESS
SUBT	Subtract from accumulator with shift specified by TREG	1/1	0110	0111	IADD	RESS
TBLR	Table read	1/3	1010	0110	IADD	RESS
TBLW	Table write	1/3	1010	0111	IADD	RESS
TRAP	Software interrupt	1/4	1011	1110	0101	0001
XOR	Exclusive-OR with accumulator	1/1	0110	1100	IADD	RESS
	Exclusive-OR immediate with accumulator with shift	2/2	1011	1111	1101	SHFT
			16-Bit Constant			
	Exclusive-OR immediate with accumulator with shift of 16	2/2	1011	1110	1000	0011
			16-Bit Constant			
ZALR	Zero low accumulator and load high accumulator with rounding	1/1	0110	1000	IADD	RESS

development support

Texas Instruments (TI™) offers an extensive line of development tools for the ’C2xx generation of DSPs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of ’C2xx-based applications:

Software Development Tools:
Assembler/Linker
Simulator
Optimizing ANSI C Compiler
Application Algorithms
C/Assembly Debugger and Code Profiler

Hardware Development Tools:
Emulator XDS510 (supports ’C2xx multiprocessor system debug)

The *TMS320 Family Development Support Reference Guide* (literature number SPRU011) contains information about development support products for all TMS320 family member devices, including documentation. Refer to this document for further information about TMS320 documentation or any other TMS320 support products from Texas Instruments. There is also an additional document, the *TMS320 Third-Party Support Reference Guide* (literature number SPRU052), which contains information about TMS320-related products from other companies in the industry. To receive copies of TMS320 literature, contact the Literature Response Center at 800/477-8924.

See Table 17 for complete listings of development support tools for the ’C2xx. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

development support (continued)

Table 17. TMS320C2xx Development Support Tools

DEVELOPMENT TOOL	PLATFORM	PART NUMBER
Software		
Compiler/Assembler/Linker	SPARC™, HP™	TMDS3242555-08
Compiler/Assembler/Linker	PC-DOS™, OS/2™	TMDS3242855-02
Assembler/Linker	PC-DOS, OS/2	TMDS3242850-02
Simulator	PC-DOS, WIN™	TMDS3245851-02
Simulator	SPARC	TMDS3245551-09
Digital Filter Design Package	PC-DOS	DFDP
Debugger/Emulation Software	PC-DOS, OS/2, WIN	TMDS3240120
Debugger/Emulation Software	SPARC	TMDS3240620
Code Composer™ Debugger	Windows™	CCMSP5XWIN
Hardware		
C2xx Evaluation Module	PC-DOS	TMDS32600XX
XDS510XL™ Emulator	PC-DOS, OS/2	TMDS00510
XDS510WS™ Emulator	SPARC	TMDS00510WS

device and development support tool nomenclature

To designate the stages in the product development cycle, Texas Instruments assigns prefixes to the part numbers of all TMS320 devices and support tools. Each TMS320 member has one of three prefixes: TMX, TMP, and TMS. Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS). This development flow is defined below.

Device Development Evolutionary Flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully-qualified production device

Support Tool Development Evolutionary Flow:

TMDX Development support product that has not yet completed Texas Instruments internal qualification testing

TMDS Fully qualified development support product

TMX and TMP devices and TMDX development support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development support tools have been fully characterized, and the quality and reliability of the device have been fully demonstrated. Texas Instruments standard warranty applies.

Predictions show that prototype devices (TMX or TMP) will have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate is still undefined. Only qualified production devices are to be used.

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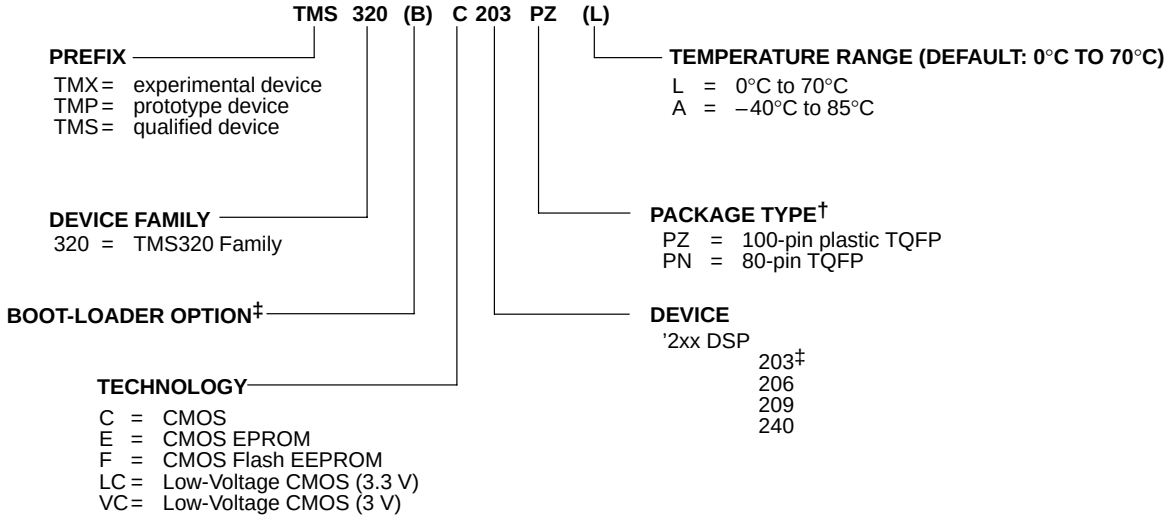
device and development support tool nomenclature (continued)

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZ or PN) and temperature range (for example, L). The following figures provide a legend for reading the complete device name for any TMS320 family member.



† TQFP = Thin Quad Flat Package
‡ The TMS320C203 is a boot-loader device without the B option.

Figure 6. TMS320C2xx Device Nomenclature

documentation support

Extensive documentation supports all of the TMS320 family generations of devices from product announcement through applications development. The types of documentation available include: data sheets, such as this document, with design specifications; complete user's guides for all devices and development support tools; and hardware and software applications.

For general background information on DSPs and TI devices, see the three-volume publication *Digital Signal Processing Applications With the TMS320 Family* (literature numbers SPRA012, SPRA016, and SPRA017). Also available is the *Calculation of TMS320C2xx Power Dissipation* application report (literature number SPRA088).

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320 newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320 customers on product information. The TMS320 DSP bulletin board service (BBS) provides access to information pertaining to the TMS320 family, including documentation, source code and object code for many DSP algorithms and utilities. The BBS can be reached at 281/274-2323.

Information regarding TI DSP products is also available on the Worldwide Web at http://www.ti.com uniform resource locator (URL).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) ('320C2xx only)†

Supply voltage range, V_{DD} (see Note 1) . . . . . – 0.3 V to 7 V
Input voltage range . . . . . – 0.3 V to 7 V
Output voltage range . . . . . – 0.3 V to 7 V
Operating free-air temperature range, T_A . . . . . – 40°C to 85°C
Storage temperature range, T_{stg} . . . . . – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions for TMS320C2xx @ 5 V

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	5-V operation	4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	CLKIN/X2	3		V_{DD} + 0.3	V
		$\overline{RS}$, CLKR, CLKX, RX	2.3			
		All other inputs	2.2		V_{DD} + 0.3	
V_{IL}	Low-level input voltage	CLKIN/X2	– 0.3		0.7	V
		$\overline{RS}$, CLKR, CLKX, RX			0.8	
		All other inputs	– 0.3		0.8	
I_{OH}	High-level output current				– 300	µA
I_{OL}	Low-level output current				2	mA
T_A	Operating free-air temperature		– 40		85	°C

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted) ('320LC2xx only)†

Supply voltage range, V_{DD} (see Note 1) . . . . . – 0.3 V to 5 V
Input voltage range . . . . . – 0.3 V to 5 V
Output voltage range . . . . . – 0.3 V to 5 V
Operating free-air temperature range, T_A . . . . . – 40°C to 85°C
Storage temperature range, T_{stg} . . . . . – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions for TMS320LC2xx @ 3.3 V

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3.3-V operation	3	3.3	3.6	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	CLKIN/X2‡	2.5		V_{DD} + 0.3	V
		$\overline{RS}$, CLKR, CLKX, RX	2			
		All other inputs	1.8		V_{DD} + 0.3	
V_{IL}	Low-level input voltage	CLKIN/X2, $\overline{RS}$, READY, $\overline{HOLD}$/$\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{NMI}$	– 0.3		0.4	V
		All other inputs	– 0.3		0.4	
I_{OH}	High-level output current				– 300	µA
I_{OL}	Low-level output current				2	mA
T_A	Operating free-air temperature		– 40		85	°C

‡ Values derived from characterization data and not tested

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature for TMS320C2xx @ 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	5-V operation, I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage	5-V operation, I_{OL} = MAX			0.7	V
I_I	Input current	$V_I = V_{DD}$ or 0 V	– 10		10	µA
I_{OZ}	Output current, high-impedance state (off-state)	$V_O = V_{DD}$ or 0 V			± 5	µA
I_{DD}	Supply current, core CPU	5-V operation, 80 MHz		76		mA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature for TMS320LC2xx @ 3.3 V (TTL levels)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	3.3-V operation, I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage	3.3-V operation, I_{OL} = MAX			0.4	V
I_I	Input current	$V_I = V_{DD}$ or 0 V	– 10		10	µA
I_{OZ}	Output current, high-impedance state (off-state)	$V_O = V_{DD}$ or 0 V			± 5	µA
I_{DD}	Supply current, core CPU	3.3-V operation, 40 MHz		22		mA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF
I_i	CLKIN input current	$V_i = V_{DD}$ or 0 V	– 350		350	µA

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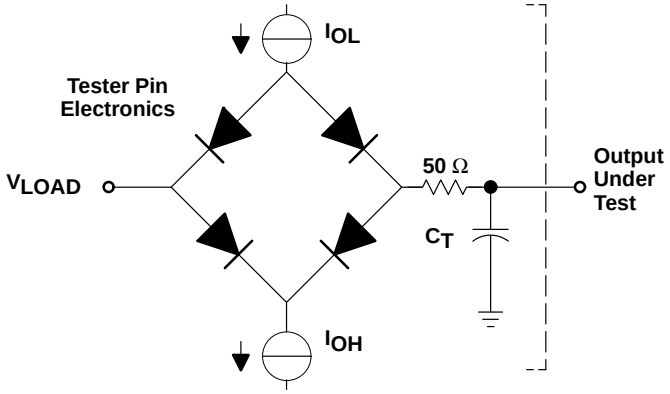
PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{LOAD} = 1.5 V
C_T = 60-pF typical load-circuit capacitance

Figure 7. Test Load Circuit

signal-transition levels

The data in this section is shown for both the 5-V version (’C2xx) and the 3.3-V version (’LC2xx). In each case, the 5-V data is shown followed by the 3.3-V data in parentheses. Note that some of the signals use different reference voltages, see the recommended operating conditions tables for 5-V and 3.3-V devices. TTL-output levels are driven to a minimum logic-high level of 2.4 V (2.4 V) and to a maximum logic-low level of 0.7 V (0.4 V).

Figure 8 shows the TTL-level outputs.

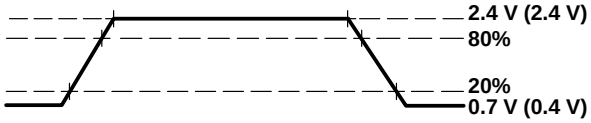


Figure 8. TTL-Level Outputs

TTL-output transition times are specified as follows:

- For a *high-to-low transition*, the level at which the output is said to be no longer high is below 80% of the total voltage range and lower and the level at which the output is said to be low is 20% of the total voltage range and lower.
- For a *low-to-high transition*, the level at which the output is said to be no longer low is 20% of the total voltage range and higher and the level at which the output is said to be high is 80% of the total voltage range and higher.

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

Figure 9 shows the TTL-level inputs.

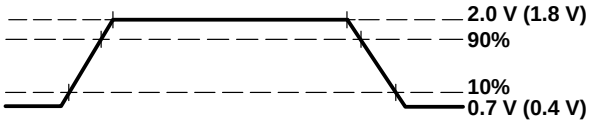


Figure 9. TTL-Level Inputs

TTL-compatible input transition times are specified as follows:

- For a *high-to-low transition* on an input signal, the level at which the input is said to be no longer high is 90% of the total voltage range and lower and the level at which the input is said to be low is 10% of the total voltage range and lower.
- For a *low-to-high transition* on an input signal, the level at which the input is said to be no longer low is 10% of the total voltage range and higher and the level at which the input is said to be high is 90% of the total voltage range and higher.

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols used are created in accordance with JEDEC Standard 100-A. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

A	Address or A[15:0]
CI	CLKIN/X2
CO	CLKOUT1
D	Data or D[15:0]
FS	FSX
H	$\overline{\text{HOLD}}$ ('203 only)
HA	$\overline{\text{HOLDA}}$ ('203 only)
IN	INTN; $\overline{\text{BIO}}$, $\overline{\text{INT1}}$–$\overline{\text{INT3}}$, $\overline{\text{NMI}}$
MS	Memory strobe pins $\overline{\text{IS}}$, $\overline{\text{DS}}$, or $\overline{\text{PS}}$
R	READY
RD	Read cycle or $\overline{\text{RD}}$
RS	RESET pins RS or $\overline{\text{RS}}$
S	$\overline{\text{STRB}}$
SCK	Serial-port clock
W	Write cycle or $\overline{\text{WE}}$

Lowercase subscripts and their meanings are:

a	access time
c	cycle time (period)
d	delay time
dis	disable time
en	enable time
f	fall time
h	hold time
r	rise time
su	setup time
t	transition time
v	valid time
w	pulse duration (width)

The following letters and symbols and their meanings are:

H	High
L	Low
V	Valid
Z	High impedance
X	Unknown, changing, or don't care level

general notes on timing parameters

All output signals from the TMS320C2xx devices (including CLKOUT1) are derived from an internal clock such that all output transitions for a given half cycle occur with a minimum of skewing relative to each other.

The signal combinations shown in the following timing diagrams may not necessarily represent actual cycles. For actual cycle examples, refer to the appropriate cycle description section of this data sheet.

CLOCK CHARACTERISTICS AND TIMING

TMS320C209 clock options

PARAMETER	CLKMOD
Internal divide-by-two with external crystal	0
PLL multiply-by-two	1

TMS320C203 and TMS320LC203 clock options

PARAMETER	DIV2	DIV1
Internal divide-by-two with external crystal or external oscillator	0	0
PLL multiply-by-one	0	1
PLL multiply-by-two	1	0
PLL multiply-by-four	1	1

internal divide-by-two clock option with external crystal

The internal oscillator is enabled by connecting a crystal across X1 and CLKIN/X2. The frequency of CLKOUT1 is one-half the crystal's oscillating frequency. The crystal should be in either fundamental or overtone operation and parallel resonant, with an effective series resistance of 30 Ω and a power dissipation of 1 mW; it should be specified at a load capacitance of 20 pF. Note that overtone crystals require an additional tuned-LC circuit. Figure 10 shows an external crystal (fundamental frequency) connected to the on-chip oscillator.

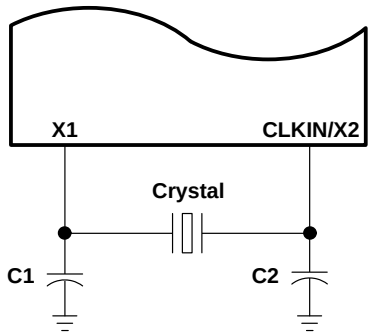


Figure 10. Internal Clock Option

timing at V_{DD} = 5 V with the PLL circuit disabled, divide-by-two mode for TMS320C2xx†

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_X	Input clock frequency	T_A = – 40°C to 85°C, 5 V	0†		80 57.14 40.96	MHz

† This device is implemented in static logic and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz, but is tested at f_X = 6.7 MHz to meet device test time requirements.

switching characteristics over recommended operating conditions for TMS320C2xx (see Figure 11)

PARAMETER		'320C2xx-40			'320C2xx-57			'320C2xx-80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT1	48.8	$2t_{c(CI)}$	‡	35	$2t_{c(CI)}$	‡	25	$2t_{c(CI)}$	‡	ns
$t_{d(CIH-CO)}$	Delay time, CLKIN high to CLKOUT1 high/low	1	11	20	1	11	20	1	9	18	ns
$t_{f(CO)}$	Fall time, CLKOUT1		5§			5			4		ns
$t_{r(CO)}$	Rise time, CLKOUT1		5§			5			4		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H – 3	H	H + 1	H – 3	H	H + 1	H – 3	H	H + 1	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H – 1	H	H + 3	H – 1	H	H + 3	H – 1	H	H + 3	ns

‡ This device is implemented in static logic and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz, but is tested at $t_{c(CI)}$ = 300 ns to meet device test time requirements.
§ Values derived from characterization data and not tested

timing requirements over recommended operating conditions for TMS320C2xx (see Figure 11)

		'320C2xx-40		'320C2xx-57		'320C2xx-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(CI)}$	Cycle time, CLKIN	25	¶	17.5	¶	12.5	¶	ns
$t_{f(CI)}$	Fall time, CLKIN§		5		5		4	ns
$t_{r(CI)}$	Rise time, CLKIN§		5		5		4	ns
$t_{w(CIL)}$	Pulse duration, CLKIN low	11	¶	8	¶	5	¶	ns
$t_{w(CIH)}$	Pulse duration, CLKIN high	11	¶	8	¶	5	¶	ns

§ Values derived from characterization data and not tested
¶ This device is implemented in static logic and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz, but is tested at a minimum $t_{c(CI)}$ = 150 ns to meet device test time requirements.

ADVANCE INFORMATION

timing at V_{DD} = 3.3 V with the PLL circuit disabled, divide-by-two mode for TMS320LC2xx†

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_X	Input clock frequency	T_A = –40°C to 85°C, 3.3 V	0†	40	MHz

† This device is implemented in static logic and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz, but is tested at f_X = 6.7 MHz to meet device test time requirements.

switching characteristics over recommended operating conditions for TMS320LC2xx (see Figure 11)

PARAMETER		’320LC2xx-40			UNIT
		MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT1	50	$2t_{c(CI)}$	‡	ns
$t_{d(CIH-CO)}$	Delay time, CLKIN high to CLKOUT1 high/low	1	11	20	ns
$t_{f(CO)}$	Fall time, CLKOUT1§		5		ns
$t_{r(CO)}$	Rise time, CLKOUT1§		5		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H – 3	H	H + 1	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H – 1	H	H + 3	ns

‡ This device is implemented in static logic and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz, but is tested at $t_{c(CI)}$ = 300 ns to meet device test time requirements.
§ Values derived from characterization data and not tested

timing requirements over recommended operating conditions for TMS320LC2xx (see Figure 11)

		’320LC2xx-40		UNIT
		MIN	MAX	
$t_{c(CI)}$	Cycle time, CLKIN	25		ns
$t_{f(CI)}$	Fall time, CLKIN§		5	ns
$t_{r(CI)}$	Rise time, CLKIN§		5	ns
$t_{w(CIL)}$	Pulse duration, CLKIN low§	9		ns
$t_{w(CIH)}$	Pulse duration, CLKIN high§	9		ns

§ Values derived from characterization data and not tested

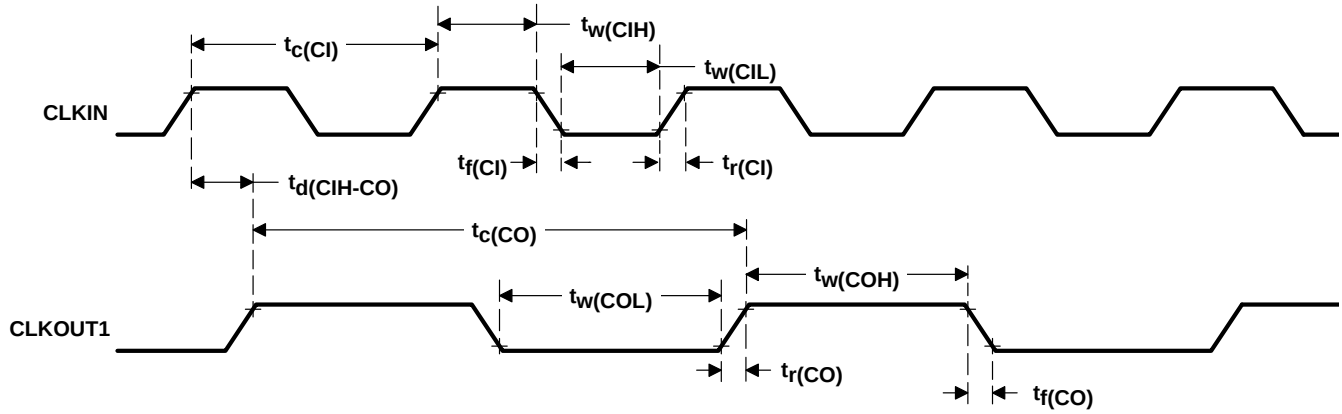


Figure 11. CLKIN-to-CLKOUT1 Timing Without PLL (using ÷2 clock option)

ADVANCE INFORMATION

timing @ V_{DD} = 5 V with the PLL circuit enabled, multiply-by-two mode for TMS320C2xx

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_X	Input clock frequency	T_A = – 40°C to 85°C, 5 V	5	20	MHz

switching characteristics over recommended operating conditions for TMS320C2xx @ 5 V (see Figure 12)

PARAMETER		’320C2xx-40			’320C2xx-57			’320C2xx-80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT1	50		100	35		75	25		55	ns
$t_{d(CIH-CO)}$	Delay time, CLKIN high to CLKOUT1 high/low	3	8	18	3	8	18	1	8	16	ns
$t_{f(CO)}$	Fall time, CLKOUT1†		5			5			4		ns
$t_{r(CO)}$	Rise time, CLKOUT1†		5			5			4		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H – 3	H	H + 1	H – 3	H	H + 1	H – 3	H	H + 1	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H – 1	H	H + 3	H – 1	H	H + 3	H – 1	H	H + 3	ns
t_p	Transition time, PLL synchronized after CLKIN supplied			2500			2500			2500	cycles

† Values derived from characterization data and not tested

timing requirements over recommended operating conditions for TMS320C2xx @ 5 V (see Figure 12)

		’320C2xx-40		’320C2xx-57		’320C2xx-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(CI)}$	Cycle time, CLKIN multiply-by-one	50	100	35	75	25	75	ns
	Cycle time, CLKIN multiply-by-two	100	200	70	200	50	150	ns
$t_{f(CI)}$	Fall time, CLKIN†		4		4		4	ns
$t_{r(CI)}$	Rise time, CLKIN†		4		4		4	ns
$t_{w(CIL)}$	Pulse duration, CLKIN low	16	95	14	95	11	95	ns
$t_{w(CIH)}$	Pulse duration, CLKIN high	16	95	14	95	11	95	ns

† Values derived from characterization data and not tested

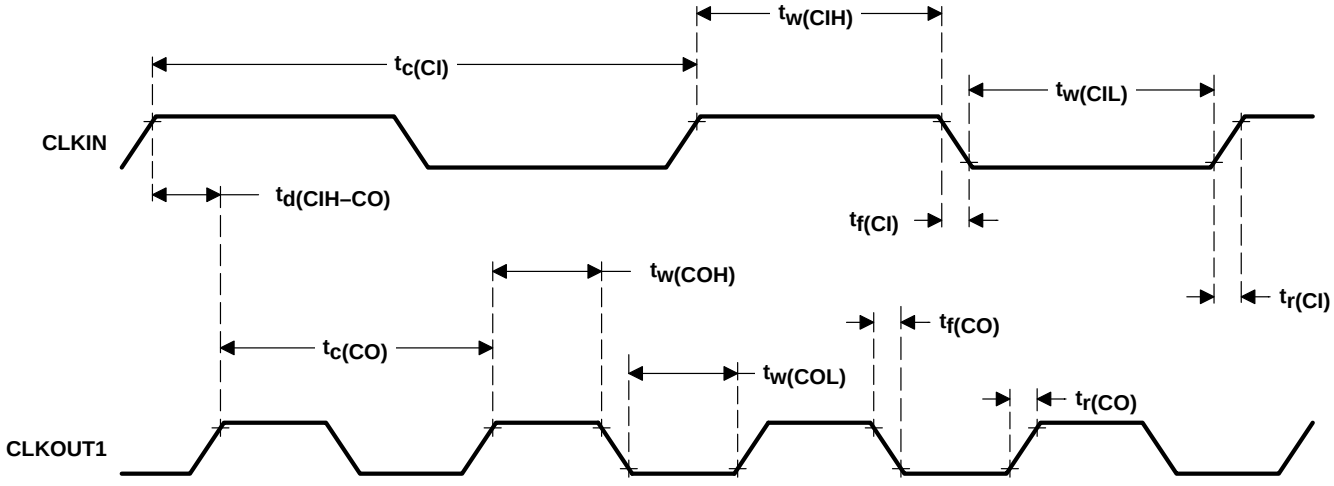


Figure 12. CLKIN-to-CLKOUT1 Timing With PLL (using ×2 clock option)

timing @ V_{DD} = 3.3 V with the PLL circuit enabled, multiply-by-two mode for TMS320LC2xx

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_X	Input clock frequency	T_A = – 40°C to 85°C, 3.3 V	5	10	MHz

switching characteristics over recommended operating conditions for TMS320LC2xx @ 3.3 V (see Figure 12)

PARAMETER		’320LC2xx-40			UNIT
		MIN	TYP	MAX	
$t_{c(CO)}$	Cycle time, CLKOUT1	50	$2t_{c(CI)}$	75	ns
$t_{d(CIH-CO)}$	Delay time, CLKIN high to CLKOUT1 high/low	3	8	18	ns
$t_{f(CO)}$	Fall time, CLKOUT1†		5		ns
$t_{r(CO)}$	Rise time, CLKOUT1†		5		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H – 3	H	H + 1	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H – 1	H	H + 3	ns
t_p	Transition time, PLL synchronized after CLKIN supplied			2500	cycles

† Values derived from characterization data and not tested

timing requirements over recommended operating conditions for TMS320LC2xx @ 3.3 V (see Figure 12)

		’320LC2xx-40		UNIT
		MIN	MAX	
$t_{c(CI)}$	Cycle time, CLKIN multiply-by-one	50	75	ns
	Cycle time, CLKIN multiply-by-two	100	150	ns
$t_{f(CI)}$	Fall time, CLKIN†		5	ns
$t_{r(CI)}$	Rise time, CLKIN†		5	ns
$t_{w(CIL)}$	Pulse duration, CLKIN low	15	95	ns
$t_{w(CIH)}$	Pulse duration, CLKIN high	15	95	ns

† Values derived from characterization data and not tested

ADVANCE INFORMATION

MEMORY AND PERIPHERAL INTERFACE TIMING

memory and parallel I/O interface read timing for TMS320C2xx @ 5 V

A15–A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in the timings referenced to A15–A0 except when in transition between read and write operations, where $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ pulse high [see $t_{w(NSN)}$].

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 13)

PARAMETER		'320C2xx-40 '320C2xx-57		'320C2xx-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(A)RD}$	Setup time, address valid before $\overline{RD}$ low	H – 5		H – 5		ns
$t_{h(A)RD}$	Hold time, address valid after $\overline{RD}$ high	– 6		– 6		ns
$t_{d(COL-A)}$	Delay time, address valid after CLKOUT1 low		5		4	ns
$t_{h(A)COLRD}$	Hold time, address valid after CLKOUT1 low	– 4		– 3		ns
$t_{d(CO-RD)}$	Delay time, CLKOUT1 high/low to $\overline{RD}$ low/high	– 1	6	– 1	5	ns
$t_{d(COL-S)}$	Delay time, CLKOUT1 low to $\overline{STRB}$ low/high†	0	9	0	9	ns
$t_{w(RDL)}$	Pulse duration, $\overline{RD}$ low (no wait states)	H – 3	H + 2	H – 3	H + 2	ns
$t_{w(RDH)}$	Pulse duration, $\overline{RD}$ high	H – 4	H + 3	H – 3	H + 3	ns

† Values derived from characterization data and not tested

timing requirements over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 13)

		'320C2xx-40 '320C2xx-57		'320C2xx-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time, read data from address valid		2H – 15		2H – 13	ns
$t_{su(D)RD}$	Setup time, data read before $\overline{RD}$ high	13		13		ns
$t_{h(D)RD}$	Hold time, data read from $\overline{RD}$ high	– 2		– 2		ns
$t_{h(D)A}$	Hold time, read data from address invalid	0		0		ns
$t_{su(DCOL)RD}$	Setup time, data read before CLKOUT1 low	9		10		ns
$t_{h(DCOL)RD}$	Hold time, data read from CLKOUT1 low	– 1		– 1		ns
$t_{a(RD)}$	Access time, read data after $\overline{RD}$ low		H – 12		H – 13	ns
$t_{a(S)}$	Access time, read data from $\overline{STRB}$ low†				8	ns

† Values derived from characterization data and not tested

ADVANCE INFORMATION

memory and parallel I/O interface read timing for TMS320LC2xx @ 3.3 V

A15–A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in the timings referenced to A15–A0 except when in transition between read and write operations, where $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ pulse high [see $t_{w(NSN)}$].

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 13)

PARAMETER		'320LC2xx-40		UNIT
		MIN	MAX	
$t_{su(A)RD}$	Setup time, address valid before $\overline{RD}$ low	H – 7		ns
$t_{h(A)RD}$	Hold time, address valid after $\overline{RD}$ high	– 8		ns
$t_{d(COL-A)}$	Delay time, address valid after CLKOUT1 low		9	ns
$t_{h(A)COLRD}$	Hold time, address valid after CLKOUT1 low	– 4		ns
$t_{d(CO-RD)}$	Delay time, CLKOUT1 high/low to $\overline{RD}$ low/high	– 1	7	ns
$t_{d(COL-S)}$	Delay time, CLKOUT1 low to $\overline{STRB}$ low/high†	3	16	ns
$t_{w(RDL)}$	Pulse duration, $\overline{RD}$ low (no wait states)	H – 3	H + 2	ns
$t_{w(RDH)}$	Pulse duration, $\overline{RD}$ high	H – 4	H + 2	ns

† Values derived from characterization data and not tested

timing requirements over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 13)

		'320LC2xx-40		UNIT
		MIN	MAX	
$t_{a(A)}$	Access time, read data from address valid		2H – 23	ns
$t_{su(D)RD}$	Setup time, data read before $\overline{RD}$ high	22		ns
$t_{h(D)RD}$	Hold time, data read from $\overline{RD}$ high	– 2		ns
$t_{h(D)A}$	Hold time, read data from address invalid	0		ns
$t_{su(DCOL)RD}$	Setup time, data read before CLKOUT1 low	17		ns
$t_{h(DCOL)RD}$	Hold time, data read from CLKOUT1 low	– 1		ns
$t_{a(RD)}$	Access time, read data after $\overline{RD}$ low		H – 20	ns

ADVANCE INFORMATION

MEMORY AND PERIPHERAL INTERFACE TIMING (CONTINUED)

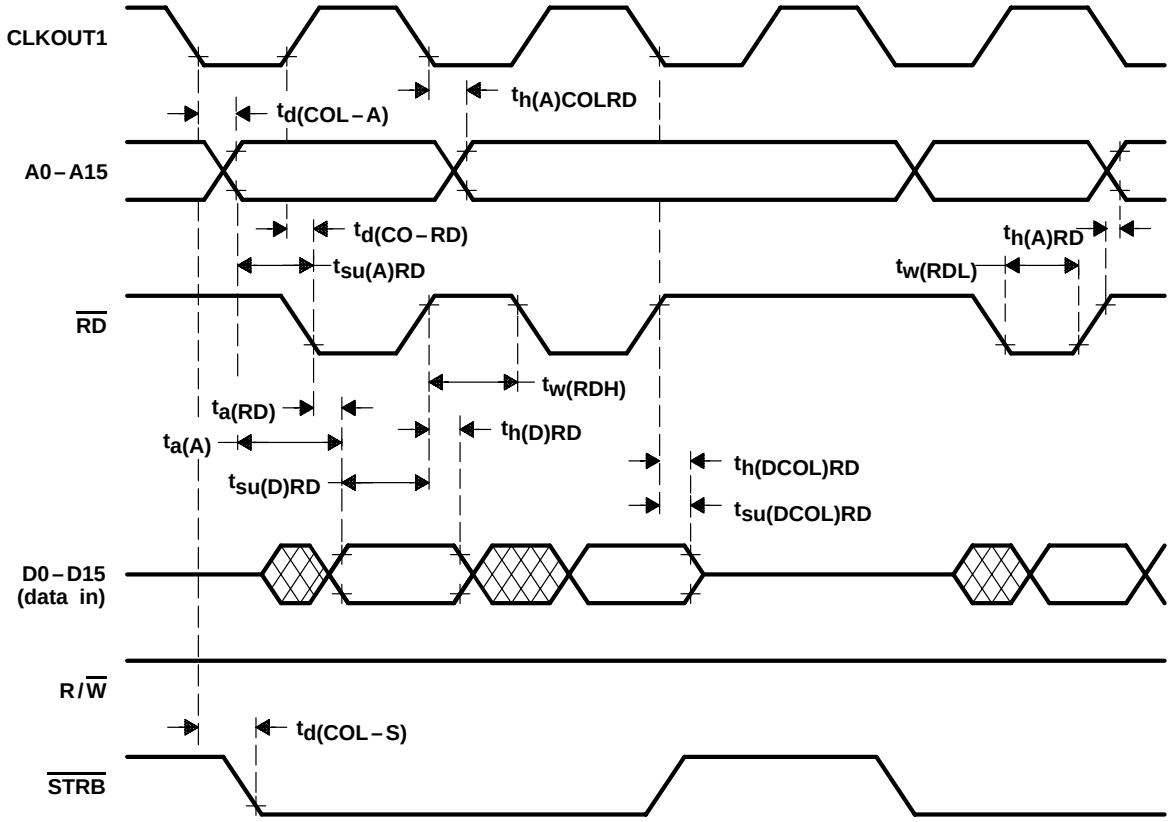


Figure 13. Memory Interface Read Timing

ADVANCE INFORMATION

memory and parallel I/O interface write timing for TMS320C2xx @ 5 V

A15–A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in the timings referenced to A15–A0 except when in transition between read and write operations, where $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ pulse high [see $t_{w(NSN)}$].

switching characteristics over recommended operating conditions @ 5 V [H = 0.5$t_{c(CO)}$] (see Figure 14)

PARAMETER		'320C2xx-40 '320C2xx-57		'320C2xx-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(A)W}$	Setup time, address valid before $\overline{WE}$ low	H – 7		H – 6		ns
$t_{h(A)W}$	Hold time, address valid after $\overline{WE}$ high	H – 10		H – 8		ns
$t_{su(A)CO}$	Setup time, address valid before CLKOUT1 low	H – 9		H – 8		ns
$t_{h(A)COLW}$	Hold time, address valid after CLKOUT1 low	H – 3		H – 5		ns
$t_{w(NSN)}$	Pulse duration, $\overline{IS}$, $\overline{DS}$, $\overline{PS}$ inactive high†	H – 9		H – 8		ns
$t_{w(WL)}$	Pulse duration, $\overline{WE}$ low (no wait states)	2H – 3	2H + 2	2H – 4	2H + 2	ns
$t_{w(WH)}$	Pulse duration, $\overline{WE}$ high	2H – 2		2H – 2		ns
$t_{d(COL-W)}$	Delay time, CLKOUT1 low to $\overline{WE}$ low/high	– 1	6	– 1	4	ns
$t_{d(RDW)}$	Delay time, $\overline{RD}$ high to $\overline{WE}$ low	2H – 8		2H – 7		ns
$t_{d(WRD)}$	Delay time, $\overline{WE}$ high to $\overline{RD}$ low	3H – 8		3H – 8		ns
$t_{su(D)W}$	Setup time, write data valid before $\overline{WE}$ high	2H – 15	2H†	2H – 14	2H†	ns
$t_{h(D)W}$	Hold time, write data valid after $\overline{WE}$ high	H – 4	H + 7†	H – 3	H + 7†	ns
$t_{su(DCOL)W}$	Setup time, write data valid before CLKOUT1 low	2H – 20	2H†	2H – 20	2H†	ns
$t_{h(DCOL)W}$	Hold time, write data valid after CLKOUT1 low	H – 4	H + 11†	H – 5	H + 11†	ns
$t_{en(D)W}$	Enable time, $\overline{WE}$ to data bus driven†	– 4		– 3		ns

† Values derived from characterization data and not tested

ADVANCE INFORMATION

memory and parallel I/O interface write timing for TMS320LC2xx @ 3.3 V

A15–A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in the timings referenced to A15–A0 except when in transition between read and write operations, where $\overline{PS}$, $\overline{DS}$, and $\overline{IS}$ pulse high [see $t_{w(NSN)}$].

switching characteristics over recommended operating conditions @ 3.3 V [H = 0.5$t_{c(CO)}$] (see Figure 14)

PARAMETER		'320LC2xx-40		UNIT
		MIN	MAX	
$t_{su(A)W}$	Setup time, address valid before $\overline{WE}$ low	H – 5		ns
$t_{h(A)W}$	Hold time, address valid before $\overline{WE}$ high	H – 10		ns
$t_{su(A)CO}$	Setup time, address valid before CLKOUT1 low	H – 9		ns
$t_{h(A)COLW}$	Hold time, address valid after CLKOUT1 low	H – 5		ns
$t_{w(NSN)}$	Pulse duration, $\overline{IS}$, $\overline{DS}$, $\overline{PS}$ inactive high†	H – 9		ns
$t_{w(WL)}$	Pulse duration, $\overline{WE}$ low (no wait states)	2H – 3	2H + 1	ns
$t_{w(WH)}$	Pulse duration, $\overline{WE}$ high	2H – 2		ns
$t_{d(COL-W)}$	Delay time, CLKOUT1 low to $\overline{WE}$ low/high	– 1	6	ns
$t_{d(RDW)}$	Delay time, $\overline{RD}$ high to $\overline{WE}$ low	2H – 8		ns
$t_{d(WRD)}$	Delay time, $\overline{WE}$ high to $\overline{RD}$ low	3H – 8		ns
$t_{su(D)W}$	Setup time, write data valid before $\overline{WE}$ high	2H – 15	2H†	ns
$t_{h(D)W}$	Hold time, write data valid after $\overline{WE}$ high	H – 4	H + 7†	ns
$t_{su(DCOL)W}$	Setup time, write data valid before CLKOUT1 low	2H – 20	2H†	ns
$t_{h(DCOL)W}$	Hold time, write data valid after CLKOUT1 low	H – 4	H + 11†	ns
$t_{en(D)W}$	Enable time, $\overline{WE}$ to data bus driven†	– 4		ns

† Values derived from characterization data and not tested

ADVANCE INFORMATION

MEMORY AND PERIPHERAL INTERFACE TIMING (CONTINUED)

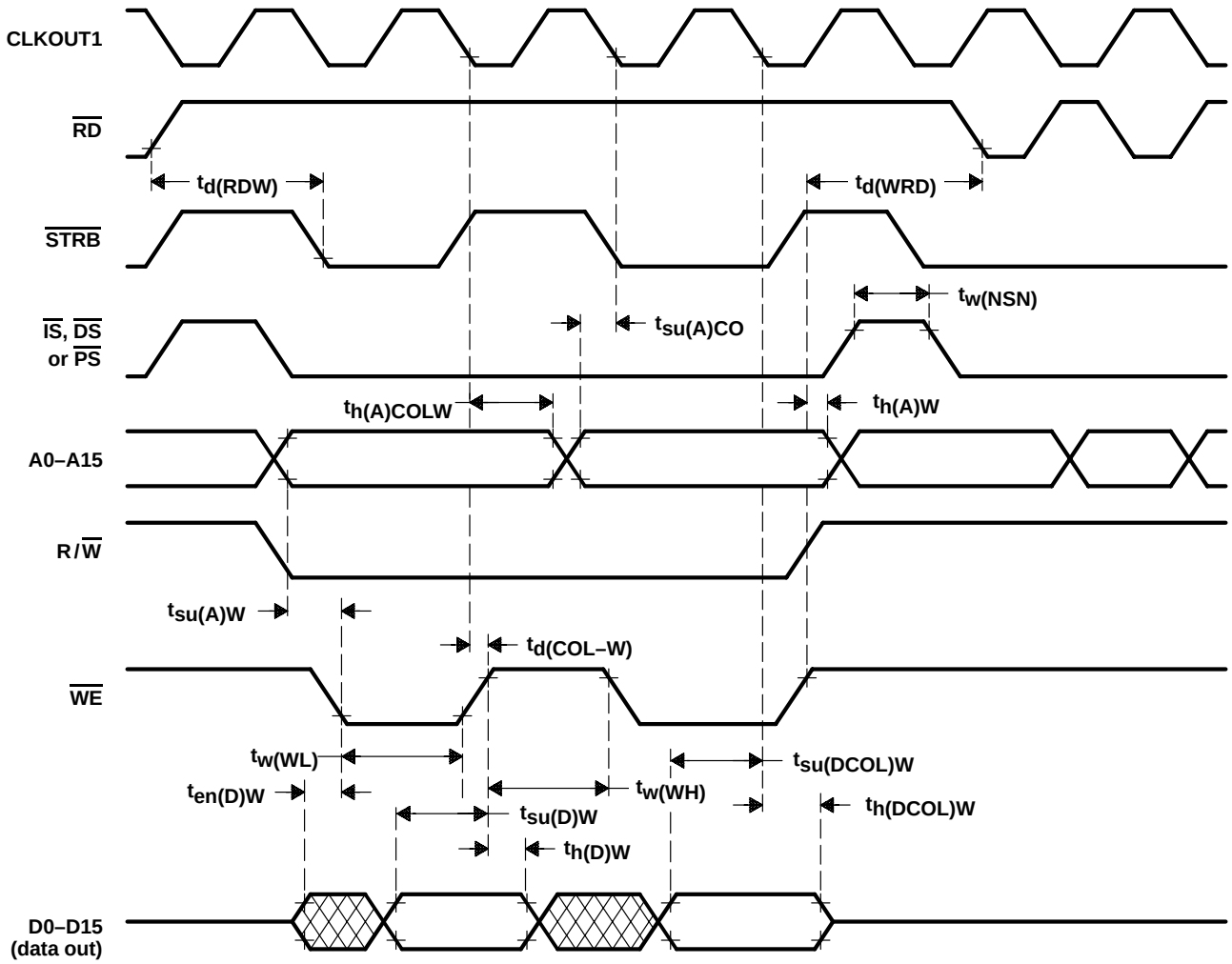


Figure 14. Memory Interface Write Timing

ADVANCE INFORMATION

READY timing

timing requirements over recommended operating conditions for TMS320C2xx @ 5 V (see Figure 15)

		’320C2xx-40 ’320C2xx-57		’320C2xx-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(R-CO)}$	Setup time, READY before CLKOUT1 rising edge	11		11		ns
$t_{h(CO-R)}$	Hold time, READY after CLKOUT1 rising edge	0		0		ns
$t_{su(R)RD}$	Setup time, READY before $\overline{RD}$ falling edge	14		14		ns
$t_{h(R)RD}$	Hold time, READY after $\overline{RD}$ falling edge	4		4		ns
$t_{v(R)W}$	Valid time, READY after $\overline{WE}$ falling edge	H – 14		H – 14		ns
$t_{h(R)W}$	Hold time, READY after $\overline{WE}$ falling edge	H + 4		H + 3		ns
$t_{v(R)ARD}$	Valid time, READY after address valid on read		H – 17		H – 16	ns
$t_{v(R)AW}$	Valid time, READY after address valid on write		2H – 18		2H – 16	ns

timing requirements over recommended operating conditions for TMS320LC2xx @ 3.3 V (see Figure 15)

		’320LC2xx-40		UNIT
		MIN	MAX	
$t_{su(R-CO)}$	Setup time, READY before CLKOUT1 rising edge	17		ns
$t_{h(CO-R)}$	Hold time, READY low after CLKOUT1 rising edge	0		ns
$t_{su(R)RD}$	Setup time, READY before $\overline{RD}$ falling edge	22		ns
$t_{h(R)RD}$	Hold time, READY after $\overline{RD}$ falling edge	4		ns
$t_{v(R)W}$	Valid time, READY after $\overline{WE}$ falling edge	H – 23		ns
$t_{h(R)W}$	Hold time, READY after $\overline{WE}$ falling edge	H + 4		ns
$t_{v(R)ARD}$	Valid time, READY after address valid on read		H – 22	ns
$t_{v(R)AW}$	Valid time, READY after address valid on write		2H – 21	ns

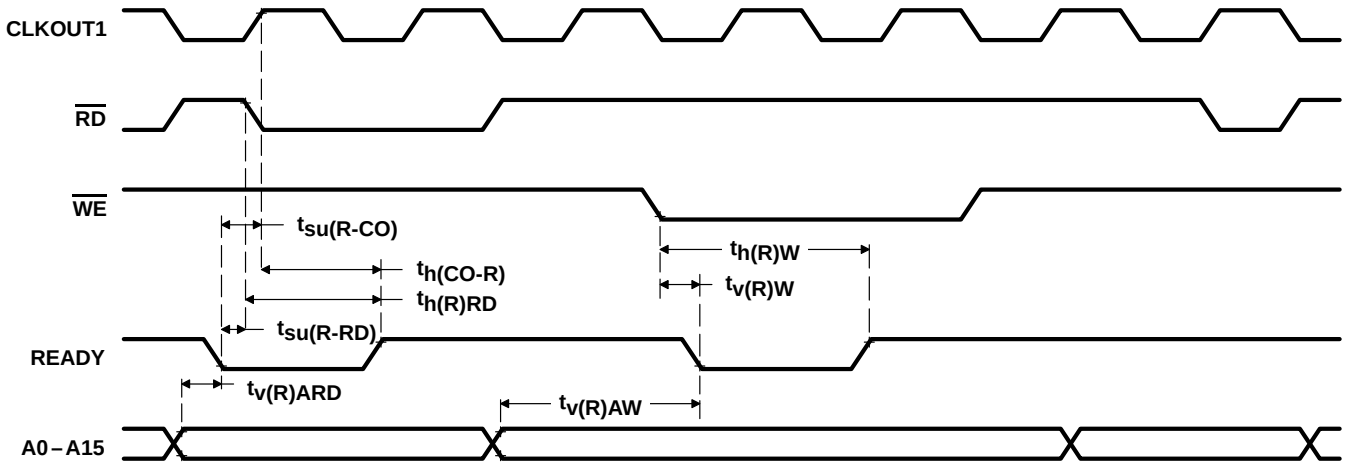


Figure 15. READY Timing

XF, TOUT, $\overline{RS}$, $\overline{INT1}$ – $\overline{INT3}$, $\overline{NMI}$, and $\overline{BIO}$ timing

switching characteristics over recommended operating conditions for TMS320C2xx @ 5 V (see Figure 16)

PARAMETER		'320C2xx-40 '320C2xx-57		'320C2xx-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{d(XF)}$	Delay time, XF valid after CLKOUT1	0†	13	0†	10	ns
$t_{d(TOUT)}$	Delay time, TOUT high/low after CLKOUT1	0†	11†	0†	11	ns
$t_{w(TOUT)}$	Pulse duration, TOUT high	2H – 12		2H – 9		ns

† Values derived from characterization data and not tested

switching characteristics over recommended operating conditions for TMS320LC2xx @ 3.3 V (see Figure 16)

PARAMETER		'320LC2xx-40		UNIT
		MIN	MAX	
$t_{d(XF)}$	Delay time, XF valid after CLKOUT1	0†	12	ns
$t_{d(TOUT)}$	Delay time, TOUT high/low after CLKOUT1	0†	15	ns
$t_{w(TOUT)}$	Pulse duration, TOUT high	2H – 12		ns

† Values derived from characterization data and not tested

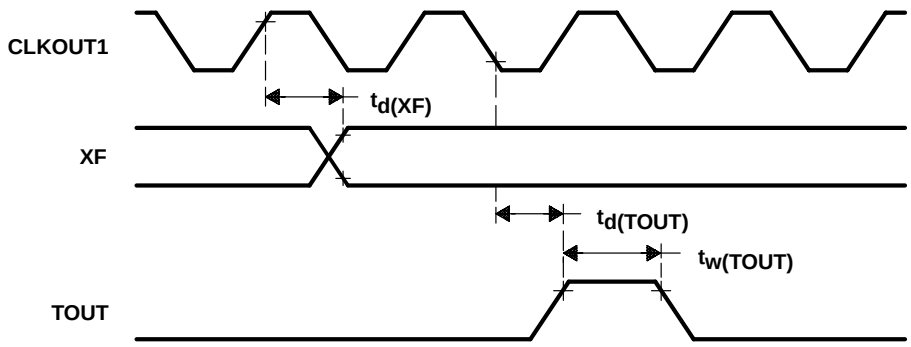


Figure 16. XF and TOUT Timing

ADVANCE INFORMATION

XF, TOUT, $\overline{RS}$, $\overline{INT1}$ – $\overline{INT3}$, $\overline{NMI}$, and $\overline{BIO}$ timing (continued)

timing requirements over recommended operating conditions for TMS320C2xx @ 5 V [H = 0.5$t_{c(CO)}$] (see Figure 17 and Figure 18)

		’320C2xx-40 ’320C2xx-57		’320C2xx-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(RS)CIL}$	Setup time, $\overline{RS}$ before CLKIN low	11		9		ns
$t_{su(RS)COL}$	Setup time, $\overline{RS}$ before CLKOUT1 low	14		11		ns
$t_{w(RSL)}$	Pulse duration, $\overline{RS}$ low†	12H		12H		ns
$t_{d(EX)}$	Delay time, $\overline{RS}$ high to reset-vector fetch	34H		34H		ns
$t_{su(IN)COL}$	Setup time, INTN before CLKOUT1 low (synchronous)	10		10		ns
$t_{h(IN)COL}$	Hold time, INTN after CLKOUT1 low (synchronous)	1		1		ns
$t_{w(IN)}$	Pulse duration, INTN low/high	2H + 18		2H + 16		ns
$t_{d(IN)}$	Delay time, INTN low to interrupt-vector fetch	12H		12H		ns

† This parameter assumes the CLKOUT1 to be stable before $\overline{RS}$ goes active.

timing requirements over recommended operating conditions for TMS320LC2xx @ 3.3 V [H = 0.5$t_{c(CO)}$] (see Figure 17 and Figure 18)

		’320LC2xx-40		UNIT
		MIN	MAX	
$t_{su(RS)CIL}$	Setup time, $\overline{RS}$ before CLKIN low	11		ns
$t_{su(RS)COL}$	Setup time, $\overline{RS}$ before CLKOUT1 low	15		ns
$t_{w(RSL)}$	Pulse duration, $\overline{RS}$ low†	12H		ns
$t_{d(EX)}$	Delay time, $\overline{RS}$ high to reset-vector fetch	34H		ns
$t_{su(IN)COL}$	Setup time, INTN before CLKOUT1 low (synchronous)	10		ns
$t_{h(IN)COL}$	Hold time, INTN after CLKOUT1 low (synchronous)	1		ns
$t_{w(IN)}$	Pulse duration, INTN low/high	2H + 18		ns
$t_{d(IN)}$	Delay time, INTN low to interrupt-vector fetch	12H		ns

† This parameter assumes the CLKOUT1 to be stable before $\overline{RS}$ goes active.

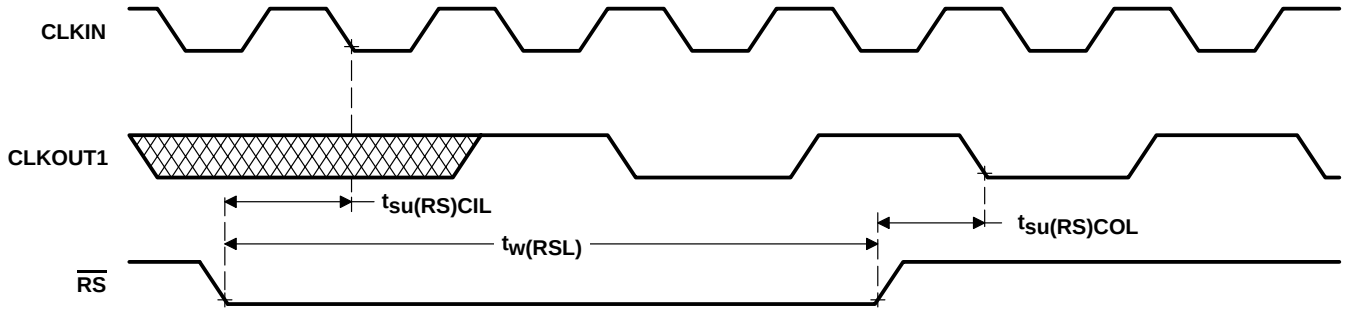


Figure 17. Reset Timing

XF, TOUT, $\overline{RS}$, $\overline{INT1}$ – $\overline{INT3}$, $\overline{NMI}$, and $\overline{BIO}$ timing (continued)

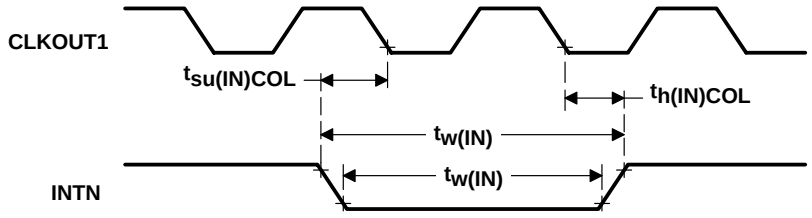


Figure 18. Interrupts and $\overline{BIO}$ Timing

external DMA timing

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 19)

PARAMETER		'320C2xx-40 '320C2xx-57 '320LC2xx-40		'320C2xx-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{d(HL-HAL)}$	Delay time, $\overline{HOLD}$ low to $\overline{HOLDA}$ low†	4H		4H		ns
$t_{d(HH-HAH)}$	Delay time, $\overline{HOLD}$ high before $\overline{HOLDA}$ high†	2H		2H		ns
$t_{z(M-HAL)}$	Address high impedance before $\overline{HOLDA}$ low‡§	H – 15		H – 10		ns
$t_{en(HAH-M)}$	Enable time, $\overline{HOLDA}$ high to address driven§	H – 5		H – 4		ns

† The delay values will change based on the software logic that activates $\overline{HOLDA}$. See the *TMS320C2xx User's Guide* (literature number SPRU127) for functional description of HOLD logic.
‡ This parameter includes all memory control lines.
§ Values derived from characterization data and not tested

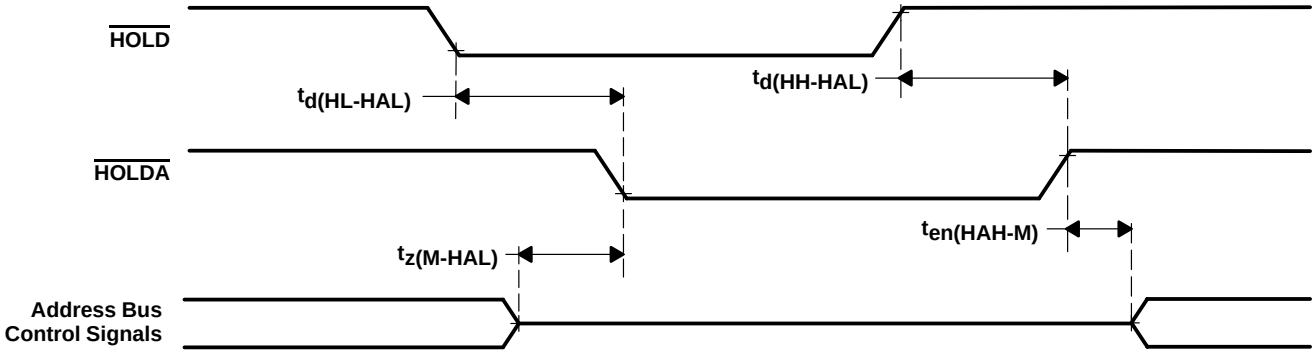


Figure 19. External DMA Timing

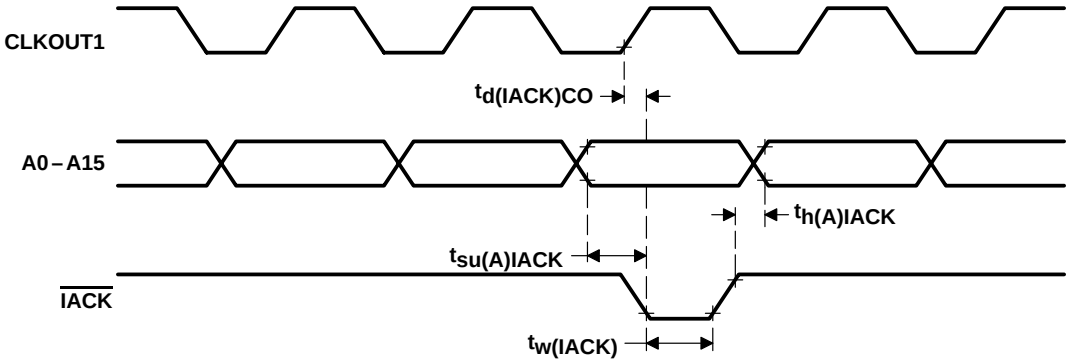
$\overline{\text{IACK}}$ timing (’C209 only)

$\overline{\text{IACK}}$ goes low during the fetch of the first word of the interrupt vector. It goes low only on the first cycle of the read when wait states are used. Address pins A1–A4 can be decoded at the falling edge to identify the interrupt being acknowledged.

switching characteristics over recommended operating conditions [H = 0.5 $t_{c(CO)}$] (see Figure 20)

PARAMETER		’320C209-40 ’320C209-57		UNIT
		MIN	MAX	
$t_{su(A)IACK}$	Setup time, address valid before $\overline{\text{IACK}}$ low†	H – 9		ns
$t_{h(A)IACK}$	Hold time, address valid after $\overline{\text{IACK}}$ high†	H – 7		ns
$t_{w(IACK)}$	Pulse duration, $\overline{\text{IACK}}$ low†	H – 7		ns
$t_{d(IACK)CO}$	Delay time, CLKOUT1 to $\overline{\text{IACK}}$ low	– 1†	3	ns

† Values derived from characterization data and not tested



NOTE A: $\overline{\text{IACK}}$ are not affected by wait states.

Figure 20. $\overline{\text{IACK}}$ Timing

serial-port receive timing

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = 0.5$t_{c(CO)}$] (see Figure 21)

		’320C2xx-40 ’320C2xx-57 ’320LC2xx-40		’320C2xx-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial-port clock	4H		4H		ns
$t_{f(SCK)}$	Fall time, serial-port clock†		8		6	ns
$t_{r(SCK)}$	Rise time, serial-port clock†		8		6	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2H		2H		ns
$t_{su(FS)}$	Setup time, FSR before CLKR falling edge	10		7		ns
$t_{su(DR)}$	Setup time, DR before CLKR falling edge	10		7		ns
$t_{h(FS)}$	Hold time, FSR after CLKR falling edge	10		7		ns
$t_{h(DR)}$	Hold time, DR after CLKR falling edge	10		7		ns

† Values derived from characterization data and not tested

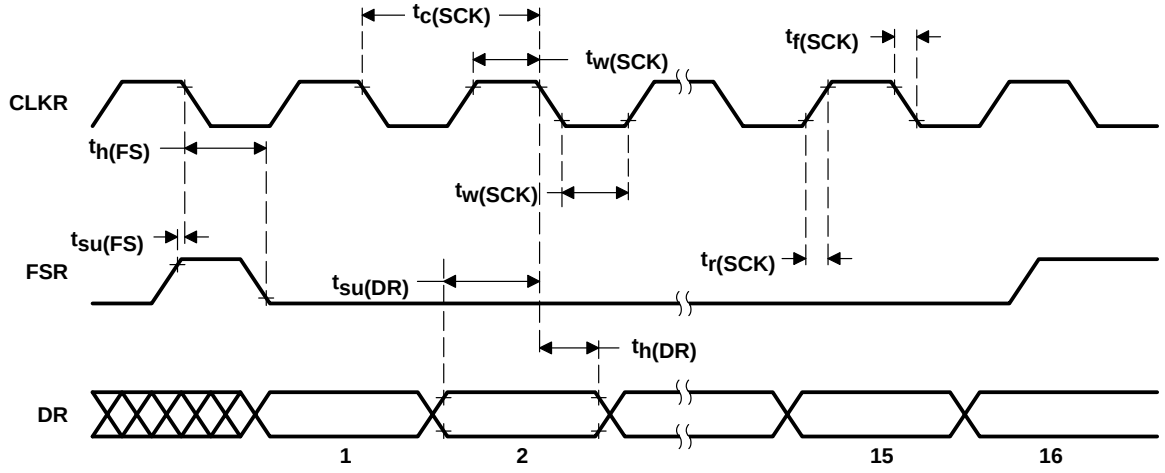


Figure 21. Serial-Port Receive Timing

serial-port transmit timing of external clocks and external frames

switching characteristics over recommended operating conditions (see Figure 22)

PARAMETER		’320C2xx-40 ’320C2xx-57 ’320LC2xx-40†		’320C2xx-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{d(DX)}$	Delay time, DX valid after CLKX high		25		25	ns
$t_{dis(DX)}$	Disable time, DX valid after CLKX high†		40		40	ns
$t_{h(DX)}$	Hold time, DX valid after CLKX high	– 5		– 5		ns

† Values derived from characterization data and not tested

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = 0.5$t_{c(CO)}$] (see Figure 22)

		’320C2xx-40 ’320C2xx-57 ’320LC2xx-40†		’320C2xx-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial-port clock	4H		4H		ns
$t_{f(SCK)}$	Fall time, serial-port clock†		8		6	ns
$t_{r(SCK)}$	Rise time, serial-port clock†		8		6	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2H		2H		ns
$t_{d(FS)}$	Delay time, FSX after CLKX rising edge high		2H – 8		2H – 8	ns
$t_{h(FS)}$	Hold time, FSX after CLKX falling edge low	10		7		ns
$t_{h(FS)H}$	Hold time, FSX after CLKX rising edge high†		2H – 8		2H – 8	ns

† Values derived from characterization data and not tested

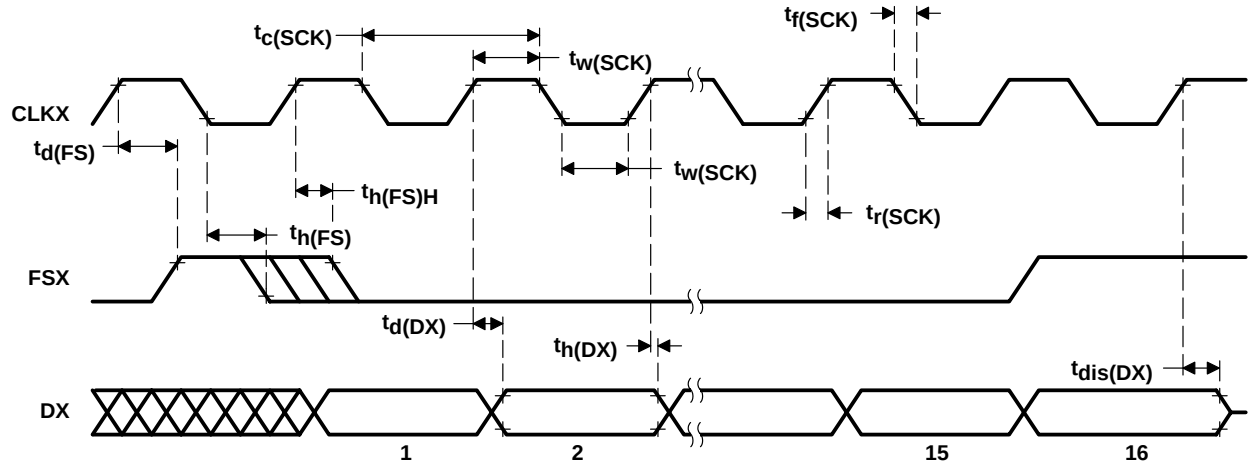


Figure 22. Serial-Port Transmit Timing of External Clocks and External Frames

ADVANCE INFORMATION

serial-port transmit timing of internal clocks and internal frames

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 23)

PARAMETER		'320C2xx-40 '320C2xx-57 '320LC2xx-40			'320C2xx-80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{d(DX)}$	Delay time, CLKX to DX			25			18	ns
$t_{dis(DX)}$	Disable time, CLKX rising to DX			40†			29†	ns
$t_{h(DX)}$	Hold time, DX valid after CLKX rising high	0†			0†			ns

† Values derived from characterization data and not tested

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = 0.5$t_{c(CO)}$] (see Figure 23)

		'320C2xx-40 '320C2xx-57 '320LC2xx-40			'320C2xx-80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(SCK)}$	Cycle time, serial-port clock		4H			4H		ns
$t_{f(SCK)}$	Fall time, serial-port clock†		5			4		ns
$t_{r(SCK)}$	Rise time, serial-port clock†		5			4		ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2H – 8†			2H – 6†			ns
$t_{d(FS)}$	Delay time, CLKX rising to FSX	– 5†		25	– 4†		18	ns

† Values derived from characterization data and not tested

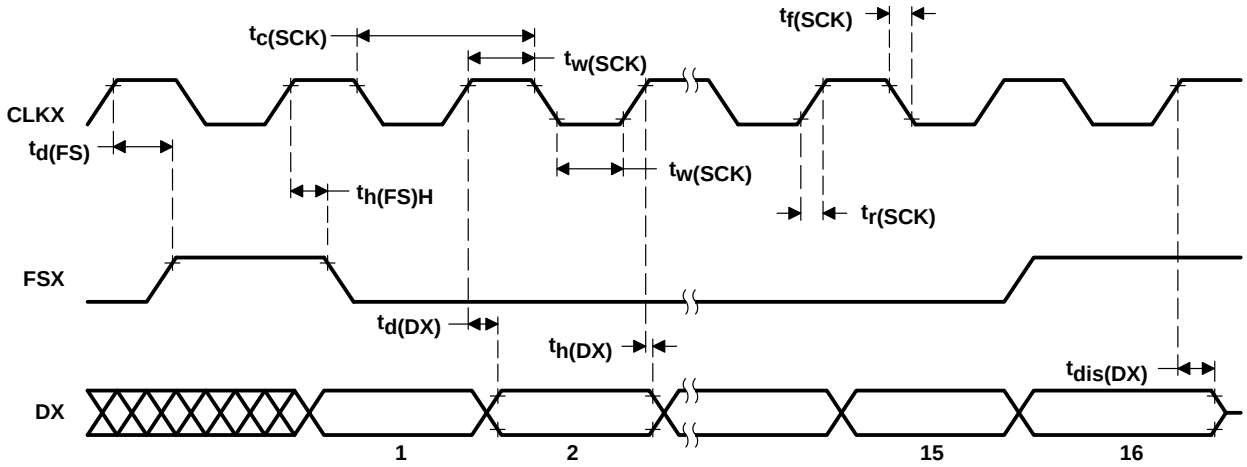
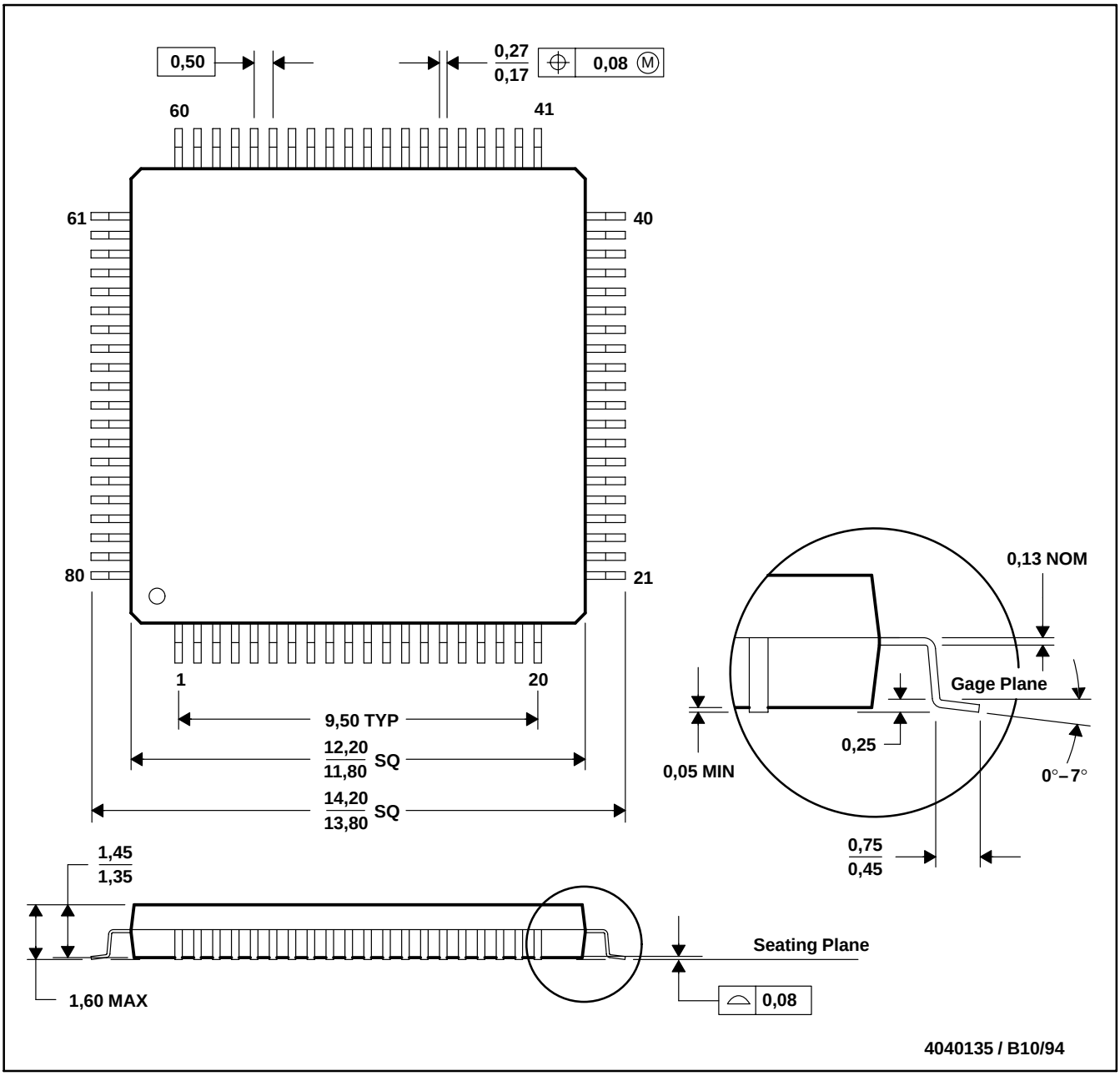


Figure 23. Serial-Port Transmit Timing of Internal Clocks and Internal Frames

MECHANICAL DATA

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



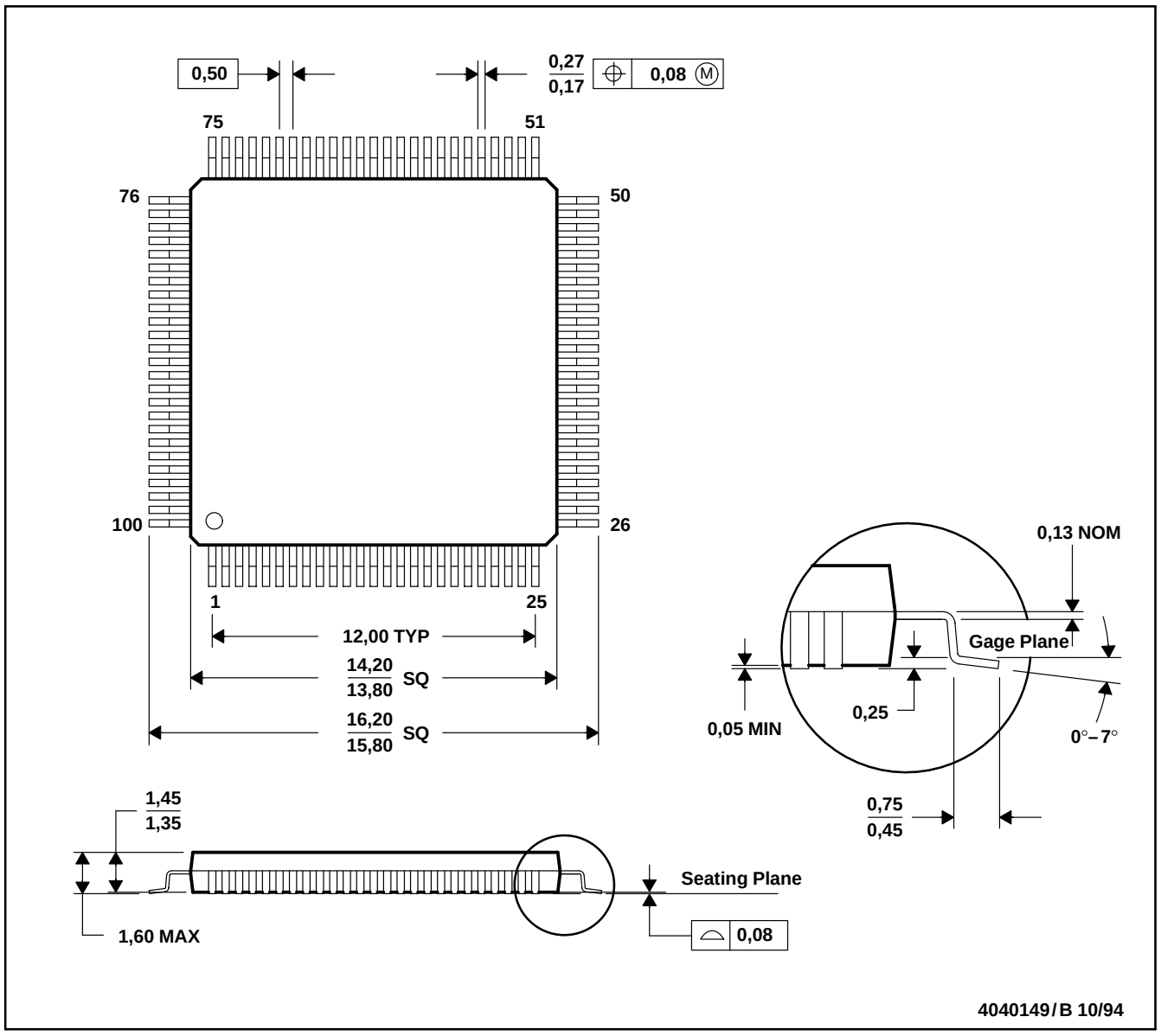
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

ADVANCE INFORMATION

ADVANCE INFORMATION

MECHANICAL DATA

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
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