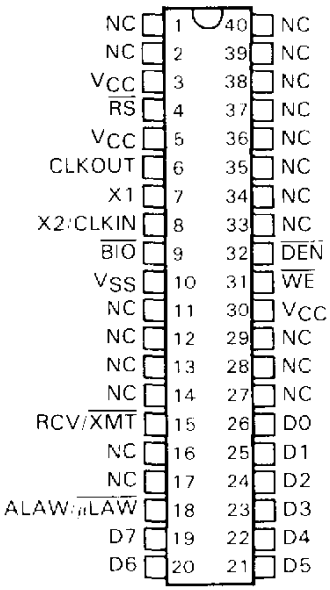
TMS320SA32
32 KBIT/S ADPCM TRANSCODER

SPRS011 NOVEMBER 1986

- ANSI 32 kbit/s ADPCM Compatible
- CCITT G.721 32 kbit/s ADPCM Compatible
- Half-Duplex Transcoder Operation
- Transmit/Receive Selection Option
- μ-Law/A-Law PCM Selection Option
- 8-Bit Parallel Data Bus
- 8-kHz PCM Sample Rate
- 20.5-MHz Clock Rate
- 165-mW Typical Power Dissipation
- CMOS Technology
- Single 5-V Supply

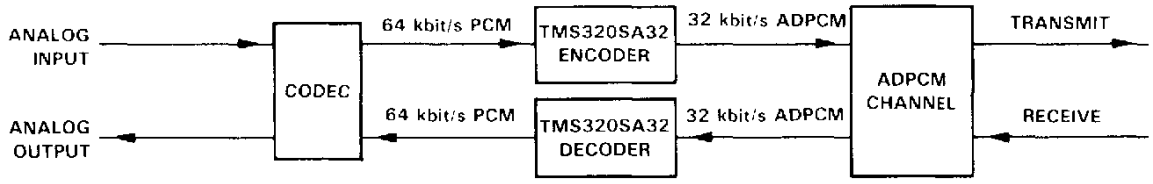
N PACKAGE
(TOP VIEW)



description

The TMS320SA32 is a CMOS half-duplex 32 kbit/s ADPCM transcoder. The transcoder implementation is fully compatible with the 32 kbit/s ADPCM standards defined by ANSI (May 1986) and CCITT (July 1986) G.721. A single device is necessary for either the encoding from 64 kbit/s PCM to 32 kbit/s ADPCM, or for the decoding from 32 kbit/s ADPCM to 64 kbit/s PCM. The same device can be pin-selected for transmitting (encoding) or receiving (decoding) and for processing the PCM data, based on either the μ-law or A-law formats. Data is received and transmitted on a single 8-bit parallel data bus. The 4-bit ADPCM data is right-justified on the 8-bit bus. Data is read at 125-μs intervals when $\overline{BIO}$ is active low, and written within 53 μs after the read occurs. Typical power dissipation of the device is 165 mW.

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

PIN NOMENCLATURE

NAME	I/O	DEFINITION
D7-D0	I/O	8-bit data bus (D7-D0 PCM :: D3-D0 ADPCM)
ALAW/$\overline{\mu LAW}$	I	A-law/μ-law PCM data coding
RCV/$\overline{XMT}$	I	Receive/transmit half-duplex operation
$\overline{BIO}$	I	External polled input for new sample data. When the sample processing ends, the device tests $\overline{BIO}$. While $\overline{BIO}$ is high, the device continues to wait. When $\overline{BIO}$ is low, the device begins a new processing cycle. The input sample is read, and within 53 μs an output sample is written.
$\overline{DEN}$	O	Data enable indicating the device is accepting data on D7-D0
$\overline{WE}$	O	Write enable indicating valid data on D7-D0
$\overline{RS}$	I	Reset used to initalize the device. When reset, the device waits for the synchronization signal on the $\overline{BIO}$ pin. An active signal on $\overline{BIO}$ initiates the initialization procedure, including the normal I/O operations. An input sample of >0A causes the device to continue the initialization cycle. When a sample other than >0A is input, the device begins the normal processing cycle.
X1	O	Output from internal oscillator for crystal.
X2/CLKIN	I	Input to internal oscillator from crystal or external clock
CLKOUT	O	System clock output, ¼ crystal/CLKIN frequency
V_{CC}	I	5 V power supply
V_{SS}	I	Ground
NC		No connection

architecture

The TMS320SA32 is based on Texas Instruments TMS320C10 Digital Signal Processor (DSP). The TMS320C10 is a CMOS pin-for-pin compatible version of the industry-standard TMS32010 DSP. The 16/32-bit Harvard architecture increases throughput for high-speed and numeric-intensive applications. The general-purpose instruction set, which includes digital signal processing instructions, facilitates programming to meet a broad range of algorithm requirements. The TMS320C10's high-performance 5-MIPS operation is already widely used in telecommunications, computer, instrumentation, medical, automotive, military, and control applications.

The TMS320C10 Digital Signal Processor is a programmable device. This feature allows for future updates in the CCITT ADPCM algorithm with no hardware redesign or relayout. Using an industry-standard component, such as the TMS320C10, reduces risk and preserves the customer's investment. Half-duplex algorithms, such as voice mail, can take advantage of using a single device to perform both the encoder and decoder functions. The TMS320SA32 thus lowers both system and inventory cost. Power-sensitive applications, such as ADPCM transcoders and MUXs, can also benefit from the low power dissipation of this CMOS device.

32 kbit/s ADPCM algorithm

The CCITT Recommendation G.721[†] or ANSI documentation[‡] provides a full description of the encoder and decoder algorithm based on the Adaptive Differential Pulse Code Modulation (ADPCM) transcoding technique. The function and transcoding process of the encoder and decoder are described in the following paragraphs. Figure 1 shows a block diagram of the ADPCM encoder and decoder.

encoder

The function of the encoder or transmitter, shown in Figure 1(a), is to receive a 64 kbit/s PCM signal and transcode it to a 32 kbit/s ADPCM signal. This is accomplished by converting the μ-law/A-law PCM signal s(k) to a linear signal from which an estimate of the signal $s_e(k)$ is subtracted to obtain a difference signal $d_q(k)$. The next step is to adaptively quantize this difference signal. The 15-level quantizer produces the output that is the 4-bit ADPCM code. The speed of adaptation automatically varies from a low speed for voiceband data to a high speed for speech signals. A speed control factor $a_l(k)$ weights the fast and slow adaptation factors to form a single quantization scale factor y(k).

The inverse adaptive quantizer uses the same signal I(k) that has been transmitted to reconstruct a quantized difference signal $d_q(k)$ with the same adaptive quantization characteristics as the adaptive quantizer section. This signal is input to an adaptive predictor for computing a signal estimate. The predictor includes a second order all-pole filter and a sixth-order all-zero filter. The signal estimate $s_e(k)$ is combined with the difference signal $d_q(k)$ to determine a reconstructed signal $s_r(k)$, the output of the decoder.

decoder

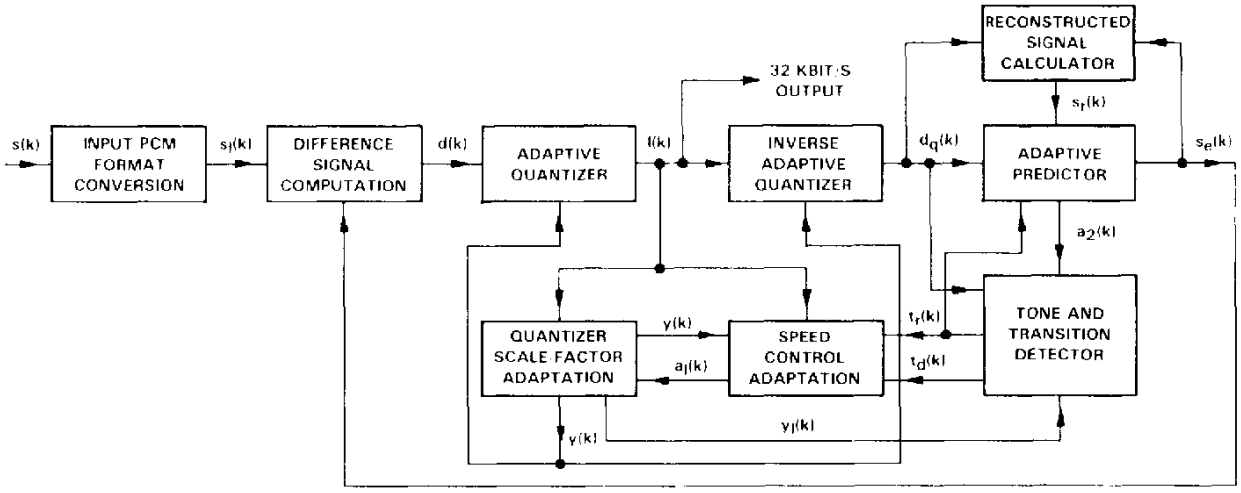
The function of the decoder or receiver, shown in Figure 1(b), is to receive a 32 kbit/s ADPCM signal and transcode it to a 64 kbit/s PCM signal. To accomplish this, the decoder utilizes many of the elements used by the encoder since the decoder is actually imbedded in the encoder. The received data I(k) is processed by an inverse adaptive quantizer to determine a quantized difference signal $d_q(k)$. By filtering the difference signal through the adaptive predictor together with the previously reconstructed signal $s_r(k)$, a signal estimate $s_e(k)$ is obtained. The signal estimate is added to the difference signal to compute the reconstructed signal $s_r(k)$ that is then converted from a linear signal to a PCM signal $s_p(k)$ and output following a synchronous coding adjustment. This adjustment can modify the output PCM signal by one step so that an encoder synchronously connected to the decoder produces the same ADPCM signal as the one received by the decoder. In the absence of transmission errors, this procedure prevents cumulative distortion occurring on synchronous tandem codings.

Note that the algorithm design achieves a convergence of the states of the encoder and decoder in spite of transmission errors. This convergence is part of each of the adaptation computations.

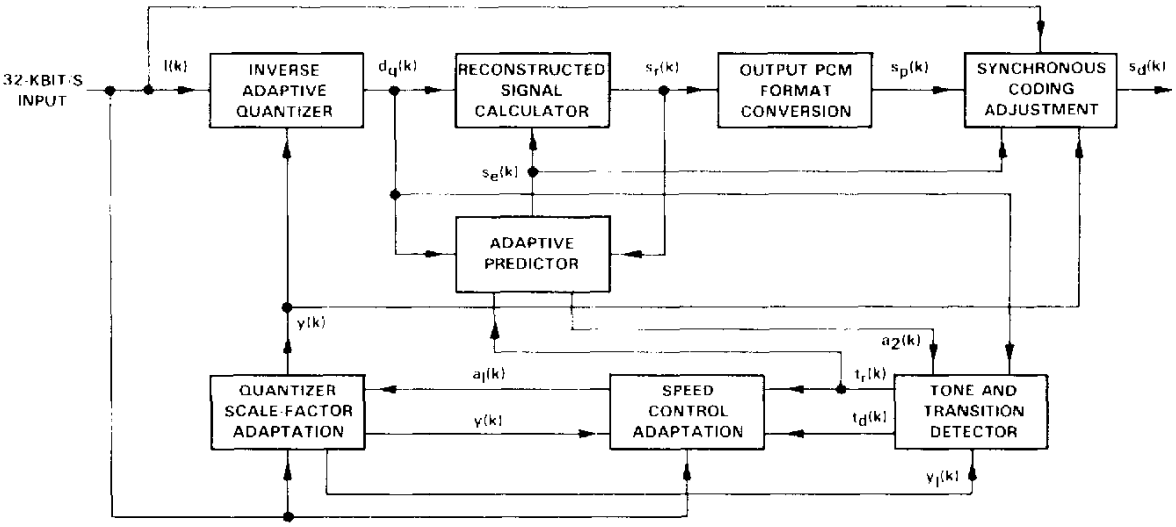
algorithm performance

Reported performance of the algorithm[§] in the transmission of speech signals reveals that the perceived quality is only slightly lower than that obtained with a 64 kbit/s PCM link and is equivalent to between three and four asynchronous PCM codings and decodings in cascade. The degradation is significant only for several ADPCM asynchronous codings and decodings in cascade. Voiceband data signals up to 2400 bit/s are not subject to significant degradations, and voiceband data performance at 4800 bit/s using modems to Recommendation V.27 bis is still acceptable after four codings and decodings in cascade.

[†]CCITT Recommendation G.721, "32 kbit/s Adaptive Differential Pulse Code Modulation (ADPCM)", adopted July 1986.
[‡]American National Standard, "32 kbit/s Adaptive Differential Pulse Code Modulation (ADPCM) Algorithm and Line Format," adopted May 1986.
[§]"The 32 kbit/s International Coding Standard," *GLOBECOM 84*, Session 23, Atlanta, GA, November 1984.



(a) ENCODER



(b) DECODER

FIGURE 1. ADPCM BLOCK DIAGRAM
(DIAGRAM TAKEN FROM CCITT RECOMMENDATION G.721 AND ANSI DOCUMENTATION)

processing description

The TMS320SA32¶ begins a normal processing cycle, shown in Figure 2, with the block CODE INPUT and ends with the block SYNCHRONIZATION. The function of the latter block is to wait for the synchronization signal, and after having received it, to branch to the beginning of the loop. The program organization is the same for both the encoder and decoder, except for the block ADPCM CODE COMPUTATION performed in the encoder only, and the block SYNCHRONOUS CODING ADJUSTMENT performed in the decoder only.

The processor first inputs a sample, which is the 8-bit PCM signal s(k) for the encoder and the 4-bit ADPCM signal I(k) for the decoder. In the encoder, the output 4-bit ADPCM sample I(k) is computed by the block ADPCM CODE COMPUTATION, including the input PCM format conversion, the difference signal computation, and the quantization.

The 4-bit ADPCM signal I(k) is then used by the block INVERSE QUANTIZER to compute the quantized difference signal $d_q(k)$ and the reconstructed signal $s_r(k)$. In the decoder, the reconstructed signal is converted and adjusted into the 8-bit PCM output sample $s_d(k)$ by the blocks RECONSTRUCTED SIGNAL CONVERSIONS and SYNCHRONOUS CODING ADJUSTMENT.

During a 125-μs cycle, the processor performs the adaptation of the parameters to be used in the next cycle. The blocks SCALE FACTOR ADAPTATION and SCALE FACTOR COMPUTATION update the speed control parameter $a_l(k)$, the quantizer scale factor y(k), and the tone and transition detection parameters $t_d(k)$ and $t_r(k)$.

The adaptive predictor computes both the new value of the coefficient and the partial product corresponding to a delayed variable, and repeats this procedure eight times. The signal estimate $s_e(k+1)$ for the next cycle is obtained by summing the partial products. The block PREDICTOR (A) corresponds mainly to the section modeling poles, and the block PREDICTOR (B) to the section modeling zeroes. The eight multiplications used to compute the signal estimate are performed in floating-point format. The conversion of the reconstructed signal $s_r(k)$ into floating-point format is performed in the block RECONSTRUCTED SIGNAL CONVERSIONS.

In the initialization procedure using $\overline{RS}$ (reset), the processor waits for the synchronization signal, then inputs a sample, and decodes the option selection as to encoder/decoder and μ-law/A-law. The RAM memory is loaded with the value of the state variables being initialized according to the CCITT and ANSI recommendations. The input code is output after filtering it. If the input code equals >0A, it returns to the beginning of the initialization routine, remaining in the initialization state. Otherwise, the main computation loop is entered. The duration of the initialization procedure is one 125-μs cycle.

initialization

The initialization procedure is designed for testing by the digital test sequences defined in the ANSI documentation and the CCITT Recommendation G.721. The procedure is entered by an action on the $\overline{RS}$ (reset) pin. After $\overline{RS}$ has returned high, the processor waits for $\overline{BIO}$ to go low, and then the initialization procedure begins. During initialization, the synchronization and the input/output operations are performed as in a normal cycle.

The input code controls the initialization procedure; i.e., the processor remains in the initialization state as long as the input code equals >0A for the encoder and >A for the decoder. When a code different from these is received (see Figure 3), the processor completes the initialization procedure until the end of the cycle, and then enters the computation loop. The next code, A1 or C1, is the first code to be processed after initialization. In a digital test, it must be the first sample of the input test sequence.

During initialization of the encoder, the output code is obtained by masking the four most significant bits of the input code; for the decoder, the output code is obtained by left-extending the 4-bit input code with zeroes. Therefore, when the input code is >0A (or >A), the output code >A (or >0A) is transmitted. This allows the synchronization of the receiving test equipment or of another coding stage.

The minimum duration of the initialization procedure is one PCM cycle, obtained when the first code entered after $\overline{RS}$ differs from >0A (or >A).

¶The ADPCM DSP code was developed by the Centre National d'Etudes (CNET) in France.

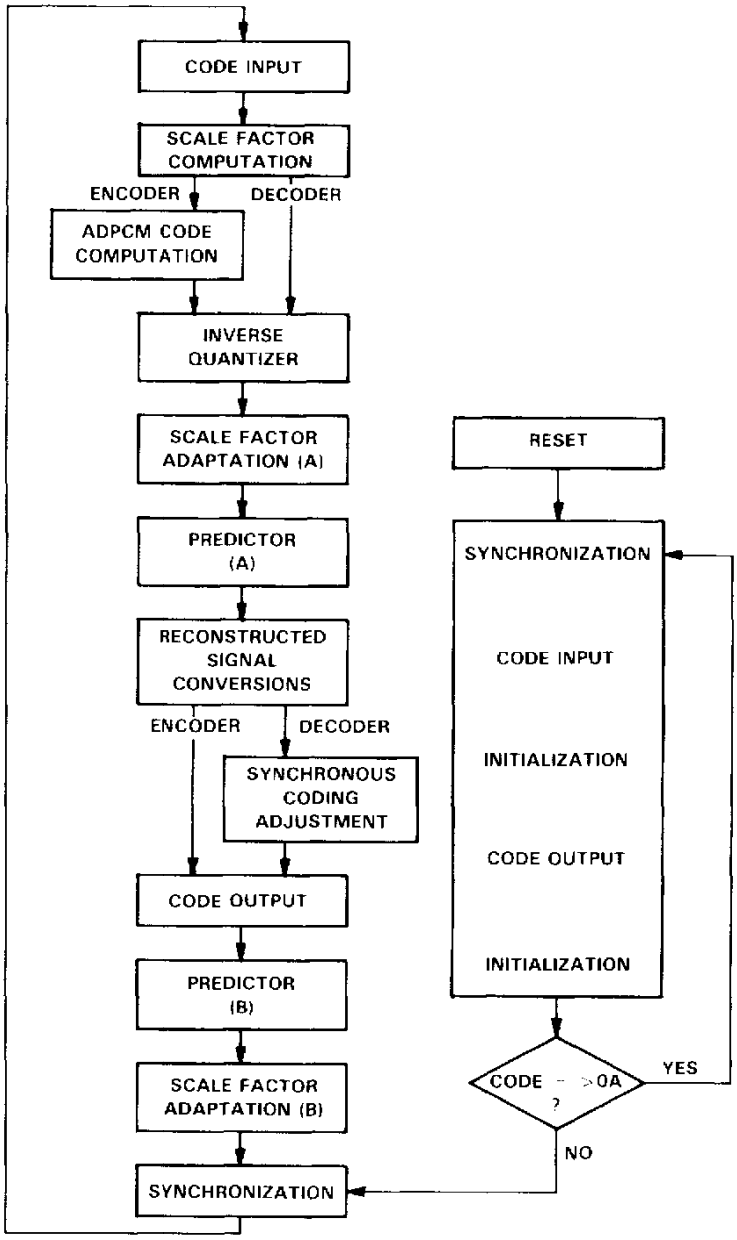
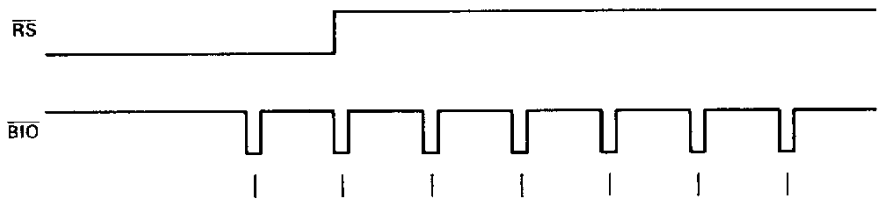


FIGURE 2. ADPCM TRANSCODER PROGRAM



CYCLE TYPE		RES	INI	INI	INI	CMP	CMP	CMP
Encoder	Input	None	>0A	>0A	>XY	A1	A2	A3
	Output	None	>A	>A	>Y	B1	B2	B3
Decoder	Input	None	>A	>A	>Z	C1	C2	C3
	Output	None	>0A	>0A	>0Z	D1	D2	D3

Legend:

$\overline{RS}$ = reset signal
$\overline{BIO}$ = synchronization signal. Its falling edge corresponds to the beginning of a 125-μs cycle.
RES = a reset cycle
INI = an initialization cycle
CMP = a normal computation cycle
>0A = 8-bit word used by encoder for initialization
>A = 4-bit word used by decoder for initialization
>XY = any 8-bit word different from >0A
>Y = 4-bit word output during encoder initialization (4 LSBs of >XY)
>Z = any 4-bit word different from >A
>0Z = 8-bit word output during decoder initialization (left extension of >Z with zeroes)
An = 8 bit PCM word
Bn = 4 bit ADPCM word, the result of An encoding
Cn = 4-bit ADPCM word
Dn = 8-bit PCM word, the result of Cn decoding
B1, D1 = computed value of the state variables, which is the initialization value

FIGURE 3. GENERAL I/O TIMING

input/output operations

The TMS320SA32 is synchronized through the $\overline{BIO}$ pin. When the computations corresponding to a sample are finished, the processor is placed in a wait state until the $\overline{BIO}$ signal goes low. Therefore, the falling edge of $\overline{BIO}$ determines the beginning of the computation cycle.

The first operation consists of inputting a sample. The output of the corresponding processed sample is performed approximately 53 μs later. The processor next completes the computation by adapting some parameters for the next cycle. The full computation duration corresponding to one sample is less than 125 μs, permitting an 8-kHz sampling rate.

TMS320SA32 ADPCM evaluation system

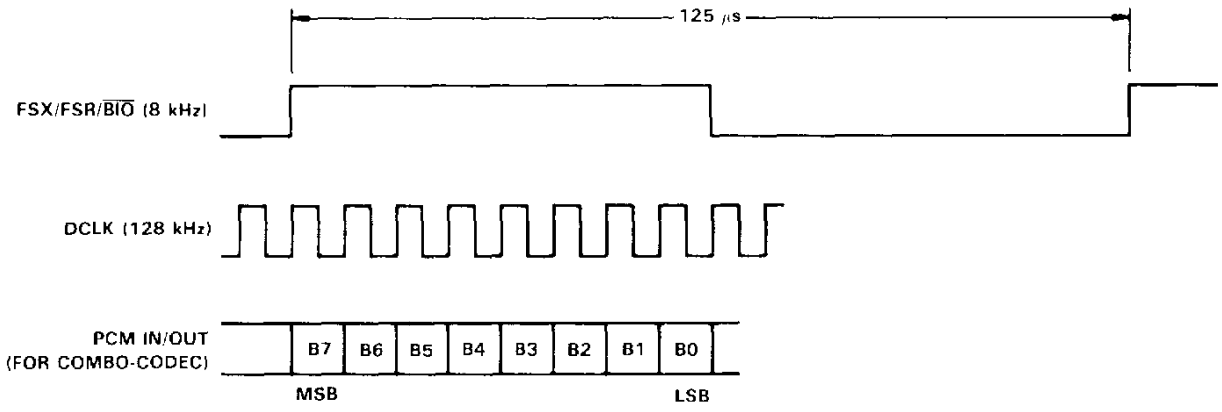
An example of an ADPCM evalulation system using a PCM codec, an ADPCM encoder, an ADPCM decoder, and a time base is shown in Figure 4. This schematic represents a possible implementation that a customer could use to test his own ADPCM system. It has been built and tested, but is not available as a product. The board can function in a local mode, implementing a one-way phone channel. The input analog signal is encoded into PCM by the codec. The codec PCM output is transferred to the ADPCM encoder through a serial interface. The encoder computes the ADPCM code for transmission. In a local mode, the ADPCM code is directly received by the ADPCM decoder. The PCM output is then decoded into an analog signal by the codec.

The ADPCM encoder and decoder each utilize a TMS320SA32 chip, an 8-bit shift/storage register 74LS299, an AND gate, and a D latch (½ 74LS74). The only difference in the coder hardware is the value placed on the RCV/$\overline{\text{XMT}}$ pin of the TMS320SA32. During every 125-μs PCM cycle, the TMS320SA32 reads the 8-bit word stored in the 74LS299 register, computes the output code, and writes it into the 74LS299. The output code is then transferred serially through the D latch while the next input code is simultaneously clocked into the 74LS299.

All of the digital interfaces are serial interfaces that transfer 8 bits every 125-μs cycle, 4 bits being set to zero for the ADPCM code. The delay introduced by the coders is then 125 μs. The $\overline{\text{RS}}$ (reset) signal can be used either to initialize the TMS320SA32 or to make the ADPCM coder serial interface transparent to PCM signals. The inputs and outputs of the ADPCM coders are externally accessible.

The time base provides all the clocks necessary to the codec and ADPCM coders. A clock connection permits a synchronous connection of several such designed ADPCM evaluation systems.

The PCM codec (with on-chip filters) chosen for this evaluation system is the Texas Instruments TCM29C13 that includes A-law and μ-law formats on the same circuit. A clocking and timing diagram for the codec interface is shown below.



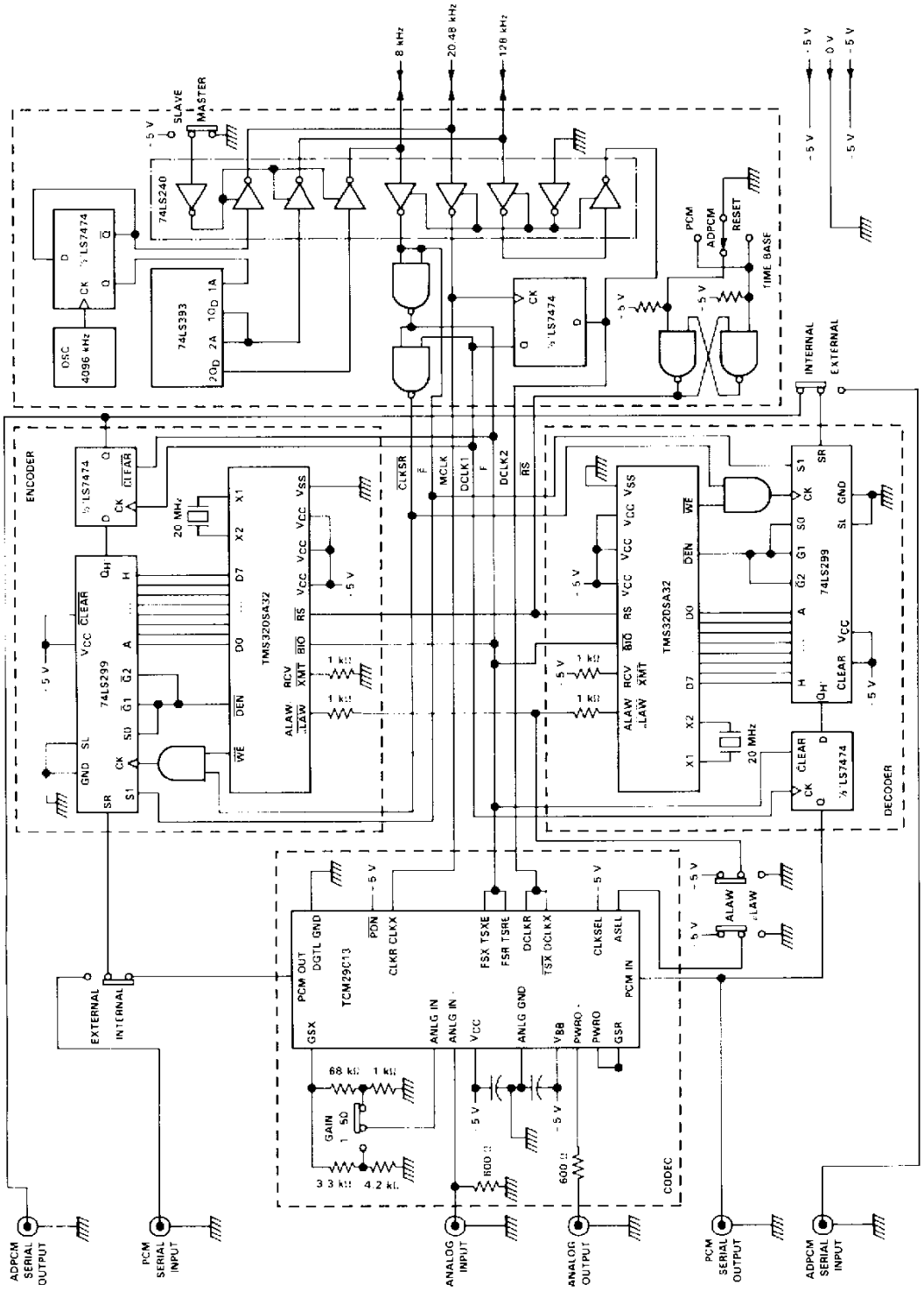


FIGURE 4. TMS320SA32 ADPCM SYSTEM EVALUATION SCHEMATIC

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}‡ . . . . . 0.3 V to 7 V
Input voltage range . . . . . −0.3 V to 15 V
Output voltage range . . . . . 0.3 V to 15 V
Continuous power dissipation . . . . . 0.3 W
Air temperature range above operating device . . . . . 0°C to 70°C
Storage temperature range . . . . . 55°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
‡All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High level input voltage	All inputs except CLKIN	2			V
		CLKIN	3			
V_{IL}	Low level input voltage (all inputs)				0.8	V
I_{OH}	High level output current (all outputs)		300			μA
I_{OL}	Low-level output current (all outputs)				2	mA
T_A	Operating free air temperature		0		70	°C

electrical characteristics over specified temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High level output voltage		I_{OH} MAX		2.4	3		V
			I_{OH} 20 μA (see Note 1)		V_{CC} 0.4†			V
V_{OL}	Low level output voltage		I_{OL} MAX			0.3	0.5	V
I_{OZ}	Off state output current		V_{CC} MAX	V_O 2.4 V			20	μA
				V_O 0.4 V			20	
I_I	Input current		V_I V_{SS} to V_{CC}				±50	μA
I_{CC}§	Supply current		f 20.5 MHz, V_{CC} 5.5 V			33	55	mA
C_i	Input capacitance	Data bus				25‡		pF
		All others				15‡		
C_o	Output capacitance	Data bus				25‡		pF
		All others				10‡		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Values derived from characterization data and not tested.
§I_{CC} characteristics are inversely proportional to temperature.
NOTE 1: This voltage specification is included for interface to HC logic. However, note that all of the other timing parameters defined in this data sheet are specified for TTL logic levels and will differ for HC logic levels.

CLOCK CHARACTERISTICS AND TIMING

The TMS320SA32 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 5). The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal frequency f_x	T_A = 40°C to 85°C	20.0		20.5	MHz
C1, C2	T_A = 40°C to 85°C		10		pF

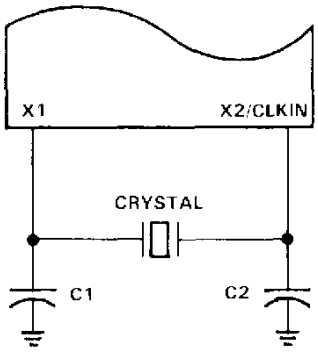


FIGURE 5. INTERNAL CLOCK OPTION

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table on page 13.

An effective method to generate the timings for the entire ADPCM circuit using a single clock source is shown in Figure 6. A 20.48-MHz crystal is used along with a SN74HC04 hex inverter for the input clock (CLKIN) to the TMS320SA32 and to the SN74HC390 decade counter. The 2.048-MHz clock generated by the decade counter is used as the master clock (MCLK) for the codec. A SN74ALS163 binary counter divides the master clock by 16 to generate the 128-kHz data clock (DCLK) for the system. Another SN74ALS163 binary counter divides the data clock again by 16 to generate the 8-kHz framing pulse ($\overline{FP}$) and the frame sync pulse $\overline{FS}$.

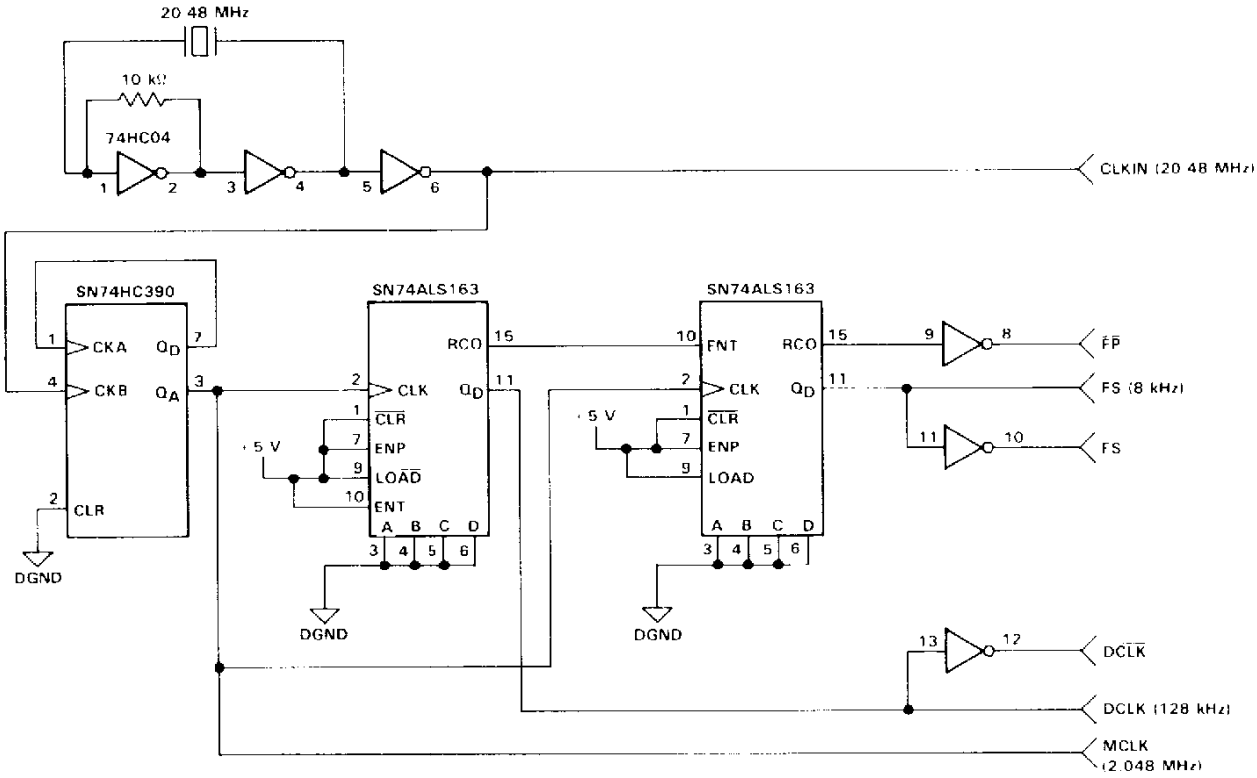


FIGURE 6. ADPCM CLOCK CIRCUIT

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{c(MC)}$	Master clock cycle time	48.78	50	150	ns
$t_{r(MC)}$	Rise time master clock input		5†	10†	ns
$t_{f(MC)}$	Fall time master clock input		5†	10†	ns
$t_{w(MCP)}$	Pulse duration master clock	$0.4t_{c(MC)}$†		$0.6t_{c(MC)}$†	ns
$t_{w(MCL)}$	Pulse duration master clock low		20†		ns
$t_{w(MCH)}$	Pulse duration master clock high		20†		ns

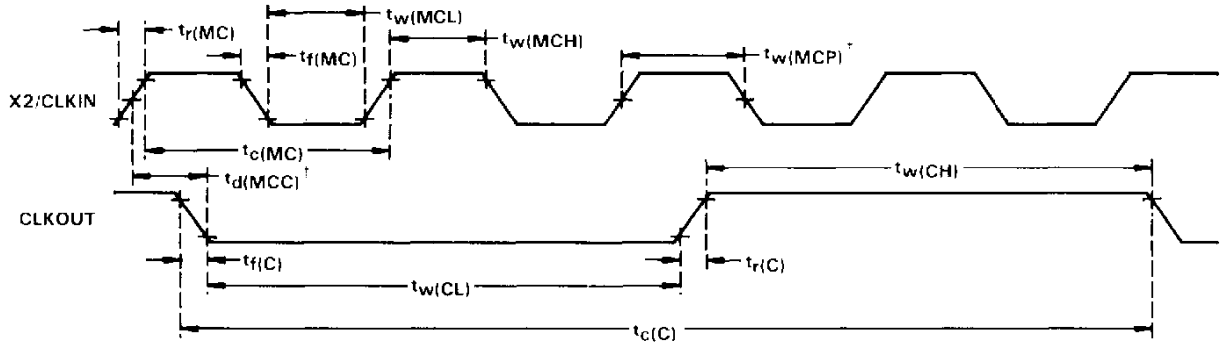
†Values derived from characterization data and not tested.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{c(C)}$	CLKOUT cycle time†	R_L = 825 Ω, C_L = 100 pF, See Figure 7	195.12	200		ns
$t_{r(C)}$	CLKOUT rise time			10‡		ns
$t_{f(C)}$	CLKOUT fall time			8‡		ns
$t_{w(CL)}$	Pulse duration, CLKOUT low			92‡		ns
$t_{w(CH)}$	Pulse duration, CLKOUT high			90‡		ns
$t_{d(MCC)}$	Delay time CLKIN† to CLKOUT↓		25‡		60‡	ns

†$t_{c(C)}$ is the cycle time of CLKOUT, i.e., $4*t_{c(MC)}$ (4 times CLKIN cycle time if an external oscillator is used).
‡Values derived from characterization data and not tested.

clock timing



NOTE 2: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted. †$t_{d(MCC)}$ and $t_{w(MCP)}$ are referenced to an intermediate level of 1.5 volts on the CLKIN waveform.

PARAMETER MEASUREMENT INFORMATION

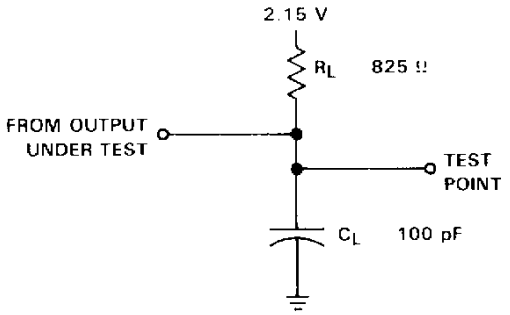


FIGURE 7. TEST LOAD CIRCUIT

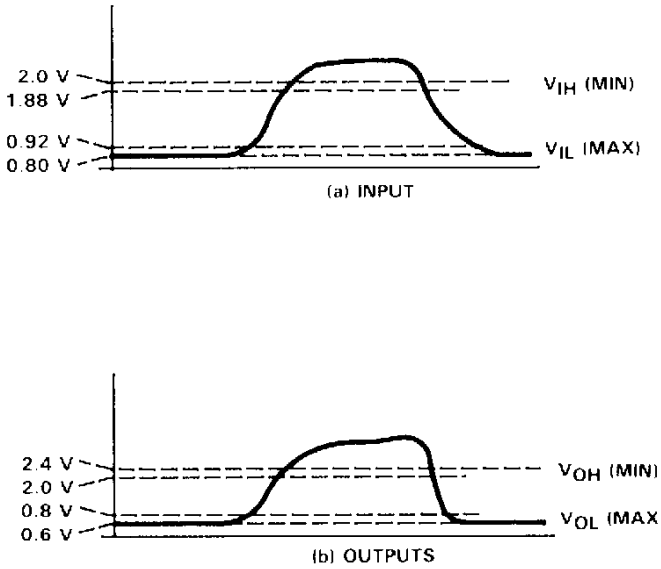


FIGURE 8. VOLTAGE REFERENCE LEVELS

PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d1}	Delay time CLKOUT↑ to $\overline{DEN}$↓	R_L = 825 Ω, C_L = 100 pF, See Figure 7	$\frac{1}{4}t_{c(C)}$ − 5†		$\frac{1}{4}t_{c(C)}$ + 15	ns
t_{d2}	Delay time CLKOUT↑ to $\overline{DEN}$↑		10†		15	ns
t_{d3}	Delay time CLKOUT↑ to $\overline{WE}$↓		$\frac{1}{4}t_{c(C)}$ − 5†		$\frac{1}{4}t_{c(C)}$ + 15	ns
t_{d4}	Delay time CLKOUT↑ to $\overline{WE}$↑		10†		15	ns
t_{d5}	Delay time CLKOUT↑ to data bus OUT valid				$\frac{1}{4}t_{c(C)}$ + 65	ns
t_{d6}	Time after CLKOUT↑ that data bus starts to be driven		$\frac{1}{4}t_{c(C)}$ − 5†			ns
t_{d7}	Time after CLKOUT↑ that data bus stops being driven				$\frac{1}{4}t_{c(C)}$ + 30†	ns
t_v	Data bus OUT valid after CLKOUT↑		$\frac{1}{4}t_{c(C)}$ − 10			ns

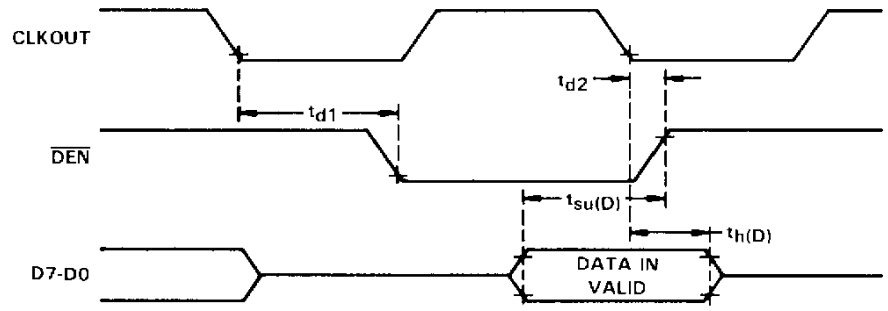
NOTE 3: Address bus will be valid upon $\overline{WE}$↑ or $\overline{DEN}$↑.
†These values were derived from characterization data and are not tested.

timing requirements over recommended operating conditions

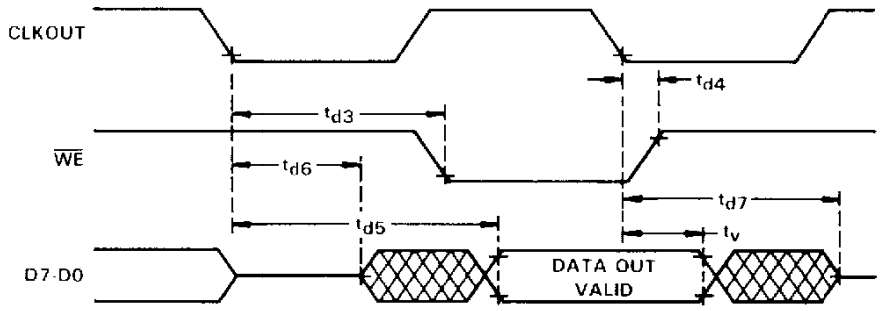
		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{su(D)}$	Setup time data bus valid prior to CLKOUT↑	R_L = 825 Ω, C_L = 100 pF, See Figure 7	50			ns
$t_{h(D)}$	Hold time data bus held valid after CLKOUT↑		0			ns

NOTE 4: Data may be removed from the data bus upon $\overline{MEN}$↑ or $\overline{DEN}$↑ preceding CLKOUT↑.

input cycle timing



output cycle timing



NOTE 2: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

RESET ($\overline{RS}$) TIMING

timing requirements over recommended operating conditions

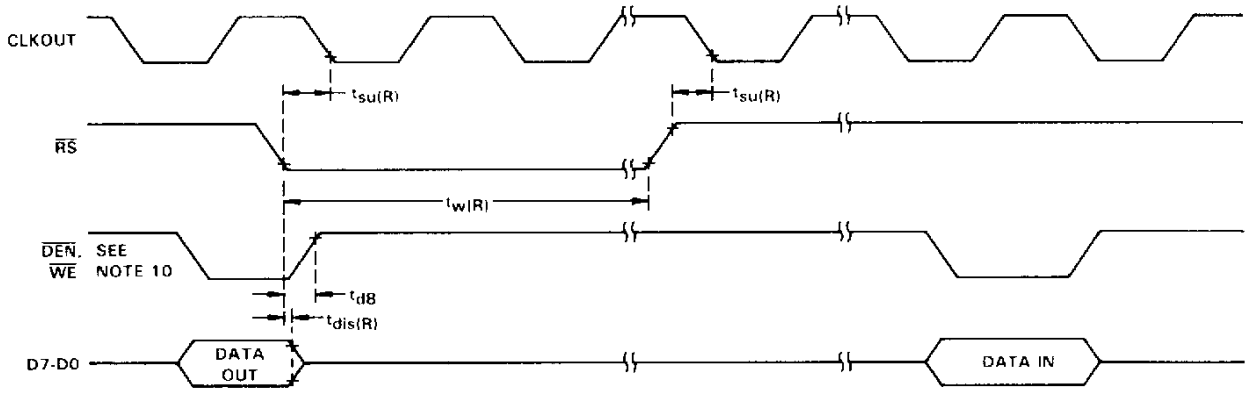
		MIN	NOM	MAX	UNIT
$t_{su(R)}$	Reset ($\overline{RS}$) setup time prior to CLKOUT. See Note 5.	50			ns
$t_{w(R)}$	$\overline{RS}$ pulse duration	$5t_{c(C)}$			ns

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d8}	Delay time $\overline{DEN}$ and $\overline{WE}$ from $\overline{RS}$	R_L 825 Ω, C_L 100 pF, See Figure 7			$\frac{1}{2}t_{c(C)} + 50$†	ns
$t_{dis(R)}$	Data bus disable time after $\overline{RS}$				$\frac{1}{4}t_{c(C)} + 50$†	ns

NOTE 5: $\overline{RS}$ can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.
†These values were derived from characterization data and are not tested.

reset timing



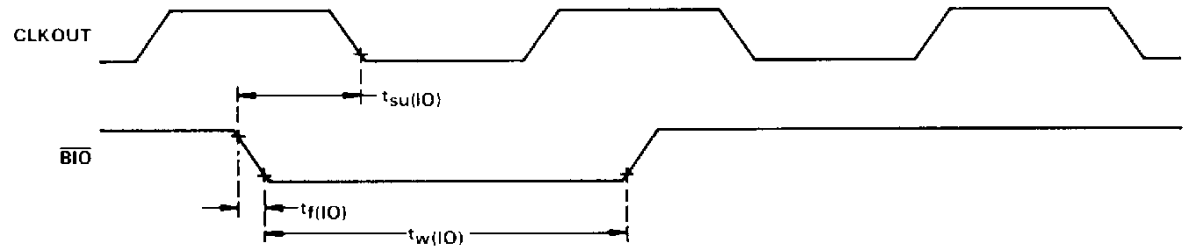
NOTES:
2. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.
6. $\overline{RS}$ forces $\overline{DEN}$ and $\overline{WE}$ high and tristates data bus D0 through D7. Program counter is synchronously cleared to zero after the next complete CLK cycle from $\overline{RS}$↓.
7. $\overline{RS}$ must be maintained for a minimum of five clock cycles
8. Resumption of normal program will commence after one complete CLK cycle from $\overline{RS}$↑.
9. Due to the synchronizing action on $\overline{RS}$, time to execute the function can vary dependent upon when $\overline{RS}$↓ or $\overline{RS}$↑ occur in the CLK cycle.
10. Diagram shown is for definition purpose only. $\overline{DEN}$ and $\overline{WE}$ are mutually exclusive.
11. During a write cycle, $\overline{RS}$ may produce an invalid write address.

I/O ($\overline{BIO}$) TIMING

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{f(IO)}$	Fall time $\overline{BIO}$			15	ns
$t_{w(IO)}$	Pulse duration $\overline{BIO}$	$t_{c(C)}$			ns
$t_{su(IO)}$	Setup time $\overline{BIO}$↓ before CLKOUT↓	50			ns

$\overline{BIO}$ timing



NOTE 2: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

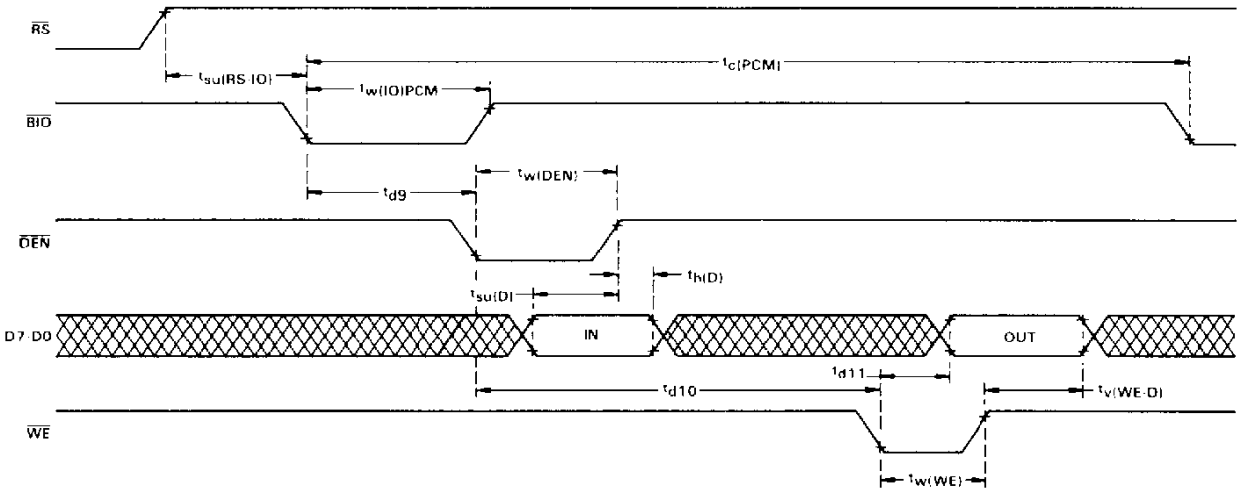
TMS320SA32 ADPCM SYSTEM TIMING

timing requirements over recommended operating conditions

		MIN	NOM	MAX	UNIT
$t_{c(PCM)}$	Synchronization cycle (PCM cycle)		125		μs
$t_{w(IO)PCM}$	Pulse duration $\overline{BIO}$	$7t_{c(C)}$		$550t_{c(C)}$	μs
t_{d9}	Delay time $\overline{BIO}$↓ to $\overline{DEN}$↓	$2t_{c(C)}$		$7t_{c(C)}$	μs
t_{d10}	Delay time $\overline{DEN}$↑ to $\overline{WE}$↓	$252t_{c(C)}$		$265t_{c(C)}$	μs
t_{d11}	Delay time $\overline{WE}$↑ to data bus valid	50 ns + $t_{c(C)}$		70 ns + $t_{c(C)}$	ns
$t_{h(D)}$	Hold time data bus valid after $\overline{DEN}$↑	0			ns
$t_{w(WE)}$	Pulse duration $\overline{WE}$	$\frac{1}{2}t_{c(C)}$ - 25		$\frac{1}{2}t_{c(C)}$ + 20	ns
$t_{v(WE-D)}$	Data bus valid after $\overline{WE}$↑	$\frac{1}{4}t_{c(C)}$ - 25		$\frac{1}{4}t_{c(C)}$	ns
$t_{su(RS-IO)}$	Setup time $\overline{RS}$↑ before $\overline{BIO}$↓	$t_{c(C)}$			ns
$t_{w(DEN)}$	Pulse duration $\overline{DEN}$	$\frac{3}{4}t_{c(C)}$ - 25		$\frac{3}{4}t_{c(C)}$ - 20	ns
$t_{su(D)}$	Setup time data bus valid to $\overline{DEN}$↑	50			ns

NOTE 12: For correct synchronization immediately after a reset action, $\overline{RS}$ must go high while $\overline{BIO}$ is high or until one $t_{c(C)}$ period after $\overline{BIO}$ goes low.

TMS320SA32 ADPCM system timing



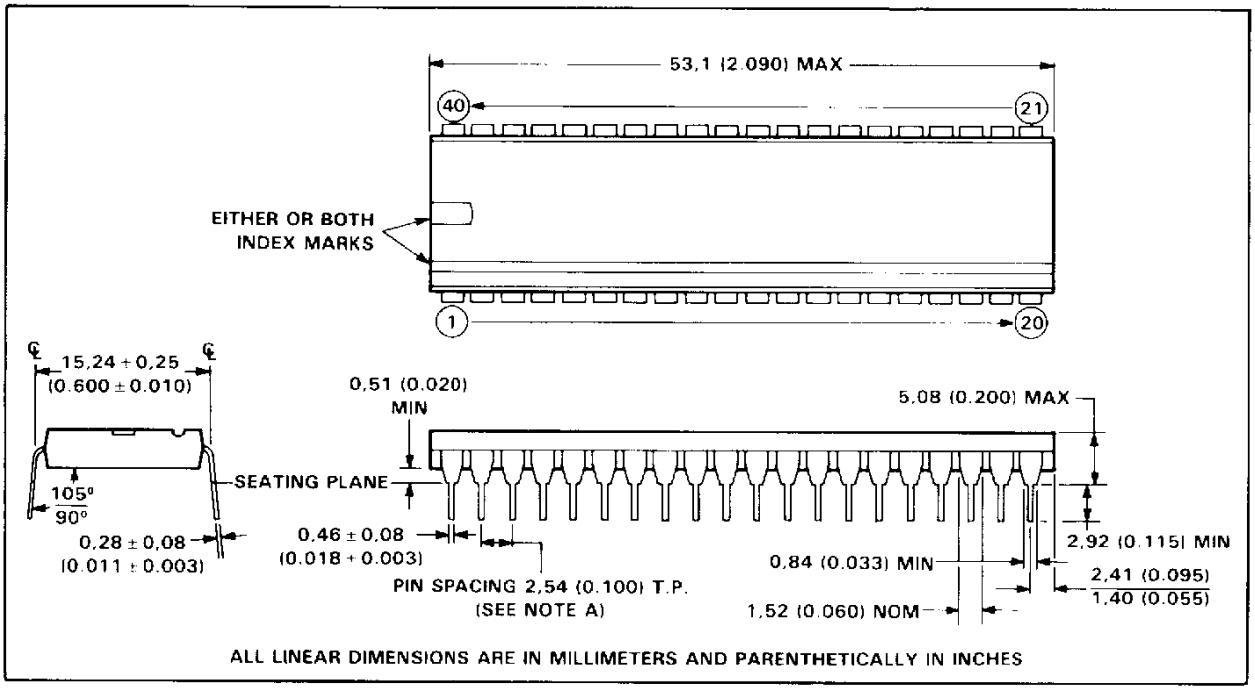
THERMAL DATA

thermal resistance characteristics

PACKAGE	$R_{\theta JA}$ (°C/W)	$R_{\theta JC}$ (°C/W)
40 pin plastic dual-in-line package	80	19

MECHANICAL DATA

40-pin plastic dual-in-line package



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.