Using the TMS320C6x McBSP as a High Speed Communication Port

APPLICATION REPORT: SPRA455

Shaku Anjanaiah

Digital Signal Processing Solutions
May 1998

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current and complete.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

TRADEMARKS

TI is a trademark of Texas Instruments Incorporated.

Other brands and names are the property of their respective owners.

CONTACT INFORMATION

US TMS320 HOTLINE	(281) 274-2320
US TMS320 FAX	(281) 274-2324
US TMS320 BBS	(281) 274-2323
US TMS320 email	dsph@ti.com

Contents

Figures

Tables

Using the TMS320C6x McBSP as a High Speed Communication Port

Abstract

This document describes how to use the two multi-channel buffered serial ports (McBSP) in the Texas Instruments (TI™) TMS320C6201 digital signal processor (DSP) as a high-speed data communication port.

Either one or both McBSPs in the C6201 can be connected to a McBSP of a different C6201 to serve as a high-speed data communication port. To achieve the maximum data rate, it is necessary to connect the two serial ports so that one device behaves both as a clock master and frame master. Master refers to a device that generates the required signal (such as clocks and frames). Using the set up described in this document, a maximum speed of 50 Mbps can be achieved with two McBSPs communicating with each other.

Product Support

Related Documentation

The following list specifies product names, part numbers, and literature numbers of corresponding TI documentation.

- *TMS320C6201 Digital Signal Processor* data sheet, March 1998, Literature number SPRS051C
- *TMS320C6201/C6701 Peripherals* Reference Guide, March 1998, Literature number SPRU190B

World Wide Web

Our World Wide Web site at **www.ti.com** contains the most up to date product information, revisions, and additions. Users registering with TI&ME can build custom information pages and receive new product updates automatically via email.

Email

For technical issues or clarification on switching products, please send a detailed email to **dsph@ti.com**. Questions receive prompt attention and are usually answered within one business day.

Design Problem

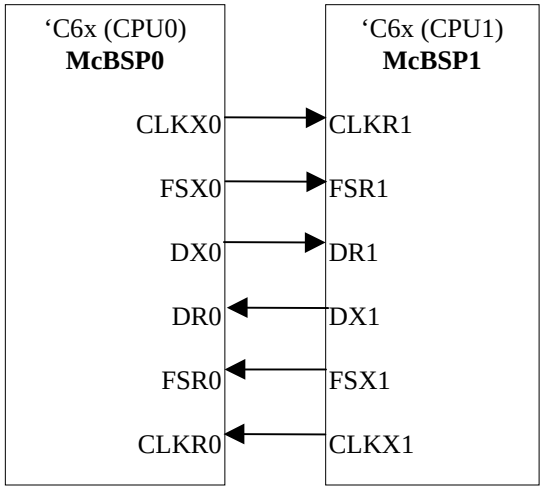
How can the two multi-channel buffered serial ports (McBSP) in the TMS320C6201 be used as a high-speed data communication port?

Solution

Either or both McBSPs in the C6201 can be connected to a McBSP of a different C6201 to serve as a high-speed data communication port. To achieve the maximum data rate, it is necessary to connect the two serial ports so that one device behaves both as a clock master and frame master. In other words, the McBSP transmitter that generates clocks for data transfer should also generate necessary frame synchronization signals. The other McBSP portion then acts as a slave awaiting these control signals from the master.

Figure 1 shows the block diagram of this arrangement. The transmit portion of McBSP0 of CPU0 is the master of clocks and frames to the receiver in McBSP1 of CPU1. This data transfer path is referred to as *mcbsp0to1*. Similarly, the McBSP1 transmitter is configured to be the clock and frame master to McBSP0 and is referred to as *mcbsp1to0*.

Figure 1. McBSP Connection for Maximum Data Rate



McBSP Register Configuration

The setup of bit-fields in the control registers for this operation is shown in Figure 2 through Figure 5 and listed in Table 1. Note that the master derives its clock from the CPU clock (CLKOUT1) with a divide ratio of 2. Since the master transmitter is responsible for generating bit clocks and frame synchronization signals, CLKX and FSX are programmed as outputs. The data delay between the FSX output and first data bit has to be a non-zero value because a data delay of zero does not provide maximum packet frequency. Therefore, both the transmitter and receiver are set for (R/X)DATDLY=1 in this example.

Figure 2. Receive Control Register (RCR)

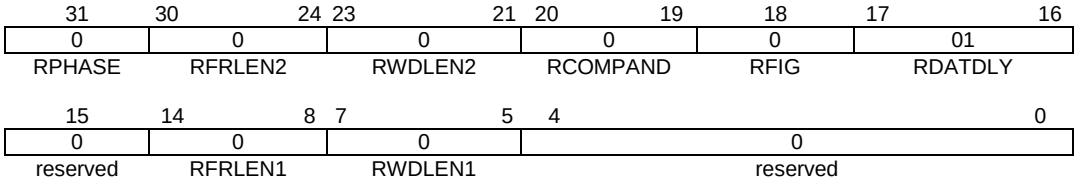


Figure 3. Transmit Control Register (XCR)

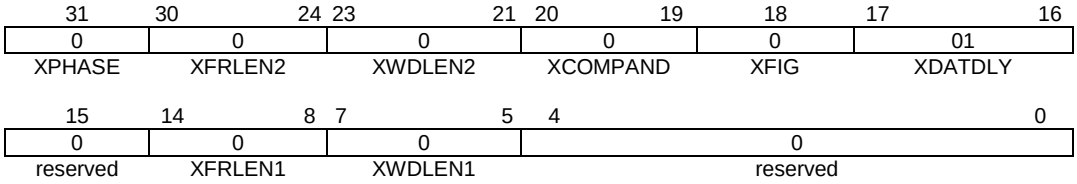


Figure 4. Sample Rate Generator Register (SRGR)

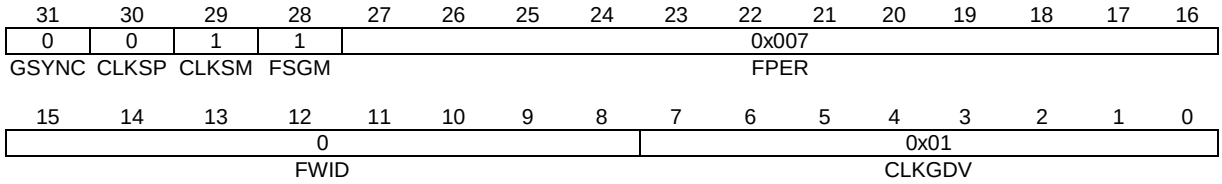


Figure 5. Pin Control Register (PCR)

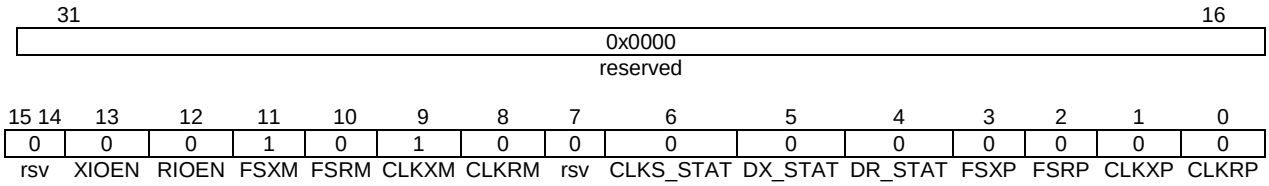


Table 1. Bit-Field Values for McBSP Registers

Register [bit-field #]	Bit-field Name	Value (in binary)	
		Master (Transmitter)	Slave (Receiver)
RCR[17:16]	RDATDLY	-	01 or 10
XCR[17:16]	XDATDLY	01 or 10	-
SRGR[29]	CLKSM	1	-
SRGR[28]	FSGM	1	-
SRGR[7:0]	CLKGDV	1	-
PCR[11]	FSXM	1	-
PCR[10]	FSRM	-	0(default)
PCR[9]	CLKXM	1	-
PCR[8]	CLKRM	-	0(default)

The bit-fields and registers not listed in Table 1 assume their default values. The user is responsible to set some of the register fields, such as number of phases, number of elements in a frame, frame length, and other parameters needed by the application.

The following macros initialize the registers to the values listed in Table 1. These macros are found in the TMS320C6x Peripheral Support Library at:

ftp://ftp.ti.com/pub/tms320bbs/c6xfiles/ devlib6x.zip

NOTE:

The following macros are only sample code. In a real application, you might want to write the initialization value to the register as a 32-bit word, which would include initialization of other parameters as well.

```
#include <regs.h>
#include <mcbsp.h>

/* Macros to initialize register bit-fields for the clock and frame MASTER*/
LOAD_FIELD (MCBSP_XCR_ADDR(0), DATA_DELAY1, XDATDLY, XDATDLY_SZ);
/* Set transmitter for 1-bit data delay */

LOAD_FIELD (MCBSP_SRGR_ADDR(0), CLK_MODE_INT, CLKSM, 1);
/* Set clock source to be CPU clock */

LOAD_FIELD (MCBSP_SRGR_ADDR(0), FSX_FSG, FSGM, 1);
/* Set Frame Sync to be generated by sample rate generator */

LOAD_FIELD (MCBSP_SRGR_ADDR(0), 1, CLKGDV, 1);
/* Set CPU clock divide-down to 1 so that CLKG frequency is ((CPU
frequency)/2) */

LOAD_FIELD (MCBSP_PCR_ADDR(0), FSYNC_MODE_INT, FSXM, 1);
/* Set FSX to be an output thereby becoming a frame master */

LOAD_FIELD (MCBSP_PCR_ADDR(0), CLK_MODE_INT, CLKXM, 1);
/* Set CLKX to be an output thereby becoming a clock master */

/* Macros to initialize register bit-fields for the SLAVE */
LOAD_FIELD (MCBSP_RCR_ADDR(1), DATA_DELAY1, RDATDLY, RDATDLY_SZ);
            /* Set receiver for 1-bit data delay */
```

Timing Analysis

The parameters that need to be satisfied to achieve maximum data rate are listed in Table 2. CLKPER is the clock period of the master clock (in this case, CLKX0/1), which can be varied in the analysis to verify the frequency at which the design margins are met. Note that a board route delay of 1 ns or about 6 inches is considered for propagation delay from source to destination.

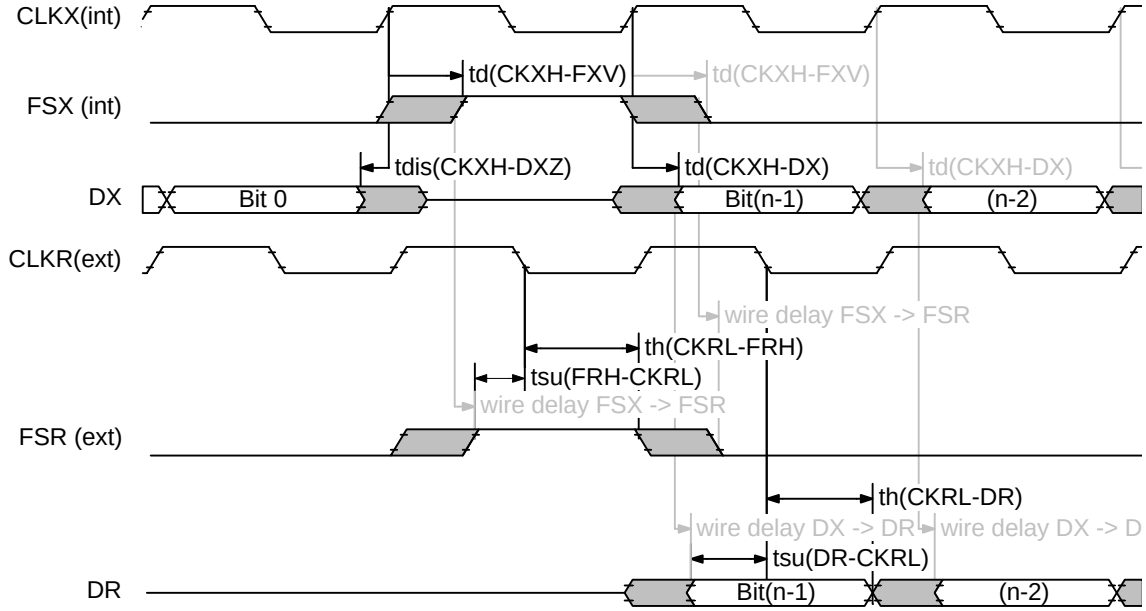
As shown in Table 2 and depicted in Figure 6, the delay parameters (switching characteristics) and constraint parameters (timing requirements) for the McBSP signals were met (no negative margins) at CLKPER of 20 ns. This means that the McBSP can have data rates up to 50 MHz when communicating to another McBSP (please refer to the note in the *Conclusion*).

Table 2. Parameter Values for Timing Requirements and Switching Characteristics at 50 MHz

Sl. No.	Parameter Type	Parameter Name	[Min, Max][1]	Margin	Description
1	Constraint	t_{su}(FRH-CKRL)	[4,]	<0>	Setup time, FSR valid to CLKR low
2	Constraint	t_h (CKRL-FRH)	[3,]	<7>	Hold time, FSR valid after CLKR low
3	Constraint	t_{su}(DRV-CKRL)	[1,]	<5>	Setup time, DR valid to CLKR low
4	Constraint	t_h (CKRL-DRV)	[4,]	<4>	Hold time, DR valid after CLKR low
5	Delay	t_d (CKXH-FXV)	[0, 6]		Delay time, FSX valid after CLKX low
6	Delay	t_{dis} (CKXH-DXZ)	[-2, 4]		Disable time, CLKX high to DX high impedance following last data bit.
7	Delay	t_d (CKXH-DX)	[-2, 4]		Delay time, DX valid after CLKX high
8	Variable	CLKPER	[20, 20]		Master clock period. Can be varied to satisfy parametric requirements.
9	Variable delay	t_{wd} (DX-DR)	[1, 1]		Wire delay from DX to DR. Set as per system needs.
10	Variable delay	t_{wd} (FSX-FSR)	[1, 1]		Wire delay from FSX to FSR. Set as per system needs.
11	Variable delay	t_{wd} (CLKX-CLKR)	[1, 1]		Wire delay from CLKX to CLKR. Set as per system needs.

[1] Numbers are from the *TMS320C6201 Digital Signal Processor* data sheet, March 1998.

Figure 6. Signal Relationship at 50 MHz Data Rate with (R/X)DATDLY=1



Conclusion

The two McBSPs can be used as a high-speed communication port at 50 MHz. This can be affected by:

- Method of data processing: For example, interrupt-driven transfer is slower than a DMA transfer. Therefore, the data transfer rate will have to be reduced so that all of the data is processed without missing any.
- Priority of data processing: DMA has a lower priority than the CPU, or the DMA channel used for servicing the McBSP has a lower priority than the other channels of the DMA. Thus, the time taken to service a write or read to/from the McBSP can be extended, causing data over-write and/or receiver full error condition. To avoid this, either the bit-clock rate should be reduced or special error-handling methods must be employed.

NOTE:
This application reportdiscusses only two TMS320C6x McBSPs communicating with each other. Higher speeds can be achieved if the McBSP is connected to any other device that meets the timing parameters listed in the *TMS320C6201 Digital Signal Processor* data sheet.