Migration Document

TMS320C6201 (Revision 2.x) to TMS320C6201B (Revision 3.x)

REFERENCE GUIDE: SPRA450

TMS320C6000 Digital Signal Processing

Digital Signal Processing Solutions
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TEXAS INSTRUMENTS

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Abstract

Samples of the Texas Instruments (TI™) TMS320C6201B DSP will be available in the second half of 1998, with volume production starting at the end of the year. The TMS320C6201B revision is manufactured using a 0.18-micron process compared to the currently available revision 2 that uses a 0.25-micron process. The use of a smaller process for the TMS320C6201B DSP will lead to significantly lower power dissipation as well as lower cost. The new data memory structure will allow simultaneous word accesses by both sides of the CPU and the DMA during a single cycle.

This document is intended to enable TMS320C6201 designers to anticipate the migration of their design to the TMS320C6201B and take advantage of the benefits of this revision.

The following lists the changes implemented by the TMS320C6201B compared to the TMS320C6201:

- Core voltage changed from 2.5V to 1.8V

  The new core architecture will be run at a lower voltage to provide less power consumption by the device.
- Dual blocks of Internal Data Memory

  64k-byte Data memory now divided into two 32K-byte blocks, with four 4K-byte banks per block.
- Thermal balls added for additional heat dissipation

  A 10 x 10 array of thermal balls are included on the underside of the device to be connected to the ground plane for additional heat dissipation.
- Voltage input to PLLV changed to 3.3V

The PLL circuit will be powered by the I/O voltage supply, rather than by the core voltage supply.

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Core Voltage (CVdd)

The voltage level of the ‘C6201 core has been changed from 2.5V to 1.8V. A new process will be used to manufacture the revision 3 silicon, which will reduce the physical size of the architecture. This change will allow more space for additional memory and peripherals on the device, and will also allow for less power consumption.

To provide a forward-compatible design that will function correctly for both revision 2 and revision 3, the core power supply must be designed to allow for an output voltage of either 2.5V or 1.8V. This may be accomplished by providing jumpers on the board, which select biasing resistors or capacitors for a linear regulator, or by providing jumpers to select a binary input to a switching regulator.

Data Memory

The internal data memory is now divided into two 32K-byte blocks, ranging from 0x80000000 to 0x80007FFF and from 0x80008000 to 0x80010000. With the division of the internal data memory into two blocks on revision 3 silicon, internal data may be accessed from different blocks without conflict, regardless of the banks accessed. Each block still contains four banks of 16-bit halfwords. Within a block the functionality is the same as on revision 2 silicon: both sides of the CPU (A or B) and the DMA may access different banks without conflict.

Thermal Balls

A 10x10 array of thermal balls has been added to the ‘C6201 to provide greater heat dissipation. Instead of requiring all of the heat to leave through the package/heat sink junction, more heat will be permitted to escape the device through the thermal ball array. The configuration of the thermal balls on the package is shown in Figure 1. The array of individual pads should be connected to the ground plane to channel the heat away from the device into the board. The pin assignments of the thermal balls are given in Table 1. To provide migration from revision 2 and revision 3 devices within a system, pads for the thermal ball array should be included in the design.

Figure 1. GGP 452-Pin Package (Bottom View)

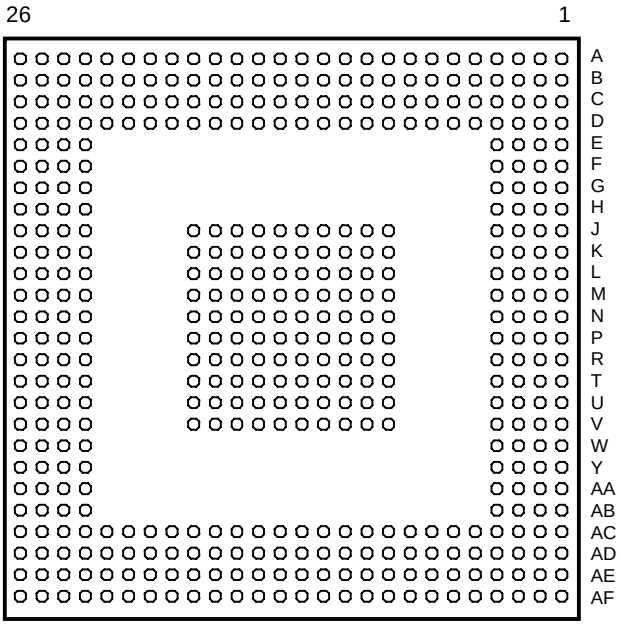

Table 1. Thermal Ball Pinout

Thermal Balls	PIN NO.
THB	J9
THB	J10
THB	J11
THB	J12
THB	J13
THB	J14
THB	J15
THB	J16
THB	J17
THB	J18
THB	K9
THB	K10
THB	K11
THB	K12
THB	K13
THB	K14
THB	K15
THB	K16
THB	K17
THB	K18
THB	L9
THB	L10
THB	L11
THB	L12
THB	L13
THB	L14
THB	L15
THB	L16
THB	L17
THB	L18
THB	M9
THB	M10
THB	M11

Thermal Balls	PIN NO.
THB	M12
THB	M13
THB	M14
THB	M15
THB	M16
THB	M17
THB	M18
THB	N9
THB	N10
THB	N11
THB	N12
THB	N13
THB	N14
THB	N15
THB	N16
THB	N17
THB	N18
THB	P9
THB	P10
THB	P11
THB	P12
THB	P13
THB	P14
THB	P15
THB	P16
THB	P17
THB	P18
THB	R9
THB	R10
THB	R11
THB	R12
THB	R13
THB	R14

Thermal Balls	PIN NO.
THB	R15
THB	R16
THB	R17
THB	R18
THB	T9
THB	T10
THB	T11
THB	T12
THB	T13
THB	T14
THB	T15
THB	T16
THB	T17
THB	T18
THB	U9
THB	U10
THB	U11
THB	U12
THB	U13
THB	U14
THB	U15
THB	U16
THB	U17
THB	U18
THB	V9
THB	V10
THB	V11
THB	V12
THB	V13
THB	V14
THB	V15
THB	V16
THB	V17
THB	V18

PLL Circuit

A slight modification affecting board design has been made to the external PLL filter circuit. The Voltage supply to the EMI filter will change from 2.5V (revision 2 CVdd) to 3.3V (DVdd). To facilitate this transition, a jumper should be place such that pin 1 of the EMI filter may connect to either power plane. The filter component values are currently not defined for revision 3 and may differ from the revision 2 values. The PLL filter circuit is shown in Figure 2.

Figure 2. Rev 3 PLL Circuit