TMS320C6201 Power Supply

APPLICATION REPORT: SPRA447

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TEXAS INSTRUMENTS

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Abstract

This document describes how to provide power to the Texas Instruments (TI™) TMS320C6201 digital signal processor (DSP). The TMS320C6201 DSP is a 3.3V I/O device with an internal core voltage level of 2.5V for rev 1 or 2 (1.8V for rev 3). To provide power to this device, separate supplies must be used for each of the two voltages and proper power sequencing to the device must be provided.

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Design Problem

How do I provide power to the TMS320C6201?

Solution

The TMS320C6201 DSP is a 3.3V I/O device with an internal core voltage level of 2.5V for rev 1 or 2 (1.8V for rev 3). To provide power to this device, separate supplies must be used for each of the two voltages and proper power sequencing to the device must be provided.

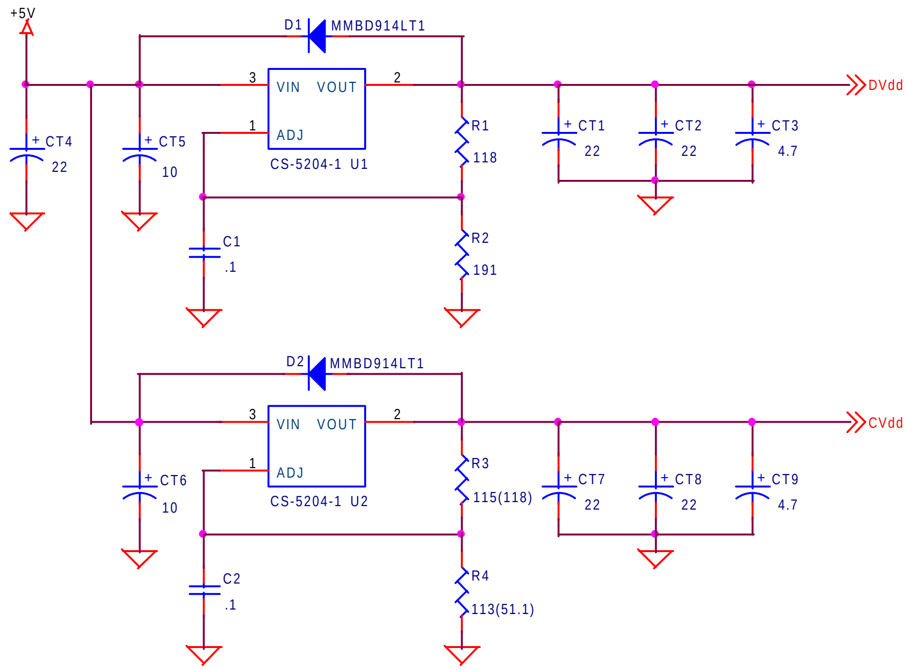
For power-up sequencing, ramp up the core (CVdd) supply first. Then ramp up the 3.3V I/O (DVdd) supply. For power-down sequencing, remove DVdd, then CVdd. The order is not mandatory but, if the DVdd must be brought up first, ensure that the 3.3V supply does not exceed the 2.5V by more than 2V, and the power up should take less than 25ms.

The reasoning behind the power sequencing is that essentially no harm will come to the device if the core is powered up and the I/O is not. There simply will be no input or output capability. If the I/O is powered up and the core is not, however, the transistors in the buffer/drivers will be driven while in an unknown state.

If this sequencing is not possible, it is permissible to ramp up both the supplies concurrently, provided that precautions are taken. The DVdd must not exceed the CVdd by more than 2V. Both power supplies should achieve 95% of their voltage level within a 25ms window. The 2.5V supply should be able to handle an output current of 3A (maximum consumption by the rev 2 device).

The simplest way to provide dual power to the DSP is to split a single source to two linear voltage regulator circuits (one regulating 3.3V and the other 2.5V). A sample circuit is shown in Figure 1 for a 5V source, using two 4A adjustable linear regulators from Cherry Semiconductor (part #CS-5204-1). Since the two regulated voltages are derived from the same source, power up sequencing should not be a problem. For component selection criteria, see the Cherry SC data sheet.

Figure 1. Power Supply Circuit for 'C6201[1]



The regulated voltage levels provided by the circuits shown in Figure 1 are determined by the resistor values. The output of each regulator is governed by the equation:

$$V_{OUT} = V_{REF}\, x \left(\frac{R1 + R2}{R1} \right) + I_{Adj}\, x R2$$

where V_{REF} is the voltage drop across R1 (1.25V fixed), and I_{Adj} is the current from the ADJ pin (typically 50µA).

If linear regulators are used in a system, large heat sinks will be required. This may make the design impractical, depending on the application.

A better, though more complicated solution, uses discrete regulators. Discrete regulators both emit a smaller amount of heat and can provide a fail-safe design.

[1] Numbers in parentheses indicate values used in a 1.8V core voltage design. If linear regulators are used, they need to be connected to large heat sinks.

To provide fail-safe operation of the device, power should be supplied so that if the core supply fails during operation, the I/O supply will be shut down as well. This can be accomplished using regulators having a “Power Good” output, whereby the device has a logical output indicating whether or not its regulated output is correct, and an “Inhibit” input, by which the device may be shut down by an external signal. The “Power Good” signal of the core supply should be tied directly to the “Inhibit” pin of the I/O supply. This configuration ensures that both power supplies will turn off if the core fails. In addition, an improper voltage level will not damage the device, and unknown outputs will not be driven from the device to the system. Figure 2 shows an example of this type of circuit using two Fairchild RC5050 [2] discrete voltage regulators.

Pins VID[4:0] of the regulator program the voltage level of the output. Table 1 lists the required pin connections for voltage levels of 3.3V, 2.5V, and 1.8V. For a complete list of possible voltage levels, see the Raytheon data sheet. In a design based on a ‘C6201 with a 2.5V core, VID[4:0] should be brought out to jumpers to allow forward compatibility. In this way, a 1.8V core device could be used in its place at a later time. The VID[4:0] pins for the 3.3V I/O may be hard-wired, as this voltage level will not change.

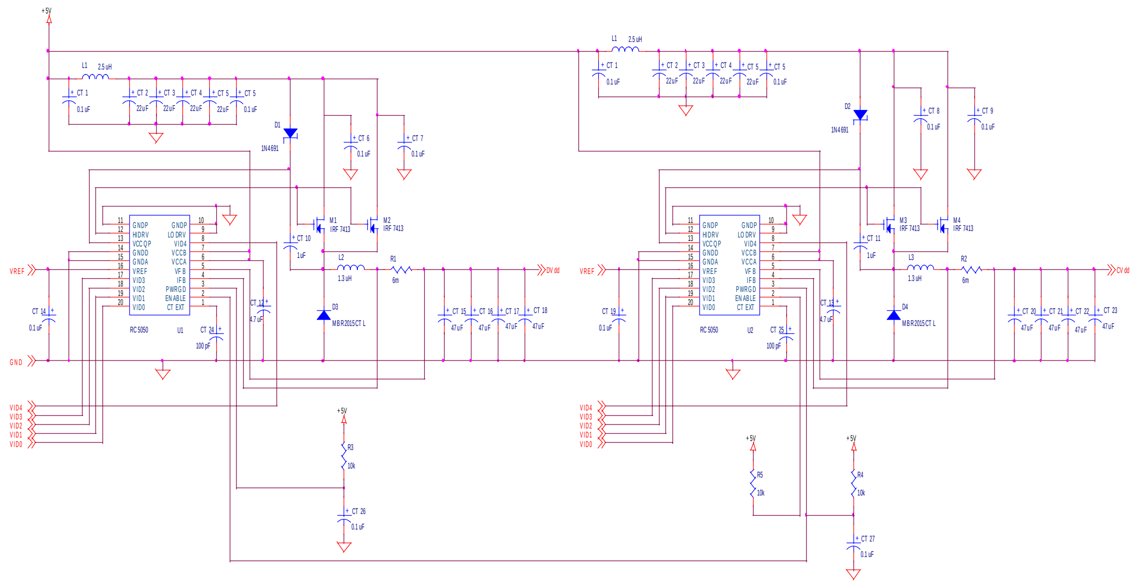
Table 1. VID[4:0] Codes[3] for Regulated Voltage Levels

Voltage Level	VID4	VID3	VID2	VID1	VID0
3.3	1	0	0	1	0
2.5	1	1	0	1	0
1.8	0	0	1	0	1

For detailed information on component selection for a design with the RC5050, please see the Fairchild data sheet.

[2] Similar devices are available from Elantec (#EL7571C and #EL7560C).
[3] 0 indicates that the pin is shorted to ground. 1 indicates that the pin is left unconnected.

Figure 2. Fail-Safe Power Supply Circuit



References

RC5050 Programmable DC-DC Converter for Low Voltage Microprocessors Data Sheet, Fairchild
http://www.fairchildsemi.com/cf/sales_contacts/

CS-5204-1 4A Adjustable, and 3.3V and 5V Fixed Linear Regulators Data Sheet, Cherry Semiconductor
http://www.cherrysemiconductor.com