TMS320C6x EMIF to External SDRAM/SGRAM Interface

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TMS320C6x EMIF to External SDRAM/SGRAM Interface

Abstract

Interfacing external SDRAM to the Texas Instruments (TI™) TMS320C6x digital signal processor (DSP) is simple compared to previous generations of TI DSPs because of the advanced External Memory Interface (EMIF). The EMIF is a glueless interface to a variety of external memory devices.

This application report describes the EMIF control registers and SDRAM/SGRAM signals along with SDRAM functionality, including functions supported by the EMIF and performance considerations when used with the EMIF.

General examples include each SDRAM configuration supported by the EMIF, including timing analysis. In addition, specific examples are provided using Texas Instrument's TMS626812B-10, Hitachi's HM5216165-10, and Samsung's KM416S4030B-8.

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Interface of EMIF with SDRAM and SGRAM

Fully Compatible Memory Types

The EMIF supports a glueless interface to 16 Mbit, 2 bank and 64 Mbit, 4 bank SDRAM, offering system designers an interface to high speed and high-density memory Table 1 lists the possible SDRAM configurations that are supported 100% by the EMIF.

Table 1. SDRAM Types Fully Supported by C6x

SDRAM Size (Mbits)	SDRAM Banks	SDRAM Width (bit)	Devices per CE Space	Memory Size per CE Space (Mbytes)
16	2	16	2	4
16	2	8	4	8
64	4	16	2	16

As Table 1 shows, the SDRAM supported by the EMIF is either 8 or 16 bits wide. However, the C6x has a 32 bit word size. Thus, four chips are used in parallel for the 8 bit SDRAM and two chips are used in parallel for the 16 bit SDRAM.

Table 2. Characteristics of Compatible Memory Types

SDRAM (Mbits)	Dimensions		Column Address	Row Address	Bank Select	Precharge
16	2 banks x 1 Mbit x 8	EMIF	EA10-EA2	SDA10, EA11-EA2	EA13	SDA10
		SDRAM	A8-A0	A10-A0	A11	A10
16	2 banks x 512 kbit x 16	EMIF	EA9-EA2	SDA10, EA11-EA2	EA13	SDA10
		SDRAM	A7-A0	A10-A0	A11	A10
64	4 banks x 1 Mbit x 16	EMIF	EA9-EA2	EA13, SDA10, EA11-EA2	EA15-EA14	SDA10
		SDRAM	A7-A0	A11-A0	A13-A12	A10

Table 3 summarizes the page characteristics of the fully supported SDRAM memory types and illustrates the EMIF to SDRAM pin mapping. The SDRAM uses addresses A[x:0] and these pins are mapped to EA[x+2:2] on the EMIF, since the EMIF assumes that SDRAM memory spaces are 32 bits wide. The four BE signals serve as the two LSBs of the external address. A key element of the supported SDRAM memory types is that A10 is always the precharge pin. To support this functionality, the EMIF's SDRAM interface uses a pin called SDA10 instead of EA12 in the pin map in order to support the necessary SDRAM operations. During row activate, SDA10 is logically equivalent to EA12. For other SDRAM operations, SDA10 is used as the precharge pin.

Forced Compatibility Memory Types

Table 3. SDRAM/SGRAM Types

SDRAM/ SGRAM Size (Mbits)	SDRAM Banks	SDRAM Width (bit)	Devices per CE Space	Memory Size per CE Space (Mbytes)
4 Mbit SDRAM	2	16	2	1 Mbyte
8 Mbit SGRAM	2	32	1	1 Mbyte
16 Mbit SGRAM	2	32	1	2 Mbyte

If a smaller amount of SDRAM is desired than offered with the fully compatible memory types, then 4 Mbit SDRAM or the SGRAM types could be useful. The advantages realized when using these memory types can be in either price or board space. Table 3 shows that the SGRAM types are 32 bits wide, and therefore only 1 device is needed per CE space, which reduces the amount of board space used. For a price advantage, 4Mbit SDRAM can be used, which still requires 2 devices per CE space.

Although SGRAM is not fully compatible with the C6x EMIF, the similarities between SGRAM and SDRAM can be exploited to force SGRAM to be functional with the EMIF. This is done by taking advantage of the identical page size between both 8 Mbit and 16 Mbit SGRAM and 16 bit wide SDRAM. This technique is also used with 4Mbit SDRAM. Table 4 shows the characteristics of 4Mbit SDRAM and 8 Mbit and 16 Mbit SGRAM.

Table 4. Characteristics of Forced Compatible Memory Types

SDRAM SGRAM	Dimensions		Column Address	Row Address	Bank Select	Precharge
4 Mbit SDRAM	2 banks x 128 kbit x 16	EMIF	EA9-EA2	SDA10, EA9 -EA2	EA11	SDA10
		SDRAM	A7-A0	A8-A0	A9	A8
8 Mbit SGRAM	2 banks x 128 kbit x 32	EMIF	EA9-EA2	SDA10, EA9-EA2	EA11	SDA10
		SDRAM	A7-A0	A8-A0	A9	A8
16 Mbit SGRAM	2 banks x 256 kbit x 32	EMIF	EA9-EA2	SDA10, EA10-EA2	EA11	SDA10
		SDRAM	A7-A0	A9-A0	A10	A9

As Table 4 shows, the column addressing of each of these memory types is identical to the column addressing used with the 16 bit wide fully compatible memory types. As discussed later, the only control that specifies the type of SDRAM in use is a control bit in the EMIF SDRAM Control Register that specifies either 8 bit wide or 16 bit wide SDRAM. If 8 bit wide SDRAM is specified, then a column address using the lower order 9 bits is used and the row address is shifted accordingly. If 16 bit wide SDRAM is specified, then the lower order 8 bits are used for the column address and the row address is shifted accordingly. Since the memory types in Table 4 all have 8 bit column addressing schemes, a 16 bit wide interface can be forced to work with these memory types.

A problem arises due to the different precharge and bank select pins used. For the memories in Table 4, either A8 or A9 is the precharge pin on the SDRAM/SGRAM and either A9 or A10 is the bank select pin. In order to force compatibility with SDRAM operations, SDA10 must still be used as the precharge signal from the EMIF. During row addressing, however, SDA10 is logically equivalent to EA12. For the 4 Mbit SDRAM and 8 Mbit SGRAM (which have identical page characteristics), EA10 is not used and thus there is a hole in the memory map, effectively giving an image of the previous 64 kbytes. For the 16 Mbit SGRAM, the hole is eliminated since every pin is used. This is summarized in Table 5 and Table 6.

Table 5. 4 Mbit SDRAM / 8 Mbit SGRAM Memory Map

1st 64 kwords	Bank 0, bottom half
Image of 1st 64 kwords	
2nd 64 kwords	Bank 1, bottom half
Image of 2nd 64 kwords	
3rd 64 kwords	Bank 0, top half
Image of 3rd 64 kwords	
4th 64 kwords	Bank 1, top half
Image of 4th 64 kwords	

Table 6. 16 Mbit SGRAM Memory Map

1st 128 kwords	Bank 0, bottom half
2nd 128 kwords	Bank 1, bottom half
3rd 128 kwords	Bank 0, top half
4th 128 kwords	Bank 1, top half

Physical Interface

The following figures describe the EMIF SDRAM interface. The two possible 16 Mbit SDRAM interfaces are given in Figure 1 and Figure 2; the 64 Mbit interface is shown in Figure 3. Table 7 describes the pin connection and related signals specific to SDRAM operation.

The forced compatible memory types, 4 Mbit SDRAM, and 8 Mbit and 16 Mbit SGRAM, are shown in Figure 4, Figure 5, and Figure 6, respectively.

Figure 1. EMIF to 16 Mbit SDRAM Interface Using Two 16 Bit Wide Chips

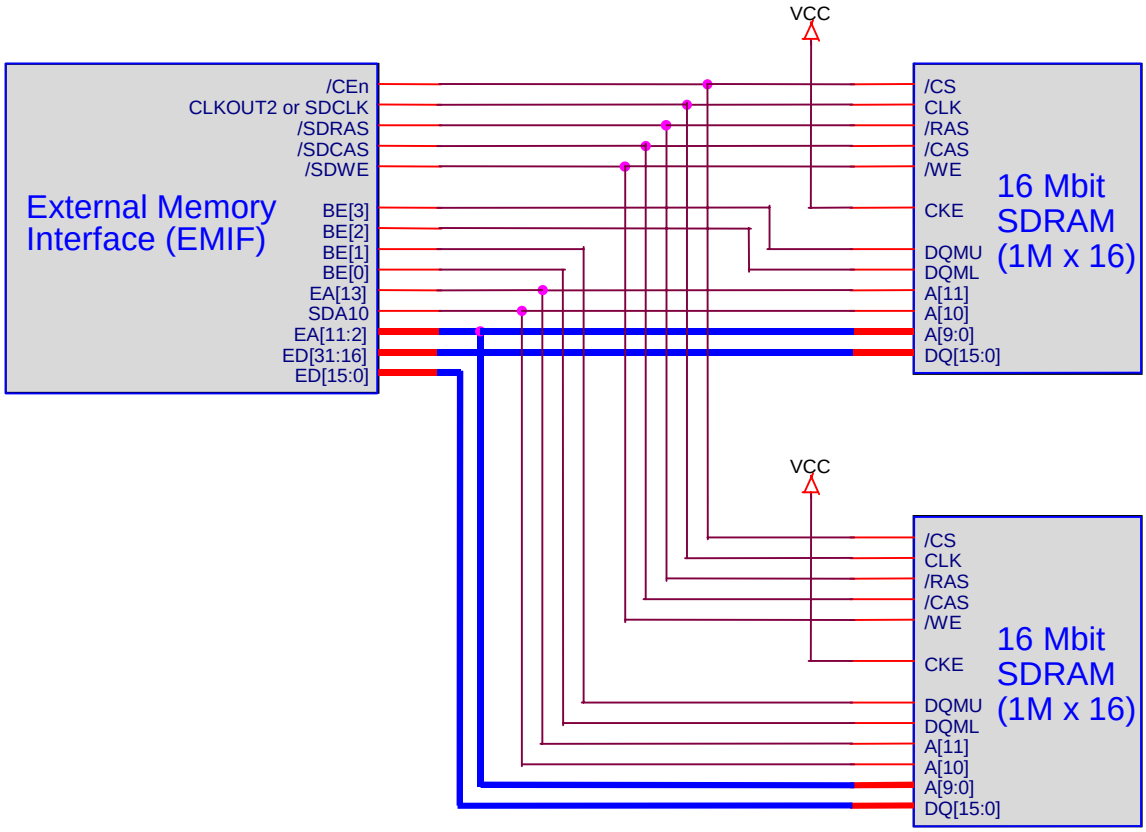


Figure 2. EMIF to 16 Mbit SDRAM Interface Using Four 8 Bit Wide Chips

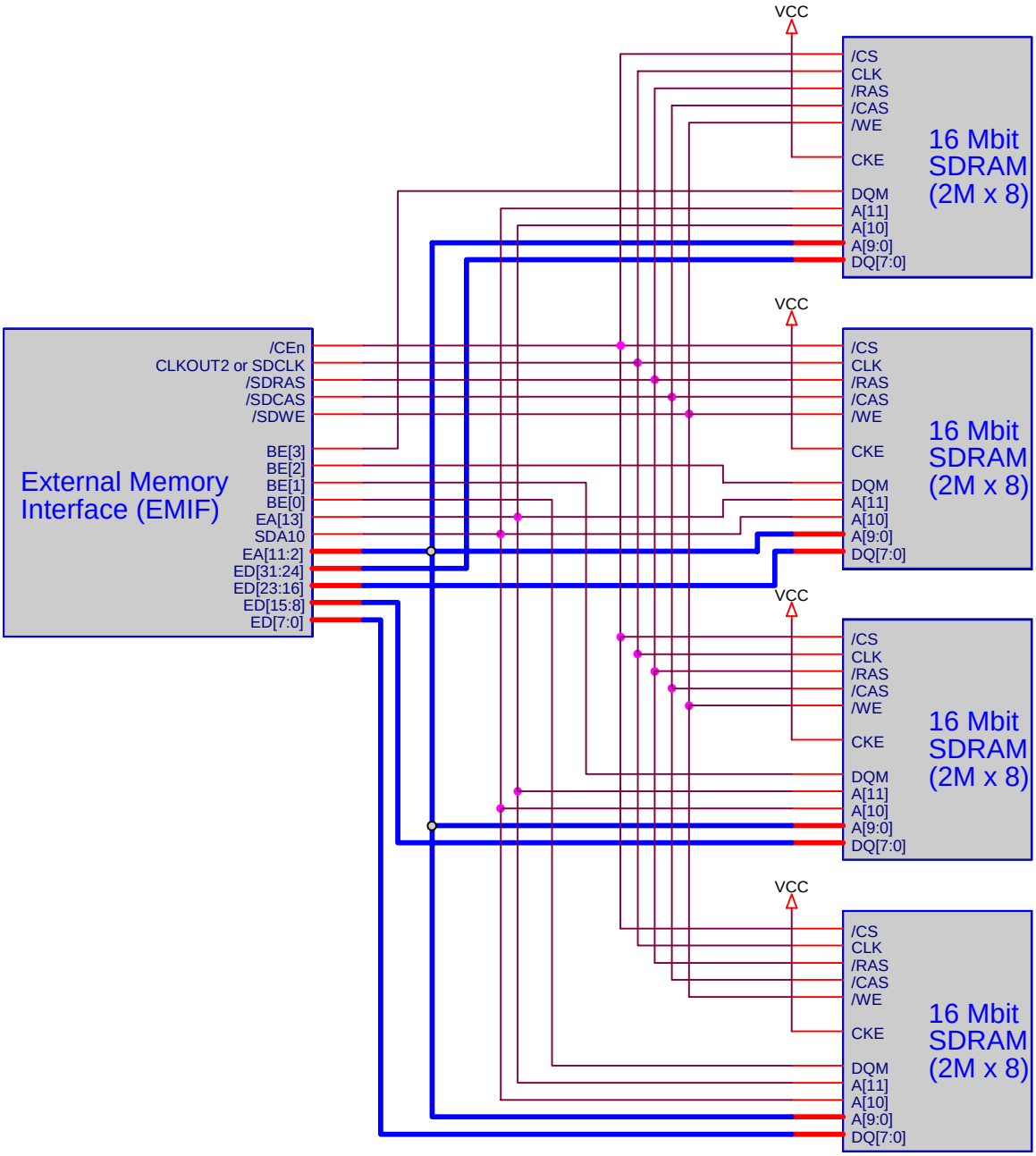


Figure 3. EMIF to 64 Mbit SDRAM Interface Using Two 16 Bit Wide Chips

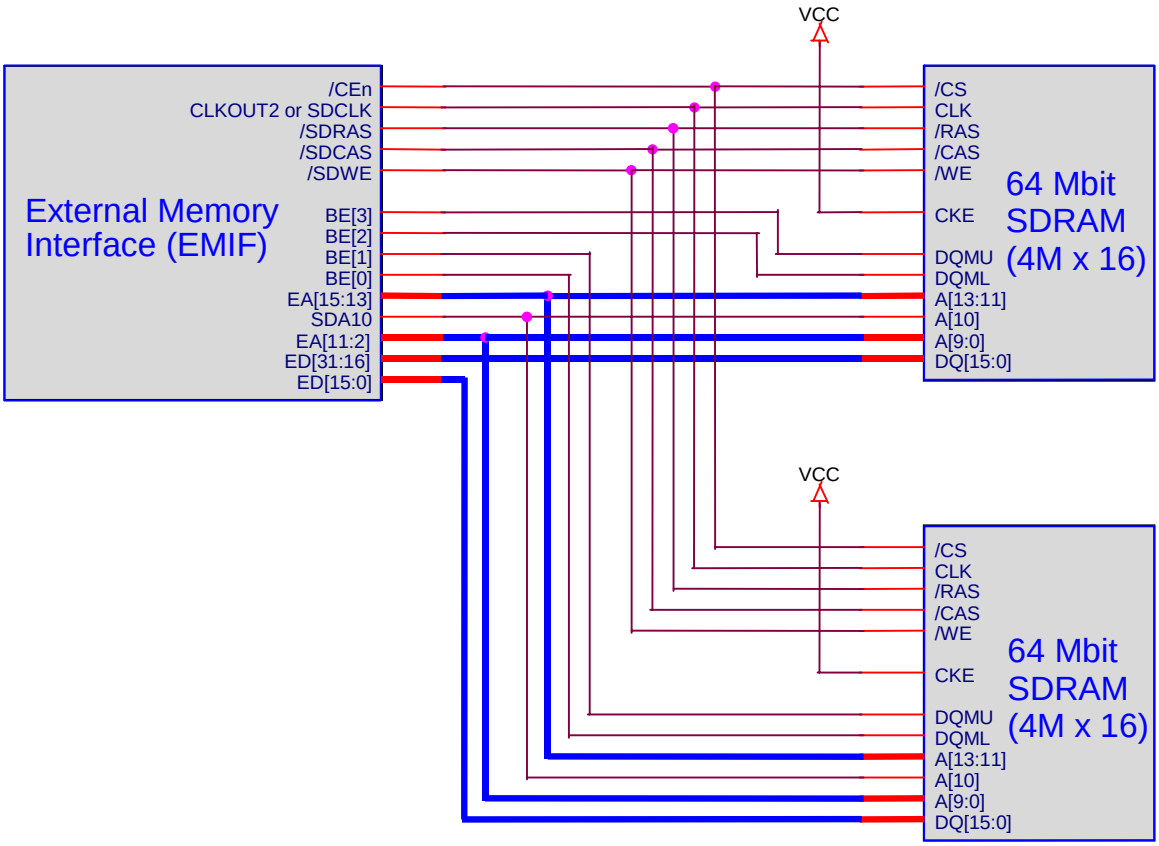


Figure 4. EMIF to 4 Mbit SDRAM Interface Using Two 16 Bit Wide Chips

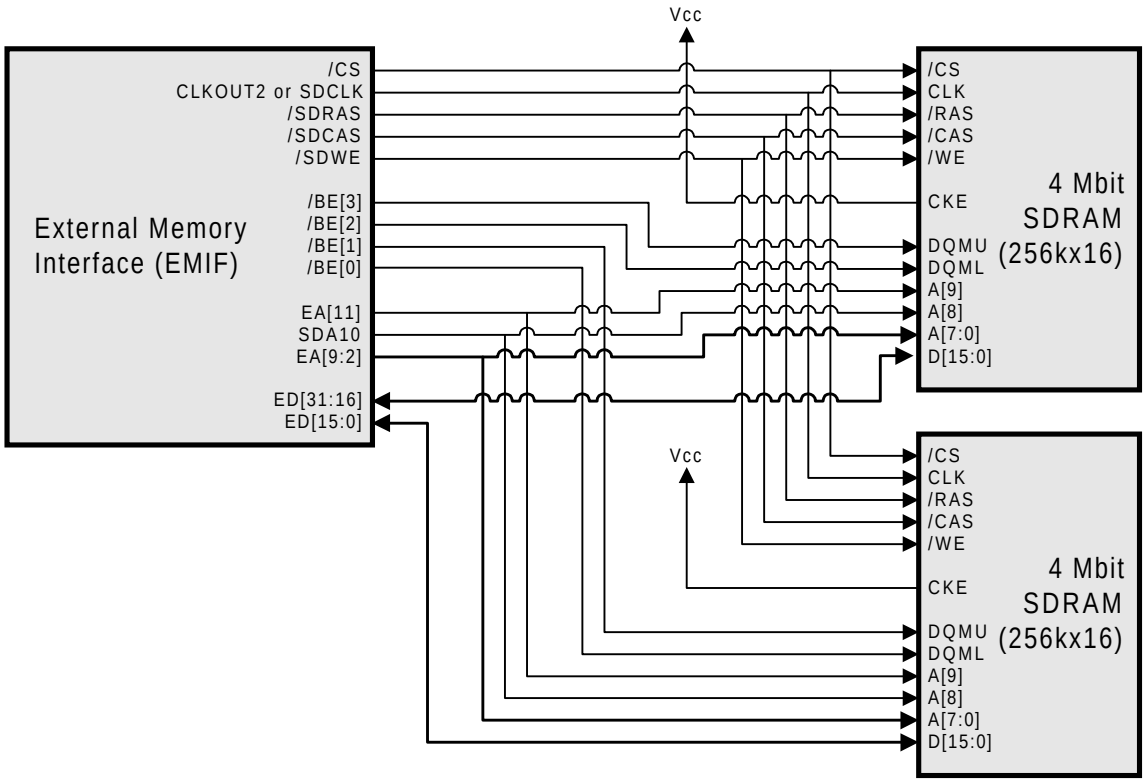


Figure 5. EMIF to 8 Mbit SGRAM

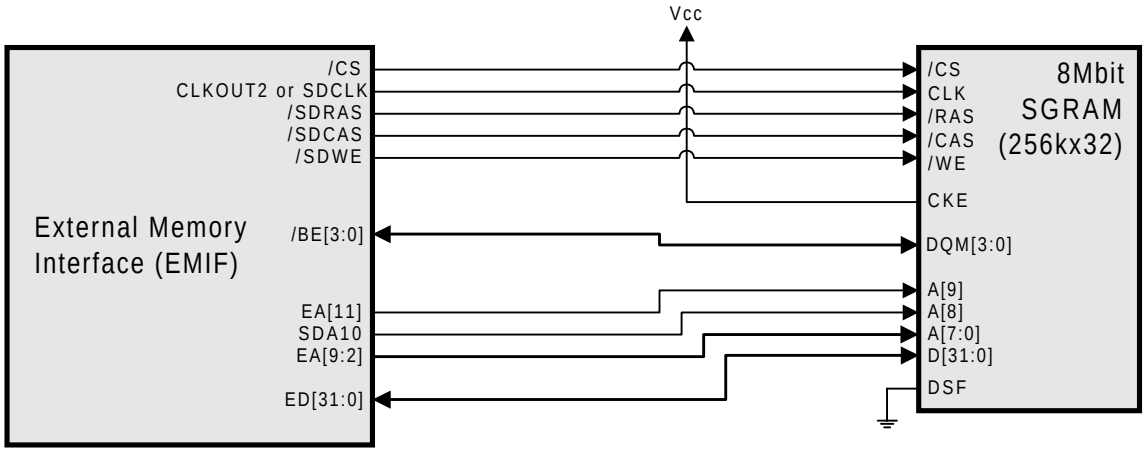
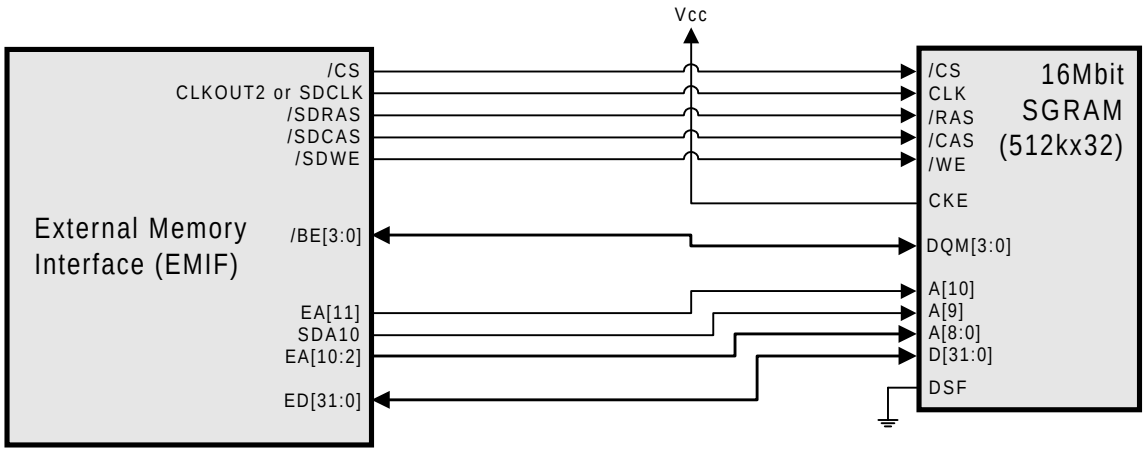


Figure 6. EMIF to 16 Mbit SGRAM



Overview of EMIF

EMIF Signal Descriptions

Figure 7 shows a block diagram of the EMIF. As the figure shows, the EMIF is the interface between external memory and the other internal units of the ‘C6x. The interface with the processor is provided via the DMA controller, Program Memory Controller, and the Data Memory Controller. The signals described in Table 7, however, focus on the SDRAM interface and the shared interface signals.

Figure 7. EMIF Block Diagram

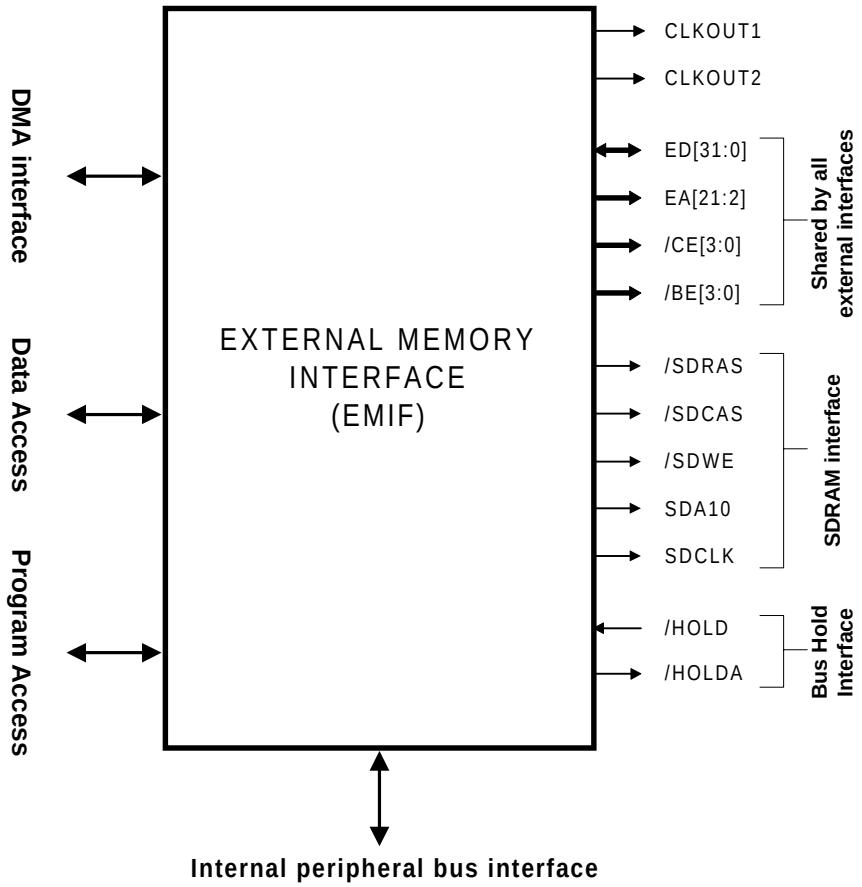


Table 7. EMIF Signal Descriptions: Shared Signals and SDRAM/SGRAM Signals

EMIF Signal	SDRAM Signal	(I/O/Z)	Description
ED[31:0]	DQ[x:0]	I/O/Z	Data I/O. 32-bit data input/output from external memories and peripherals.
EA[15:2]	A[13:0]	O/Z	External Address output. Drives bits 15-2 of the byte address. EA15 maps to A13, EA14 maps to A12, … , EA2 maps to A0, excluding EA12, which is replaced with SDA10.
/CE0, /CE2, or /CE3	/CS	O/Z	External /CE0 Chip Select. Active low chip select for CE space 0, 2, or 3.
/BE[3:0]	DQM[3:0]	O/Z	Byte Enables. Active low byte strobes. Individual bytes and halfwords can be selected for both read and write cycles. Decoded from 2 LSBs of the byte address.
/SDRAS	/RAS	O/Z	Row Address Strobe. Active low /RAS for SDRAM memory interface.
/SDCAS	/CAS	O/Z	Column Address Strobe. Active low /CAS for SDRAM memory interface.
/SDWE	/WE	O/Z	Write Enable. Active low /W for SDRAM memory interface.
SDA10	A10	O/Z	SDRAM A10 Address Line. Address line/auto-precharge disable for SDRAM memory. Serves as a row address bit (logically equivalent to EA12) during ACTV commands and also disables the auto-pre-charging function of SDRAM during read or write operations.
SDCLK	CLK	O/Z	Clock. SDRAM interface clock- one half the CPU clock rate. Equivalent to CLKOUT2.
/HOLD	-	I	Active-low external bus hold (3-state) request.
/HOLDA	-	O	Active-low external bus hold acknowledge.
-	CKE		CKE clock enable. Tied active high when interface to EMIF to always enable clocking.
-	DSF		Define Special Function. Tied low to disable special graphic commands of SGRAM. With this tied low, SGRAM behaves exactly as standard SDRAM.

EMIF Registers

Control of the EMIF and the memory interfaces it supports is maintained through a set of memory mapped registers within the EMIF. The memory mapped registers are shown in Table 8.

Table 8. EMIF Memory Mapped Registers

Byte Address	Name
0x01800000	EMIF Global Control
0x01800004	EMIF CE1 Space Control
0x01800008	EMIF CE0 Space Control
0x0180000C	Reserved
0x01800010	EMIF CE2 Space Control
0x01800014	EMIF CE3 Space Control
0x01800018	EMIF SDRAM Control
0x0180001C	EMIF SDRAM Refresh Period

EMIF Global Control Register

The EMIF Global Control Register configures parameters common to all the CE spaces (see Figure 8). Table 9 only lists those parameters that are relevant for use with SDRAM.[1]

Figure 8. EMIF Global Control Register Diagram

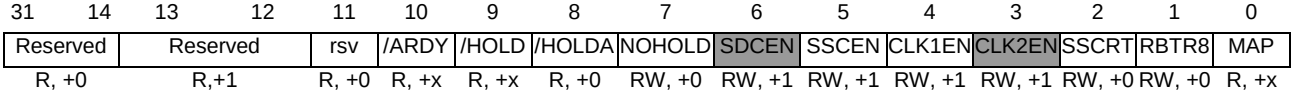


Table 9. EMIF Global Control Register Bit Field Description

Field	Description
SDCEN	SDCLK enable
	SDCEN =0, SDCLK held high
	SDCEN =1, SDCLK enabled to clock
CLK2EN	CLKOUT2 enable
	CLK2EN=0, CLKOUT2 held high
	CLK2EN=1, CLKOUT2 enabled to clock

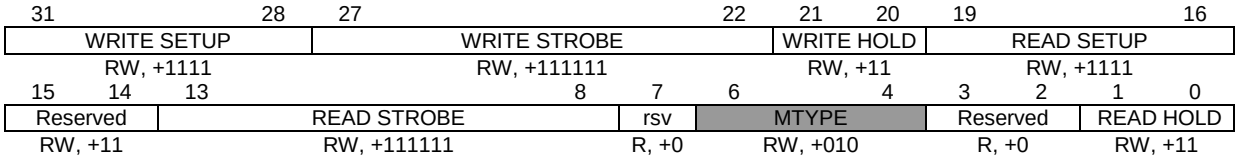
[1] For a description of all of the parameters of the EMIF Global Control Register, see the *TMS320C6201/6701 Peripherals Reference Guide*.

CE Space Control Registers

The four CE Space Control Registers correspond to the four CE spaces supported by the EMIF (see Figure 9). The MTYPE field identifies the memory type for the corresponding CE space. If MTYPE selects SDRAM or SBSRAM, the remaining fields in the register do not apply.

For a CE space to be configured for SDRAM, the MTYPE field should be set to 011. Also, SDRAM can not be used in CE1.

Figure 9. EMIF CE(0/1/2/3) Space Control Register Diagram



SDRAM Control Register

The SDRAM Control Register controls SDRAM parameters for all CE spaces that specify an SDRAM memory type in the MTYPE field of its associated CE Space Control Register (see Figure 10). Since the SDRAM Control Register controls all SDRAM spaces, each space ***must*** contain SDRAM with the same timing and page characteristics.

Figure 10. EMIF SDRAM Control Register

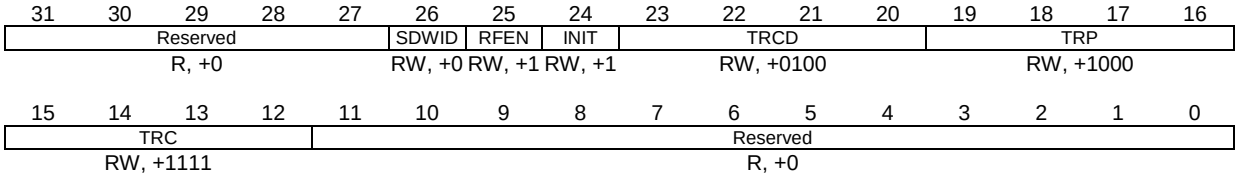


Table 10. EMIF SDRAM Control Register Bit Field Description

Field	Description
TRC	Specifies t_{RC} value of the SDRAM in CLKOUT2 cycles. TRC = (t_{RC} / CLKOUT2) - 1.
TRP	Specifies t_{RP} value of the SDRAM in CLKOUT2 cycles. TRP = (t_{RP} / CLKOUT2) - 1.
TRCD	Specifies t_{RCD} value of the SDRAM in CLKOUT2 cycles. TRCD = (t_{RCD} / CLKOUT2) - 1.
INIT	Forces an initialization of all SDRAM present. INIT = 0, no effect. INIT = 1, initialize SDRAM in each CE space configured for SDRAM.
RFEN	Refresh Enable. RFEN = 0, SDRAM refresh disabled. RFEN = 1, SDRAM refresh enabled.
SDWID	SDRAM Width Select. SDWID=0, Each External SDRAM Space Consists of four 8 bit SDRAMs with a page size of 512 words. SDWID=1, Each External SDRAM Space Consists of two 16 bit SDRAM with a page size of 256 words.

SDRAM Refresh Period

The SDRAM Refresh Period controls the refresh PERIOD for SDRAM in terms of CLKOUT2 cycles (one half the CPU clock rate). When the counter reaches zero, it is automatically reloaded with the PERIOD.

Figure 11. EMIF SDRAM Refresh Period

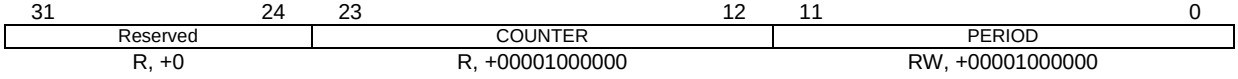


Table 11. EMIF SDRAM Refresh Period Bit Field Description

Field	Description
PERIOD	Refresh period/CLKOUT2
COUNTER	Current value of the refresh counter.

SDRAM

SDRAM Commands

The EMIF supports the SDRAM commands described Table 12. These commands are detailed in the following sections.

Table 12. EMIF SDRAM Commands

Command	Function
DCAB	Deactivate (also known as pre-charge) all banks
ACTV	Activate the selected bank and select the row
READ	Input the starting column address and begin the read operation
WRT	Input the starting column address and begin the write operation
MRS	Mode Register Set, configures SDRAM mode register
REFR	Auto refresh cycle with internal address

Table 13. Truth Table for SDRAM Commands

Command	/CS (/CE)[2]	/RAS (/SDRAS)	/CAS (/SDCAS)	/W (/SDWE)	A13-A11; A9-A0 (EA15-13; EA11-EA2)	A10 (SDA10)
DCAB	L	L	H	L	X	H
ACTV	L	L	H	H	Bank Select/Row Address	Row Address
READ	L	H	L	H	Column Address	L
WRT	L	H	L	L	Column Address	L
MRS	L	L	L	L	Mode	X
REFR	L	L	L	H	X	X

[2] The designator in parentheses is the EMIF signal; the preceding designator is the SDRAM signal it is connected to.

Timing Requirements

Five SDRAM timing parameters decouple the EMIF from SDRAM speed limitations. Three of these parameters are programmable via the EMIF SDRAM control register; the remaining two are assumed to be static values as shown in Table 14. The three programmable values assure that EMIF control of SDRAM obeys these minimum timing requirements. Consult the manufacturer's data sheet for the particular SDRAM.

Table 14. SDRAM Timing Parameters

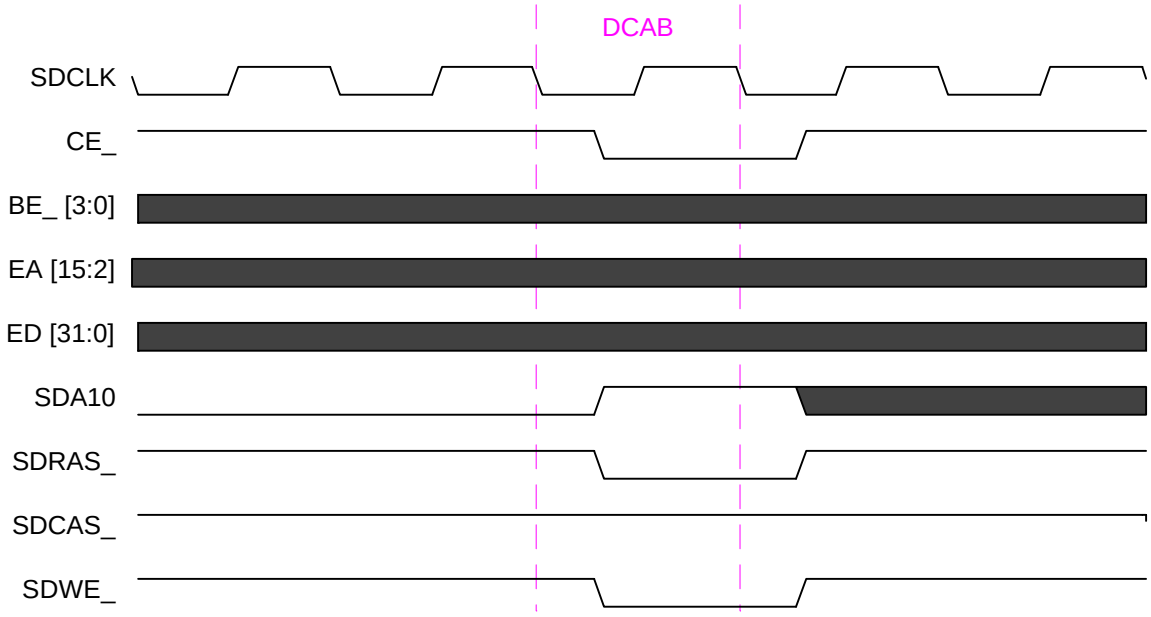
Parameter	Description	Value in CLKOUT2 Cycles
t_{RC}	REFR command to ACTV, MRS, or subsequent REFR command	(TRC + 1) * CLKOUT2
t_{RCD}	ACTV command to READ or WRT command	(TRCD + 1) * CLKOUT2
t_{RP}	DCAB command to ACTV, MRS, or REFR command	(TRP + 1) * CLKOUT2
t_{RAS}	ACTV command to DCAB command	7 * CLKOUT2
t_{nEP}	Overlap between read data and a DCAB command	2 * CLKOUT2

Note: Cycles shown in the following timing diagrams have TRCD = 10b (t_{RCD} = 3 CLKOUT2 cycles).

Deactivate (DCAB)

The DCAB command is issued to close the active page of memory. The SDRAM deactivation (DCAB) is performed after a hardware reset or when INIT=1 in the EMIF SDRAM Control Register. This cycle is also required by the SDRAMs prior to REFR, MRS, and when a page boundary is crossed. During the DCAB command, SDA10 is driven high to ensure that all SDRAM banks are deactivated.

Figure 12. SDRAM Deactivation



SDRAM DCAB COMMAND

Activate (ACTV)

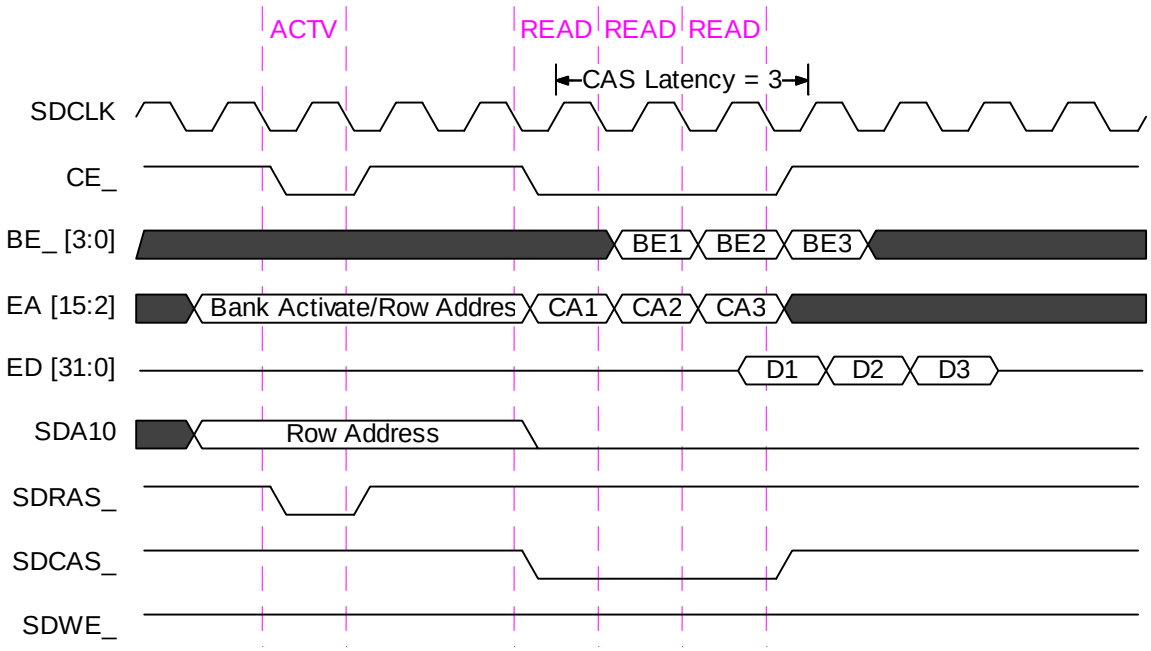
The Activate command is issued before a read or write to a new row of SDRAM. This command opens up a page of memory, allowing future accesses (reads or writes) with a minimum latency. As seen in Figure 13 and Figure 14, when an ACTV command is issued by the EMIF, a delay of t_{RCD} is incurred before a read or write command is issued (assume t_{RCD} = 3 CLKOUT2 cycles.) Reads or writes to the currently active row and bank of SDRAM are able to achieve much higher throughput than reads or writes to random areas, since every time a new page is accessed, the ACTV command must be issued.

SDRAM Read (READ)

During a SDRAM read the selected bank is activated with the row address during the ACTV command. In this example, three read commands are performed to three different column addresses in the same page. The EMIF uses a CAS latency of 3 and a burst length of 1. The 3 cycle read latency causes data to appear 3 cycles after the corresponding column address, as shown in Figure 13.

If a Refresh cycle or an access to a different page of memory is required, then following the last column access, a DCAB cycle is performed to deactivate the bank. An idle cycle is inserted between the final read command and the DCAB command to meet SDRAM timing requirements. Note that the transfer of data completes during and past the DCAB command. If no new access is pending, the DCAB command is not performed until such time that the page information becomes invalid.

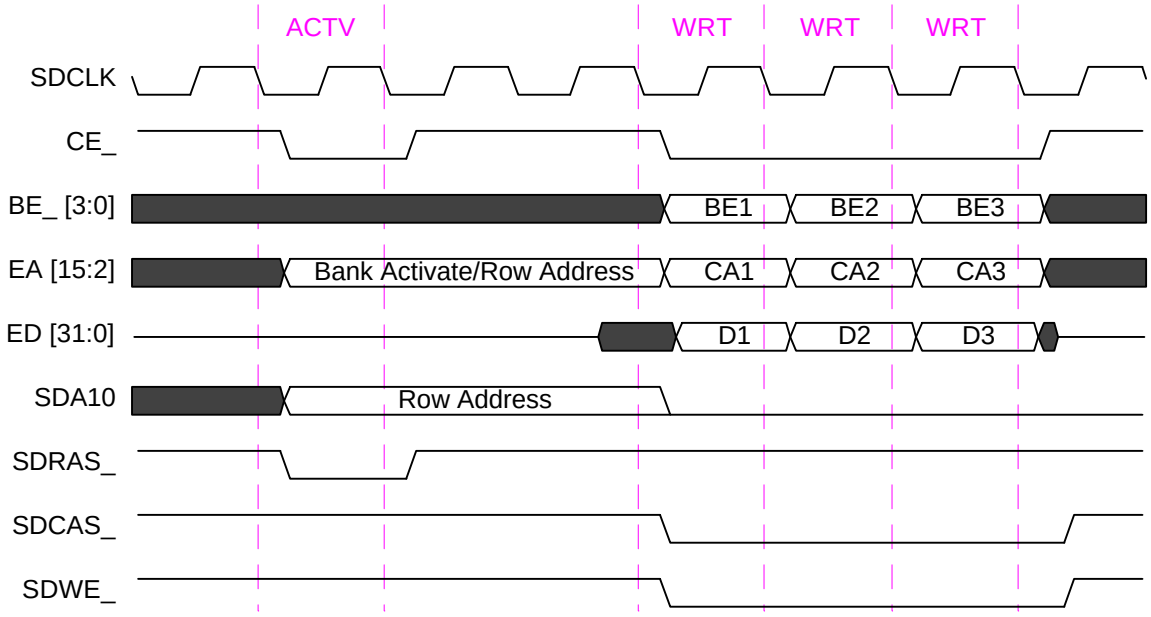
Figure 13. SDRAM Read - CAS Latency 3



SDRAM Write (WRT)

All SDRAM writes have a burst length of 1. The bank is activated with the row address during the ACTV command. There is no latency on writes so data is output on the same cycle as the column address. Byte and halfword writes are enabled via the appropriate DQM inputs. Following the final write command, an idle cycle is inserted to meet SDRAM timing requirements. If required, the bank is then deactivated with a DCAB command and the memory interface can begin a new page access. If no new access is pending, or if an access is pending to the same page, the DCAB command is not performed until such time that the page information becomes invalid.

Figure 14. SDRAM Burst Length 1 Write



3 SDRAM WRT COMMANDS

Mode Register Set (MRS)

The Mode Register is a register located in the external SDRAM memory which dictates its operating characteristics. When initializing SDRAM, the EMIF must set this register to the value described here before normal read or write accesses can occur.

The EMIF automatically performs a DCAB command followed by a MRS command whenever the INIT field in the EMIF SDRAM Control Register is set. INIT can be set by device reset, or by a user write. Like DCAB and REFR commands, MRS commands are sent to all CE spaces configured as SDRAM. Following the MRS cycle, the INIT bit is cleared to prevent multiple MRS cycles. The EMIF always uses a Mode Register value of 0x0030 during an MRS command. Figure 15 shows the mapping between mode register bits, EMIF pins, and the mode register value.

Table 15 shows the SDRAM configuration selected by this mode register value.

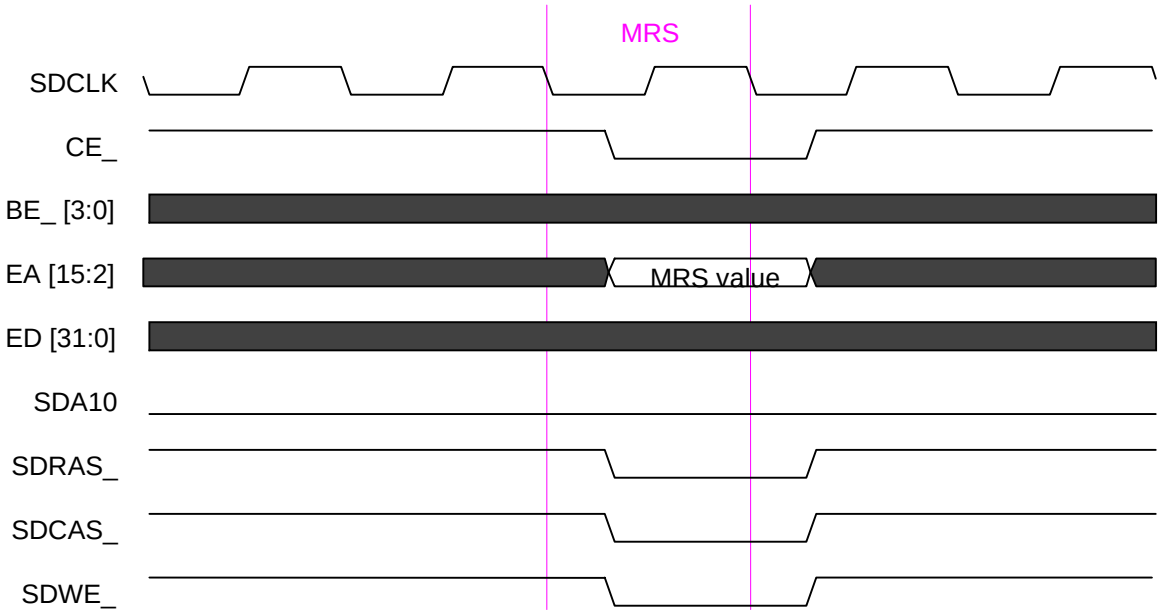
Figure 15. Mode Register Value

Mode Register Bit	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMIF Pins	EA15	EA14	EA13	SDA10	EA11	EA10	EA9	EA8	EA7	EA6	EA5	EA4	EA3	EA2
Field	Reserved				Write Burst Length	Reserved		Read Latency			S/I	Burst Length		
Value	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Table 15. Implied SDRAM Configuration by MRS Value

Field	Selection
Write Burst Length	1
Read Latency	3
Serial/Interleave Burst Type	Serial
Burst Length	1

Figure 16. SDRAM Mode Register Set: MRS Command



SDRAM MRS

Refresh

The RFEN bit in the SDRAM Control Register (Figure 10) selects the SDRAM refresh mode of the EMIF. A value of 0 in the RFEN field disables all EMIF refreshes; the user must insure that refreshes are implemented in an external device. A value of 1 in the RFEN field enables the EMIF to perform refreshes of SDRAM as described below.

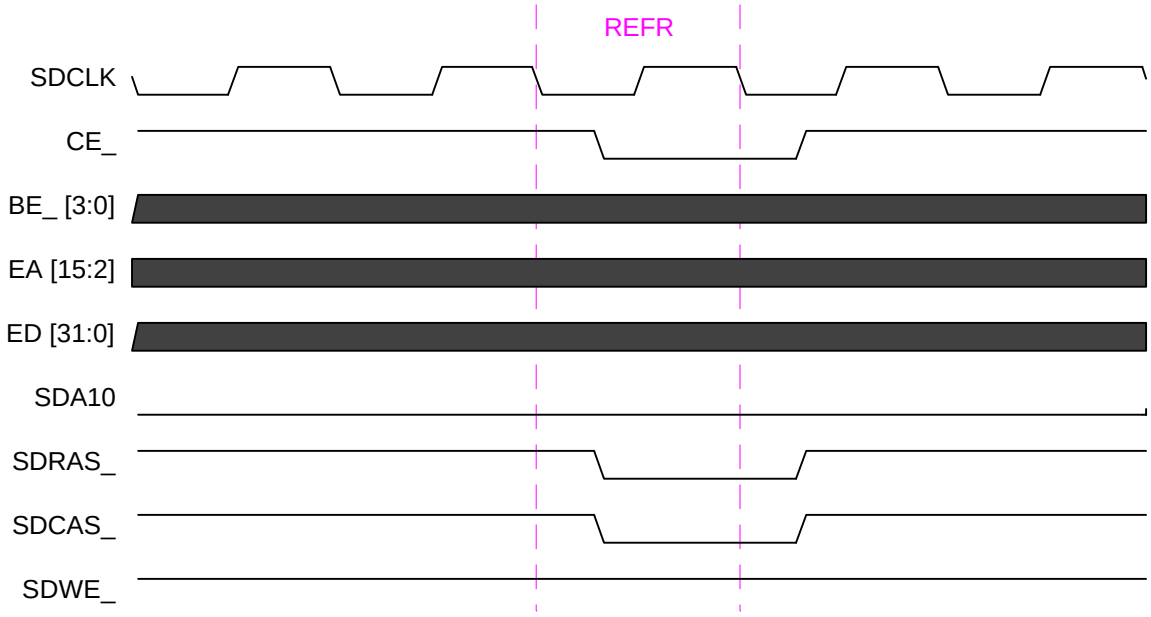
The refresh command (REFR) is sent to all CE spaces configured to use SDRAM by the MTYPE field of the corresponding CE Space Control Register (see Figure 9). REFR is automatically preceded by a DCAB command. This ensures all CE spaces selected with SDRAM are deactivated before refresh occurs. Page information is always invalid before and after a REFR command; thus a refresh cycle always forces a page miss on the next access. Following the DCAB command, the EMIF begins performing “trickle” refreshes at a rate defined by the PERIOD value in the EMIF SDRAM Control register, provided no other SDRAM access is pending.

The SDRAM interface monitors the number of refresh requests posted to it and performs them. Within the EMIF SDRAM control block, a 2 bit counter monitors the backlog of refresh requests. The counter increments once for each refresh request and decrements once for each refresh cycle performed. The counter will saturate at the value of 11 and also at 00. At reset, the counter is automatically set to 11 to ensure that several refreshes occur before accesses begin.

The value of 11 indicates an urgent refresh condition, causing the page information register to be invalidated and forcing the controller to close the current SDRAM page. Thus, the EMIF SDRAM controller performs three REFR commands, decrementing the counter to 00 following the DCAB command before proceeding with the remainder of the current access. If SDRAM is present in multiple CE spaces, the DCAB-refresh sequence occurs in all spaces containing SDRAM.

During idle times on the SDRAM interface(s), if no request is pending from the EMIF, the SDRAM interface performs REFR commands as long as the counter value is nonzero. This feature reduces the likelihood of having to perform urgent refreshes during actual SDRAM accesses later. Note that if SDRAM is present in multiple CE spaces, this refresh occurs only if all interfaces are idle with invalid page information.

Figure 17. SDRAM Refresh



SDRAM REFR COMMAND

SDRAM Initialization

The EMIF performs the necessary functions to initialize SDRAM if any of the CE spaces are configured for SDRAM. An SDRAM initialization is requested by a write of 1 to the INIT in the EMIF SDRAM Control Register (see Figure 10). This should not be done if an SDRAM access is occurring.

The actual sequence of events of an initialization is as follows:

1) DCAB command to all CE spaces configured as SDRAM

2) 3 REFR commands

3) MRS command to all CE spaces configured as SDRAM

Monitoring Page Boundaries

Because SDRAM is a paged memory type, the EMIF SDRAM controller monitors the active row of SDRAM so that row boundaries are not crossed during the course of an access. To accomplish this monitoring, the EMIF stores the address of the open page, and performs compares against that address for subsequent accesses to the SDRAM bank. This storage and comparison is performed independently for each CE space.

The number of address bits compared is a function of the page size programmed in the SDWID field in the EMIF SDRAM Control Register. If SDWID=0 in the SDRAM Control Register, the EMIF expects CE Spaces configured as SDRAM to have four 8 bit wide SDRAMs that have page sizes of 512. Thus, the logical byte address bits compared are 25:11. If SDWID=1, the EMIF expects CE Spaces with SDRAM to have two 16 bit wide SDRAMs that have page sizes of 256. Thus, the logical byte address bits compared are 25:10.[3]

If, during the course of an access, a page boundary is crossed, the EMIF performs a DCAB command and starts a new row access. Note that simply ending the current access is not a condition, which forces the active SDRAM row to be closed. The EMIF speculatively leaves the active row open until it becomes necessary to close it. This feature decreases the deactivate-reactivate overhead and allows the interface to fully capitalize on address locality of memory accesses.

[3] Note that the upper address bit, 25, for both 8 bit and 16 bit wide SDRAM is used to indicate the logical address range accessible for the EMIF, i.e., the top of CE3, which is at address 0x03FFFFFF. Thus, 26 logical address lines (0:25) are needed.

Address Shift

Because the same EMIF pins address the row and column address, the EMIF interface appropriately shifts the address in row and column address selection. Table 16 shows the translation between bits of the byte address and how they appear on the EA pins for row and column addresses. SDRAMs use the address inputs for control as well as address. With this consideration, the following items clarify the figure:

- The address line that corresponds to the SDRAM's Bank Select bit is latched internally by the SDRAM controller. This ensures that the bank select remains correct during READ and WRT commands. Thus EMIF maintains these values as shown in both row and column addresses.
- The EMIF forces the precharge disable (SDA10) to be low unless /RAS is active low, yet high during DCAB commands at the end of a page of accesses. This prevents the auto precharge from occurring following a READ or WRT command.

Table 16. Byte Address to EA Mapping for SDRAM RAS and CAS[4]

	SDRAM width	SDWID	DRAM Command																
SDRAM pins						A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
EMIF pins				EA21-EA17	EA 16	EA 15	EA 14	EA 13	SDA 10	EA 11	EA 10	EA 9	EA 8	EA 7	EA 6	EA 5	EA 4	EA 3	EA 2
Address	x16	1	RAS		24	23	22	21	20	19	18	17	16	15	14	13	12	11	10
Bit			CAS		24	23	22	21	20	19	18	9	8	7	6	5	4	3	2
Address	x8	0	RAS			24	23	22	21	20	19	18	17	16	15	14	13	12	11
Bit			CAS			24	23	22	21	20	10	9	8	7	6	5	4	3	2

Legend:

Bit is internally latched during ACTV command.

Reserved for future use. Undefined.

[4] The RAS and CAS values indicate the bit of the byte address present on the corresponding EA pin during a RAS or CAS cycle.

Timing Constraints

This section will discuss the timing characteristics of SDRAMs necessary to meet the requirements of the C6x.

For the following constraint calculations, a time t_{margin} will be calculated, which represents the margin in the system after taking into account the worst case numbers from the data sheets of the memory and the 'C6x.

After calculating the time t_{margin}, it is a system level issue to determine if the proper amount of margin has been met. The required timing margin is extremely system dependent, depending primarily on trace length and loading, but other factors can come into play. Therefore, this parameter should be determined for the particular system in question.

In general, the timing margin required will not be the same for the different parameters of the read/write cycles. For output signals, the timing margin required will be minimal, since the output clock and the output control/data signals will both be propagating from the C6x to the SDRAM. Therefore, the timing margin will be the skew between the two signals (SSCLK vs. Control and Data) caused by loading effects or differences in route length. For a well designed board, with relatively short board routes, the necessary margin can be estimated as approximately 0.5 ns.

For reads, however, the timing margin required is more complicated. The issue with reads is that the memory is outputting data relative to a clock that has undergone a propagation delay when traveling from the C6x to the SDRAM. The memory outputs the data a time t_{acc} from this delayed clock, and the output data from the memory undergoes a delay itself before arriving at the C6x. Therefore, the timing margin for read setup must account for these two propagation delays. The read hold time is improved because of the same reasons and can be considered negligible. For a well designed board, with relatively short leads, the read setup margin can be estimated as approximately 1.0 ns and the read hold margin can be estimated as 0 ns.

These numbers are guidelines and the actual margin required for any system may be different from these guidelines.

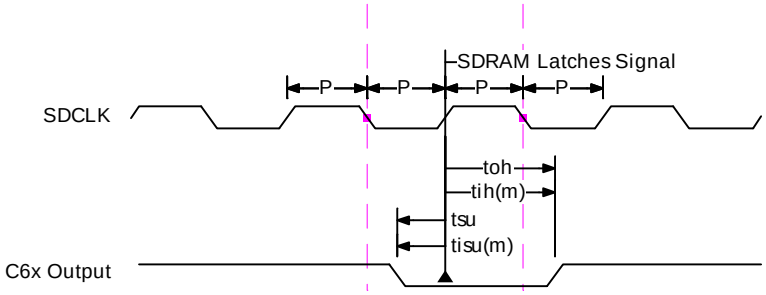
In the discussion below, an 'm' is used to denote the memory specifications and no additional designators will be used to denote the 'C6x timing specifications.

C6x Outputs (ED, EA, CE, BE, SDA10, SDRAS, SDCAS, SDWE)

The C6x begins the output of address, data, and control signals on the falling edge of SDCLK, whereas the SDRAM will latch these signals on the rising edge of SDCLK. For simplicity, the *TMS320C6201 Digital Signal Processor* data sheet specifies the outputs as a setup time to a rising edge and a hold time from a rising edge so that the comparison between C6x specifications and memory specifications is extremely straightforward. The following constraints, which are derived from Figure 18, should be used to verify timing between the C6x and the desired SDRAM.

- Setup Time: Output setup time (t_{su}) from inactive to active must provide an ample setup time ($t_{isu(m)}$) for the input. Therefore, the timing margin available is:
- $t_{margin} = t_{su} - t_{isu(m)}$
- Hold Time: Output hold time (t_{oh}) from active to inactive must be greater than the Hold Time required by the input ($t_{ih(m)}$). As seen in Figure 18, since the transition occurs t_{oh} after the rising edge of SDCLK and the input is read by the SDRAM on the rising edge, this means that the hold time required by the input ($t_{ih(m)}$) must be less than the output hold time. The margin is:
- $t_{margin} = t_{oh} - t_{ih(m)}$

Figure 18. Timing Example for Outputs from the C6x

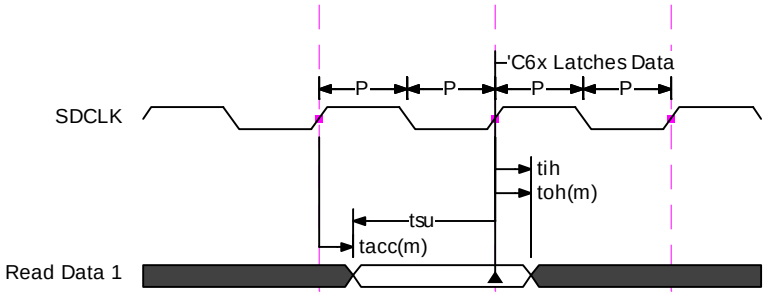


C6x Inputs (Output Data from the SDRAM, Read ED)

A similar situation applies on an SDRAM read. The SDRAM will always output the data on a rising SDCLK edge and the ‘C6x will latch the data on a rising edge of SDCLK. The following constraints, derived from Figure 19, should be used to verify timing between the C6x and the desired SDRAM.

- Setup Times: The access time ($t_{acc(m)}$) of the SDRAM must provide a large enough input setup time (t_{su}) for the input to the C6x. The P used here refers to the period of CLKOUT1, which is one half the period of SDCLK. The timing margin is:
- $t_{margin} = 2P – (t_{acc(m)} + t_{su})$
- Hold Times: The output hold time ($t_{oh(m)}$) for data output from the SDRAM, must provide a hold time greater than the hold time required by the input (t_h) of the C6x. The timing margin is:
- $t_{margin} = t_{oh(m)} – t_h$

Figure 19. Timing Example for Outputs from SDRAM



Timing Comparisons for Three SDRAMs

This section summarizes the comparisons listed above for three different SDRAMs. One of each configuration of SDRAM supported by the C6x is listed. Based on the results shown in the chart below, when compared to the margin guidelines explained earlier, each of these SDRAMs meet the requirements of the C6x and are useable in a design at 100 MHz.

The Texas Instruments and Hitachi parts listed (-10) are 100 MHz devices, and, as seen in the tables, give slightly less margin than the Samsung (-8) 125 MHz device when operating with a 100 MHz SDCLK. Each of the devices listed are available at 125 MHz, but both speed grades are shown here to illustrate that additional timing margin is attainable by using faster SDRAMs.

Several vendors have SDRAM devices available at 100 MHz or faster. Since new data sheets are constantly becoming available, the newest data sheets should be compared to the TMS320C6x data sheet to guarantee operation with the desired margins.

P refers to the period of CLKOUT1 (5 ns for this example), which is equal to one half of the period of SDCLK, or 10 ns for a 100 MHz SDCLK.

- Texas Instruments' TMS626812B-10 is 2 banks x 1M x 8
- Hitachi's HM5216165TT-10 is 2 banks x 512k x 16
- Samsung's KM416S4030BT-8 is 4 banks x 1M x 16

Table 17. Timing Comparisons for SDRAM

Given : P = 5 ns			**Condition**	**Satisfied ?**
C6x Output Setup Time		t_{su} = P – 2.5 ns	$t_{margin} = t_{su} - t_{isu(m)}$	
SDRAM Input Setup Time	TI's TMS626812B-10	$t_{su(m)}$ = 2 ns	t_{margin} = 0.5 ns	✔
	Hitachi's HM5216165TT-10	$t_{su(m)}$ = 2 ns	t_{margin} = 0.5 ns	✔
	Samsung's KM416S4030BT-8	$t_{su(m)}$ = 2 ns	t_{margin} = 0.5 ns	✔
C6x Output Hold Time		t_{oh} = P – 3.5 ns	$t_{margin} = t_{oh} - t_{ih(m)}$	
SDRAM Input Hold Time	TI's TMS626812B-10	$t_{ih(m)}$ = 1 ns	t_{margin} = 0.5 ns	✔
	Hitachi's HM5216165TT-10	$t_{ih(m)}$ = 1 ns	t_{margin} = 0.5 ns	✔
	Samsung's KM416S4030BT-8	$t_{ih(m)}$ = 1 ns	t_{margin} = 0.5 ns	✔
C6x Input Setup Time		t_{su} = 1.5 ns	$t_{margin} = 2P - (t_{acc(m)} + t_{su})$	
SDRAM Output Access Time	TI's TMS626812B-10	$t_{acc(m)}$ = 7.5 ns	t_{margin} = 1 ns	✔
	Hitachi's HM5216165TT-10	$t_{acc(m)}$ = 7.5 ns	t_{margin} = 1 ns	✔
	Samsung's KM416S4030BT-8	$t_{acc(m)}$ = 6 ns	t_{margin} = 2.5 ns	✔
C6x Input Hold Time		t_h = 1.2 ns	$t_{margin} = t_{oh(m)} - t_h$	
SDRAM Output Hold Time	TI's TMS626812B-10	$t_{oh(m)}$ = 3 ns	t_{margin} = 1.8 ns	✔
	Hitachi's HM5216165TT-10	$t_{oh(m)}$ = 3 ns	t_{margin} = 1.8 ns	✔
	Samsung's KM416S4030BT-8	$t_{oh(m)}$ = 3 ns	t_{margin} = 1.8 ns	✔

Complete Example Using Texas Instruments' TMS626812B-10 (2x1Mx8bit)

This section walks through the register configuration for interfacing the C6x with TI's TMS626812B-10, which is 1M x 8 bit x 2 bank SDRAM capable of operating at 100 MHz. If additional timing margin is needed, this device is available at 125 MHz and will provide the same margin as the Samsung SDRAM mentioned previously. Since the memory is 8 bits wide, we use four devices in parallel to complete the 32 bit word, giving a total addressable space of 8 MB. The block diagram for the interface schematic is identical to that shown in Figure 2.

Assumptions:

- CLKOUT1 frequency of 200 MHz
- 100 MHz SDRAM clock frequency.
  (SDCLK = CLKOUT2 = ½ x CLKOUT1 frequency)
- Period = 10 ns
- SDRAM to be located at CE2 (logical address 0x02000000)
- Driven by SDCLK
- SSCLK and CLKOUT1 used by other memory in system
- CLKOUT2 is not in use in the system

Register Configuration

Table 18. SDRAM Registers

Register Name	Fields Required
EMIF Global Control	SDCEN, CLK2EN, SSCEN, CLK1EN
EMIF CE2 Space Control	MTYPE
EMIF SDRAM Control	TRC, TRP, TRCD, INIT, RFEN, SDWID
EMIF SDRAM Timing	PERIOD

EMIF Global Control Registers

Since the TMS626812B -10 SDRAM will be driven by SDCLK, we must then set the following:

Figure 20. EMIF Global Control Register Diagram

31 14	13 12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	rsv	/ARDY	/HOLD	/HOLDA	NOHOLD	SDCEN	SSCEN	CLK1EN	CLK2EN	SSCRT	RBTR8	MAP
0	1 1	0	0	1	1	0	1	1	1	0	0	0	1

SDCEN = 1 indicates that SDCLK is enabled to clock, since we assume it is driving the SDRAM interface

SSCEN = 1 Indicates that SSCLK is enabled, since we assume it is in use by the system

CLK1EN = 1 Indicates that SSCLK is enabled, since we assume it is in use by the system

CLK2EN = 0 indicates that CLKOUT2 is disabled, since we assume it is NOT in use by the system

Thus, a valid setting for the EMIF Global Control Register is 0x00003371.

For additional information on the remainder of the fields, see the *TMS320C6201/6701 Peripherals Reference Guide*.

EMIF CE2 Space Control Register

Figure 21. EMIF CE2 Space Control Register Diagram

31 28	27 22	21 20	19 16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
1111	111111	11	1111

15 14	13 8	7	6 4	3 2	1 0
rsv	READ STROBE	Rsv	MTYPE	Reserved	READ HOLD
11	111111	0	011	00	11

MTYPE = 011 indicates that 32 bit wide SDRAM is located in the CE2 address space. Since SDRAM is configured for this space, the rest of the fields are irrelevant, since they refer to Asynchronous memory.

A valid setting for EMIF CE2 Space Control is 0xFFFFFF33.

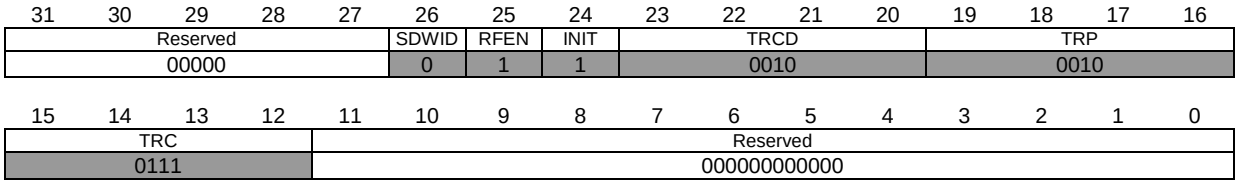
EMIF SDRAM Control Register

For the SDRAM Control Register, values must actually be calculated based on the Clock Frequency used (100 MHz for this example, $t_{CLKOUT2}$ = 10ns) and the parameters of the SDRAM being used. Table 19 summarizes the values.

Table 19. Timing Parameter Calculation for SDRAM Control Register

Field Name	Formula	Value from TMS626812B Data Sheet	Value Calculated for Field	Value Recommended
TRC	TRC = (t_{RC} / $t_{CLKOUT2}$) - 1	t_{RC}=80 ns (min)	TRC = 7	7
TRP	TRP = (t_{RP} / $t_{CLKOUT2}$) - 1	t_{RP} =30 ns (min)	TRP = 2	2
TRCD	TRCD = (t_{RCD} / $t_{CLKOUT2}$) - 1	t_{RCD} = 30 ns (min)	TRCD = 2	2

Figure 22. EMIF SDRAM Control Register



SDWID = 0 Indicates that 8 bit wide SDRAM is used.

RFEN = 1 Indicates that SDRAM refresh is enabled.

INIT = 1 Forces initialization of the SDRAM.

TRCD = 0010b from previous calculation.

TRP = 0010b from previous calculation.

TRC = 0111b from previous calculation.

Based on the above calculations, a value of 0x03227000 should be written to the EMIF SDRAM Control Register.

EMIF SDRAM Refresh Period

Table 20. Period Calculation for SDRAM Refresh Period

Field Name	Formula	Value from TMS626812B Data Sheet	Value Calculated for Field
PERIOD	PERIOD = $t_{Refresh}/t_{CLKOUT2}$	$t_{Refresh}$ = 64 ms / 4096	Period = 0x61A cycles

Figure 23. EMIF SDRAM Refresh Period

31 24	23 12	11 0
Reserved	COUNTER	PERIOD
00000000	000000000000	11000011010 (0x61A)
R, +0	R, +00001000000	RW, +00001000000

Period = 0x61A from previous calculation.

Based on this result, a value of 0x61A should be written to the EMIF SDRAM Refresh Period Register.

Code Segment

The following code segment will set up the EMIF as described above, using The TMS320C6x Peripheral Runtime Support Control Library.

```
#include <emif.h>
.
.   /*OTHER USER CODE*/
.
/* Get default values for all EMIF registers */
unsigned int g_ctrl     = GET_REG(EMIF_GCTRL);
unsigned int ce0_ctrl   = GET_REG(EMIF_CE0_CTRL);
unsigned int ce1_ctrl   = GET_REG(EMIF_CE1_CTRL);
unsigned int ce2_ctrl   = GET_REG(EMIF_CE2_CTRL);
unsigned int ce3_ctrl   = GET_REG(EMIF_CE3_CTRL);
unsigned int sdram_ctrl = GET_REG(EMIF_SDRAM_CTRL);
unsigned int sdram_ref  = GET_REG(EMIF_SDRAM_REF);

/* Set Global Control - Disable CLKOUT2 */
/*                    - Enable SDCLK, CLKOUT1, and SSCLK */
RESET_BIT(&g_ctrl, CLK2EN);
SET_BIT(&g_ctrl, CLK1EN);
SET_BIT(&g_ctrl, SSCEN);
SET_BIT(&g_ctrl, SDCEN);

/* Configure CE2 as SDRAM  */
LOAD_FIELD(&ce2_ctrl  , MTYPE_32SDRAM, MTYPE , MTYPE_SZ       );

/* Configure SDRAM Control Register */
LOAD_FIELD(&sdram_ctrl, 7            , TRC   , TRC_SZ         );
LOAD_FIELD(&sdram_ctrl, 2            , TRP   , TRP_SZ         );
LOAD_FIELD(&sdram_ctrl, 2            , TRCD  , TRCD_SZ        );
RESET_BIT(&sdram_ctrl, SDWID);
SET_BIT(&sdram_ctrl, INIT);
SET_BIT(&sdram_ctrl, RFEN);

/* Set Refresh Period */
LOAD_FIELD(&sdram_ref, 0x61A         , PERIOD, PERIOD_SZ      );

/* Store EMIF Control Registers */
emif_init(g_ctrl, ce0_ctrl, ce1_ctrl, ce2_ctrl, ce3_ctrl,
                sdram_ctrl, sdram_ref);
.
.   /*OTHER USER CODE*/
.
```

Complete Example Using Hitachi's HM5216165TT-10 (2x512kx16bit)

This section walks through the register configuration for interfacing the C6x with Hitachi's HM5216165TT-10. The HM5216165TT-10 is 512k x 16 bit x 2 bank SDRAM capable of operating at 100 MHz. Since the memory is 16 bits wide, we use two devices in parallel to complete the 32 bit word, giving a total addressable space of 4 MB. The block diagram for the interface schematic is identical to that shown in Figure 1.

Assumptions:

- CLKOUT1 frequency of 200 MHz
- 100 MHz SDRAM clock frequency.
  (SDCLK = CLKOUT2 = ½ x CLKOUT1 frequency)
- Period = 10 ns
- SDRAM to be located at CE2 (logical address 0x02000000)
- Driven by SDCLK
- SSCLK, CLKOUT1 not in use in the system
- CLKOUT2 is being used in the system

Register Configuration

Table 21. SDRAM Registers

Register Name	Fields Required
EMIF Global Control	SDCEN, and CLK2EN
EMIF CE2 Space Control	MTYPE
EMIF SDRAM Control	TRC, TRP, TRCD, INIT, RFEN, SDWID
EMIF SDRAM Timing	PERIOD

EMIF Global Control Registers

Since the HM5216165TT-10 SDRAM will be driven by SDCLK, we must then set the following:

Figure 24. EMIF Global Control Register Diagram

31 14	13 12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Rsv	/ARDY	/HOLD	/HOLDA	NOHOLD	SDCEN	SSCEN	CLK1EN	CLK2EN	SSCRT	RBTR8	MAP
0	1 1	0	0	1	1	0	1	0	0	1	0	0	1

SDCEN = 1 indicates that SDCLK is enabled to clock.

SSCEN = 0 Indicates that SSCLK is disabled, since we assume it is NOT in use by the system

CLK1EN = 0 Indicates that SSCLK is disabled, since we assume it is NOT in use by the system

CLK2EN = 1 Indicates that CLKOUT2 is enabled, assuming that some other peripheral makes use of this signal.

Thus, a valid setting for the EMIF Global Control Register is 0x00003349.

For additional information on the remainder of the fields, see the *TMS320C6201/6701 Peripherals Reference Guide*.

EMIF CE2 Space Control Register

Figure 25. EMIF CE2 Space Control Register Diagram

31 28	27 22	21 20	19 16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
1111	111111	11	1111

15 14	13 8	7	6 4	3 2	1 0
Rsv	READ STROBE	Rsv	MTYPE	Reserved	READ HOLD
11	111111	0	011	00	11

MTYPE = 011 indicates that 32 bit wide SDRAM is located in the CE2 address space. Since SDRAM is configured for this space, the rest of the fields are irrelevant, since they refer to Asynchronous memory.

A valid setting for EMIF CE2 Space Control is 0xFFFFFF33.

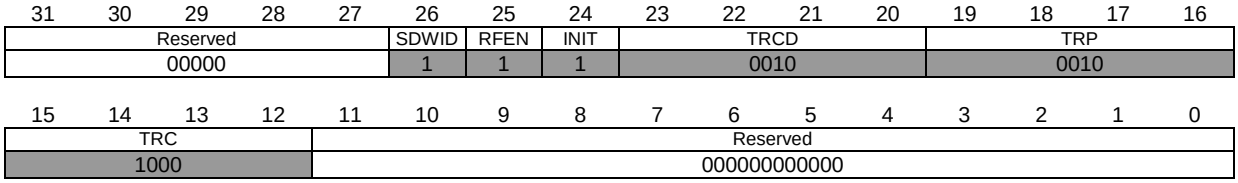
EMIF SDRAM Control Register

For the SDRAM Control Register, values must actually be calculated based on the Clock Frequency used (100 MHz for this example, $t_{CLKOUT2}$ = 10ns) and the parameters of the SDRAM being used. Table 22 summarizes the values.

Table 22. Timing Parameter Calculation for SDRAM Control Register

Field Name	Formula	Value from HM5216165 Data Sheet	Value Calculated for Field	Value Recommended
TRC	TRC = (t_{RC} / $t_{CLKOUT2}$) - 1	t_{RC}=90 ns (min)	TRC = 8	8
TRP	TRP = (t_{RP} / $t_{CLKOUT2}$) - 1	t_{RP} =30 ns (min)	TRP = 2	2
TRCD	TRCD = (t_{RCD} / $t_{CLKOUT2}$) - 1	t_{RCD} = 30 ns (min)	TRCD = 2	2

Figure 26. EMIF SDRAM Control Register



SDWID = 1 indicates that 16 bit wide SDRAM is used.

RFEN = 1 indicates that SDRAM refresh is enabled.

INIT = 1 forces initialization of the SDRAM.

TRCD = 0010b from previous calculation.

TRP = 0010b from previous calculation.

TRC = 1000b from previous calculation.

Based on the above calculations, a value of 0x07228000 should be written to the EMIF SDRAM Control Register.

EMIF SDRAM Refresh Period

Table 23. Period Calculation for SDRAM Refresh Period

Field Name	Formula	Value from HM5216165 Data Sheet	Value Calculated for Field
PERIOD	PERIOD = $t_{Refresh}/t_{CLKOUT2}$	$t_{Refresh}$ = 64 ms / 4096	Period = 0x61A cycles

Figure 27. EMIF SDRAM Refresh Period

31 24	23 12	11 0
Reserved	COUNTER	PERIOD
00000000	000000000000	11000011010 (0x61A)

Period = 0x61A from previous calculation.

Based on this result, a value of 0x61A should be written to the EMIF SDRAM Refresh Period Register.

Code Segment

The following code segment will set up the EMIF as described above, using The TMS320C6x Peripheral Runtime Support Control Library.

```
#include <emif.h>
.
.   /*OTHER USER CODE*/
.
/* Get default values for all EMIF registers */
unsigned int g_ctrl     = GET_REG(EMIF_GCTRL);
unsigned int ce0_ctrl   = GET_REG(EMIF_CE0_CTRL);
unsigned int ce1_ctrl   = GET_REG(EMIF_CE1_CTRL);
unsigned int ce2_ctrl   = GET_REG(EMIF_CE2_CTRL);
unsigned int ce3_ctrl   = GET_REG(EMIF_CE3_CTRL);
unsigned int sdram_ctrl = GET_REG(EMIF_SDRAM_CTRL);
unsigned int sdram_ref  = GET_REG(EMIF_SDRAM_REF);

/* Set Global Control - Enable CLKOUT2 and SDCLK*/
/*                    - Disable CLKOUT1 and SSCLK */
SET_BIT(&g_ctrl, CLK2EN);
RESET_BIT(&g_ctrl, CLK1EN);
RESET_BIT(&g_ctrl, SSCEN);
SET_BIT(&g_ctrl, SDCEN);

/* Configure CE2 as SDRAM  */
LOAD_FIELD(&ce2_ctrl  , MTYPE_32SDRAM, MTYPE , MTYPE_SZ       );

/* Configure SDRAM Control Register */
LOAD_FIELD(&sdram_ctrl, 8            , TRC   , TRC_SZ         );
LOAD_FIELD(&sdram_ctrl, 2            , TRP   , TRP_SZ         );
LOAD_FIELD(&sdram_ctrl, 2            , TRCD  , TRCD_SZ        );
SET_BIT(&sdram_ctrl, SDWID);
SET_BIT(&sdram_ctrl, INIT);
SET_BIT(&sdram_ctrl, RFEN);

/* Set Refresh Period */
LOAD_FIELD(&sdram_ref, 0x61A         , PERIOD, PERIOD_SZ      );

/* Store EMIF Control Registers */
emif_init(g_ctrl, ce0_ctrl, ce1_ctrl, ce2_ctrl, ce3_ctrl,
                sdram_ctrl, sdram_ref);
.
.   /*OTHER USER CODE*/
.
```

Complete Example Using Samsung's KM416S4030BT-8 (2x512kx16bit)

This section will walk through the register configuration for interfacing the C6x with Samsung's KM416S4030BT-8, which is 1M x 16 bit x 4 bank SDRAM capable of operating at 125 MH. Since the memory is 16 bits wide, we use two devices in parallel to complete the 32 bit word, giving a total addressable space of 16 MB. The block diagram for the interface schematic is identical to that shown in Figure 3.

This 125 MHz SDRAM is featured, since it offers additional timing margin compared to typical 100 MHz SDRAMs and may be used in a system that requires extra margin.

Assumptions:

- CLKOUT1 frequency of 200 MHz
- 100 MHz SDRAM clock frequency.
  (SDCLK = CLKOUT2 = ½ x CLKOUT1 frequency).
- Period = 10 ns
- SDRAM to be located at CE3 (logical address 0x03000000)
- Driven by SDCLK
- CLKOUT1, CLKOUT2, and SSCLK not in use by the system

Register Configuration

Table 24. SDRAM Registers

Register Name	Fields Required
EMIF Global Control	SDCEN, SSCEN, CLK1EN, CLK2EN
EMIF CE2 Space Control	MTYPE
EMIF SDRAM Control	TRC, TRP, TRCD, INIT, RFEN, SDWID
EMIF SDRAM Timing	PERIOD

EMIF Global Control Registers

Since the KM416S4030BT-8 SDRAM will be driven by SDCLK, we must then set the following:

Figure 28. EMIF Global Control Register Diagram

31 14	13 12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	rsv	/ARDY	/HOLD	/HOLDA	NOHOLD	SDCEN	SSCEN	CLK1EN	CLK2EN	SSCRT	RBTR8	MAP
0	1 1	0	0	1	1	0	1	0	0	0	0	0	1

SDCEN = 1 indicates that SDCLK is enabled to clock, since we assume it is driving the SDRAM interface

SSCEN = 1 Indicates that SSCLK is enabled, since we assume it is in use by the system

CLK1EN = 1 Indicates that SSCLK is enabled, since we assume it is in use by the system

CLK2EN = 0 indicates that CLKOUT2 is disabled, since we assume it is NOT in use by the system

Thus, a valid setting for the EMIF Global Control Register is 0x00003341.

For additional information on the remainder of the fields, see the *TMS320C6201/6701 Peripherals Reference Guide*.

EMIF CE3 Space Control Register

Figure 29. EMIF CE3 Space Control Register Diagram

31 28	27 22	21 20	19 16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
1111	111111	11	1111

15 14	13 8	7	6 4	3 2	1 0
rsv	READ STROBE	rsv	MTYPE	Reserved	READ HOLD
11	111111	0	011	00	11

MTYPE = 011 indicates that 32 bit wide SDRAM is located in the CE3 address space. Since SDRAM is configured for this space, the rest of the fields are irrelevant, since they refer to Asynchronous memory.

A valid setting for EMIF CE3 Space Control is 0xFFFFFF33.

EMIF SDRAM Control Register

For the SDRAM Control Register, values must actually be calculated, based on the Clock Frequency used (100 MHz for this example, $t_{CLKOUT2}$ = 10ns) and the parameters of the SDRAM being used. Table 25 summarizes the values.

Table 25. Timing Parameter Calculation for SDRAM Control Register

Field Name	Formula	Value from KM416S4030 Data Sheet	Value Calculated for Field	Value Recommended
TRC	TRC = (t_{RC} / $t_{CLKOUT2}$) – 1	t_{RC}=68 ns (min)	TRC = 5.8	6
TRP	TRP = (t_{RP} / $t_{CLKOUT2}$) – 1	t_{RP} =20 ns (min)	TRP = 1	1
TRCD	TRCD = (t_{RCD} / $t_{CLKOUT2}$) - 1	t_{RCD} = 20 ns (min)	TRCD = 1	1

Figure 30. EMIF SDRAM Control Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					SDWID	RFEN	INIT	TRCD				TRP			
00000					1	1	1	0001				0001			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRC				Reserved											
0110				000000000000											

SDWID = 1 indicates that 16 bit wide SDRAM is used.

RFEN = 1 indicates that SDRAM refresh is enabled.

INIT = 1 forces initialization of the SDRAM.

TRCD = 0001b from previous calculation.

TRP = 0001b from previous calculation.

TRC = 0110b from previous calculation.

Based on the above calculations, a value of 0x07116000 should be written to the EMIF SDRAM Control Register.

EMIF SDRAM Refresh Period

Table 26. Period Calculation for SDRAM Refresh Period

Field Name	Formula	Value from KM416S4030 Data Sheet	Value Calculated for Field
PERIOD	PERIOD = $t_{Refresh}/t_{CLKOUT2}$	$t_{Refresh}$ = 64 ms / 4096	Period = 0x61A cycles

Figure 31. EMIF SDRAM Refresh Period

31	24	23	12	11	0
Reserved		COUNTER		PERIOD	
00000000		000000000000		11000011010 (0x61A)	
R, +0		R, +00001000000		RW, +00001000000	

Period = 0x61A from previous calculation.

Based on this result, a value of 0x61A should be written to the EMIF SDRAM Refresh Period Register.

Code Segment

The following code segment will set up the EMIF as described above, using The TMS320C6x Peripheral Runtime Support Control Library.

```
#include <emif.h>
.
.   /*OTHER USER CODE*/
.
/* Get default values for all EMIF registers */
unsigned int g_ctrl     = GET_REG(EMIF_GCTRL);
unsigned int ce0_ctrl   = GET_REG(EMIF_CE0_CTRL);
unsigned int ce1_ctrl   = GET_REG(EMIF_CE1_CTRL);
unsigned int ce2_ctrl   = GET_REG(EMIF_CE2_CTRL);
unsigned int ce3_ctrl   = GET_REG(EMIF_CE3_CTRL);
unsigned int sdram_ctrl = GET_REG(EMIF_SDRAM_CTRL);
unsigned int sdram_ref  = GET_REG(EMIF_SDRAM_REF);

/* Set Global Control - Enable SDCLK*/
/*                    - Disable CLKOUT2, CLKOUT1, SSCLK */
RESET_BIT(&g_ctrl, CLK2EN);
RESET_BIT(&g_ctrl, CLK1EN);
RESET_BIT(&g_ctrl, SSCEN);
SET_BIT(&g_ctrl, SDCEN);

/* Configure CE2 as SDRAM  */
LOAD_FIELD(&ce2_ctrl  , MTYPE_32SDRAM, MTYPE , MTYPE_SZ       );

/* Configure SDRAM Control Register */
LOAD_FIELD(&sdram_ctrl, 6            , TRC   , TRC_SZ         );
LOAD_FIELD(&sdram_ctrl, 1            , TRP   , TRP_SZ         );
LOAD_FIELD(&sdram_ctrl, 1            , TRCD  , TRCD_SZ        );
SET_BIT(&sdram_ctrl, SDWID);
SET_BIT(&sdram_ctrl, INIT);
SET_BIT(&sdram_ctrl, RFEN);

/* Set Refresh Period */
LOAD_FIELD(&sdram_ref, 0x61A         , PERIOD, PERIOD_SZ      );

/* Store EMIF Control Registers */
emif_init(g_ctrl, ce0_ctrl, ce1_ctrl, ce2_ctrl, ce3_ctrl,
                sdram_ctrl, sdram_ref);
.
.   /*OTHER USER CODE*/
.
```

References

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