

TMS320C6x Reset Circuit

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TMS320C6x Reset Circuit

Abstract

This document describes how to provide a reset circuit to the Texas Instruments (TI™) TMS320C6x digital signal processor (DSP).

To ensure that the TMS320C6x will not generate signals unless the supply voltages are at their appropriate levels, it is necessary to place a supervisor on the power supplies. Anytime the device is powered up, it should be held in reset until both the 3.3V I/O supply (DVdd) and the 2.5V core supply (CVdd) reach their nominal values. Likewise, the device should be held in reset anytime either supply falls below a certain threshold value (88%).

Product Support

Related Documentation

The following list specifies product names, part numbers, and literature numbers of corresponding TI documentation.

- ❑ *TLC77xx Series of BiCMOS Supply Voltage Supervisors*, April 1995, Literature number SLVAE03
- ❑ *Supply Voltage Supervisor TLC77xx Series*, Eilhard Haseloff, March 1997, Literature number SLVAE04
- ❑ *TLC7701, TLC7725, TLC7703, TLC7733, TLC7705 Micropower Supply Voltage Supervisors* data sheet, August 1997, Literature number SLVS087I

World Wide Web

Our World Wide Web site at **www.ti.com** contains the most up to date product information, revisions, and additions. Users registering with TI&ME can build custom information pages and receive new product updates automatically via email.

Email

For technical issues or clarification on switching products, please send a detailed email to **dsph@ti.com**. Questions receive prompt attention and are usually answered within one business day.



Design Problem

How do I provide a reset circuit to the TMS320C6x?

Solution

To ensure that the TMS320C6x will not begin to generate signals unless the supply voltages are at their appropriate levels, it is necessary to place a supervisor on the power supplies. Anytime the device is powered up, it should be held in reset until both the 3.3V I/O supply (DVdd) and the 2.5V core supply (CVdd) reach their nominal values. Likewise, the device should be held in reset anytime either supply falls below a certain threshold value (88%).

One simple way to accomplish both of these tasks is to set a supervisor on each of the supply voltages, DVdd and CVdd. The TLC7733 and TLC7725 voltage supervisors from Texas Instruments, for example, each assert a /RESET signal (active LOW) during power-up when their supply voltage reaches 1V. This signal continues to be asserted until DVdd reaches its threshold voltage (plus an additional delay period¹), at which time the device is released from reset. The /RESET signal is reasserted anytime the voltage level falls below 90% (2.93V for the TLC7733 and 2.25V for the '7725).

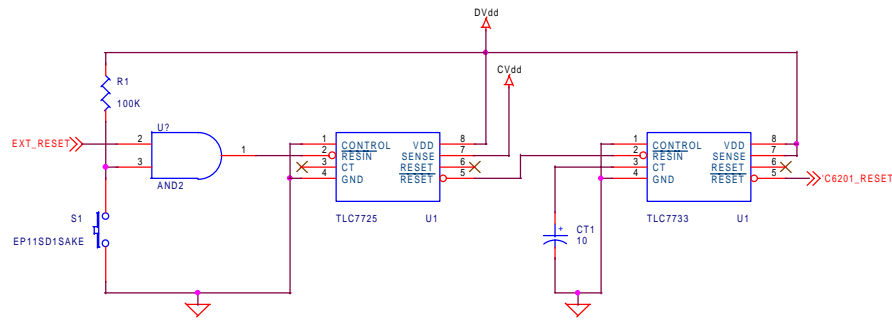
In addition to holding the DSP in reset while not fully powered up, the TLC77xx also allows for an externally generated signal to generate the /RESET assertion. This signal could result from another device driving a reset signal or a manual pushbutton switch being depressed. If both a digital signal and a manual reset are used in the design, the two signals should be combined logically (AND gate), then connected to /RESIN of the first supervisor. All external reset signals should go through the supervisor circuit². If an external reset is introduced after the supervisor circuit, the timing delay requirements may not be met.

Figure 1 shows a sample circuit for the 'C6x using the supervisor chip, which monitors both supply voltages and allows for both a manual (pushbutton) and externally generated reset. The second-stage supervisor should set the delay time to ensure that it is constant regardless of the cause of the reset.

¹ The delay period is determined by the capacitor CT of the reset circuit. In the design example provided, the delay times are <40ns (see data sheet for propagation times with CT = NC) for the first stage and 210ms for the second stage.

² All inputs to /RESIN must meet the minimum pulse requirement of 1μs, with rise and fall times of less than 10ns.

Figure 1. Reset Circuit Using TLC77xx³



The delay time set by the reset circuit should be determined by considering the switch-on time of several components. These are summarized in Table 1.

Table 1. Setting of the Delay Timing t_d

	Switch-On Time
Line operated power supply	10ms - 100ms
Battery power supply	0.03ms - 30ms
Oscillator (Start-up Time)	10ms – 100ms
Reset program	Several microseconds
Range of delay times t_d to be set	20ms – 500ms

For additional information about designing with the TLC77xx supervisors, see the application note, *TLC77xx Series of BiCMOS Supply Voltage Supervisors*.

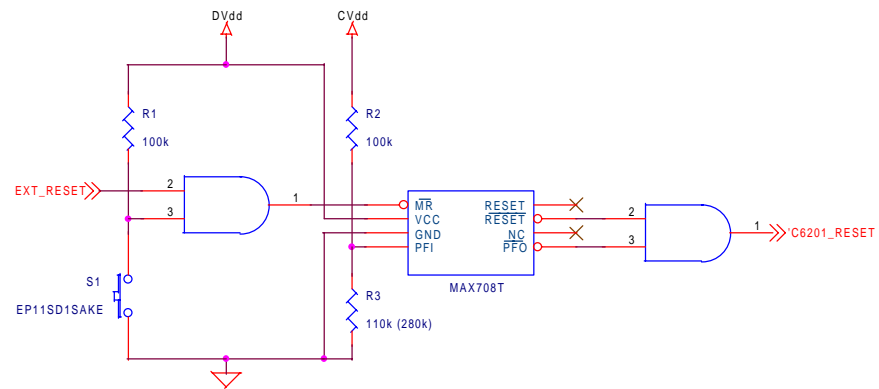
Another solution is to monitor both the 2.5/1.8V and 3.3V power supplies. This allows the DSP to be released from reset only if both its power supplies are at the proper levels. This can be easily done with a device that is also available in an 8-pin package and does not require an external capacitor to set its reset pulse width. It requires two resistors to set the 1.8/2.5 voltage selection and is available from at least two sources:

- ❑ Analog Devices (ADM708)
- ❑ Maxim (MAX708)

A reference diagram showing the reset circuit using the Maxim Part is shown in Figure 2.

³ To provide a reset circuit which could be used for Rev 3 and later, it would be necessary to use the TLC7701 (threshold voltage = 1.1V) in place of the TLC7725 with a voltage divider to the SENSE input. Please see the TLC77xx data sheet for selecting voltage divider resistors.

Figure 2. Reset Circuit Using MAX708T⁴



⁴ Circuit shown is for CVdd=2.5V. For CVdd=1.8V, use the resistor value in parentheses for R3.