TMS320C24x PWM Full Compare in Symmetric Mode

Application Report
SPRA369

TEXAS INSTRUMENTS

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Overview

There are three Full Compare Units in the Event Manager Module. Each Full Compare Unit has two associated PWM outputs. The time base for Full Compare Units is provided by GP Timer One.
This application report presents applications of the Full Compare: up to six PWM, three PWM plus three complemented PWM generation in symmetric mode.

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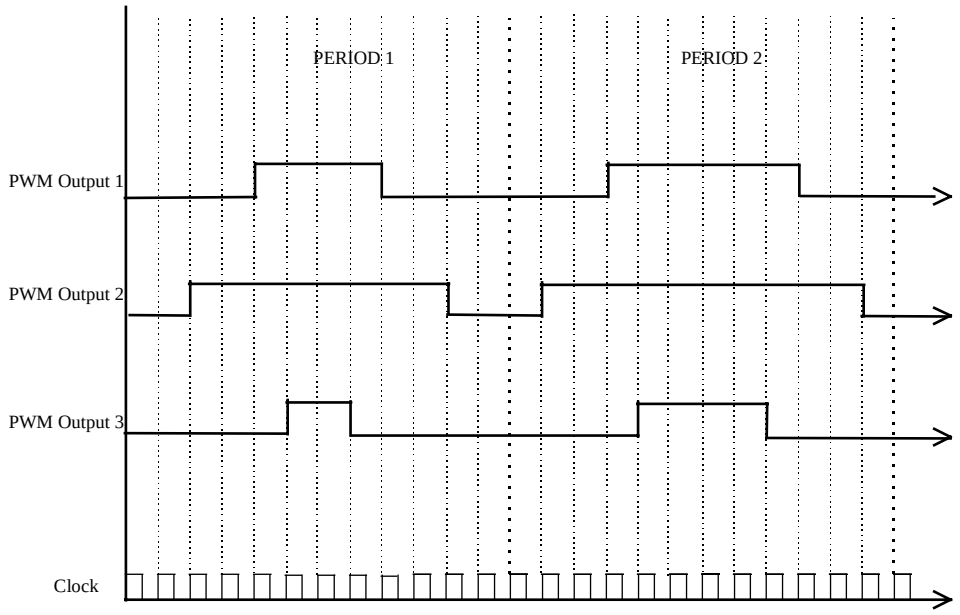
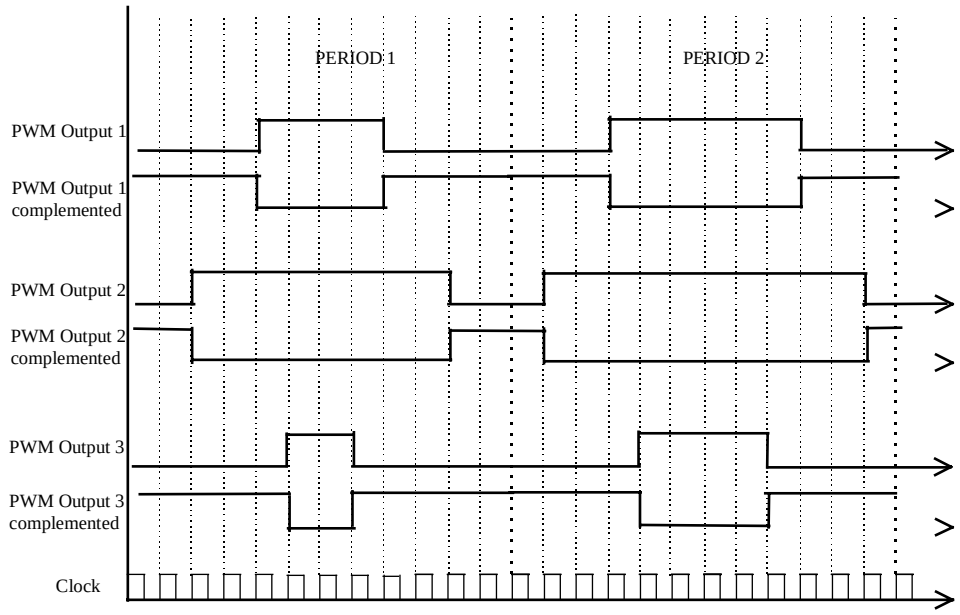
1. Possibilities of PWM Full Compare in Symmetric Mode

Full Compare in symmetric mode can be used:

- To generate **three symmetrical PWM** on the Full Compare outputs

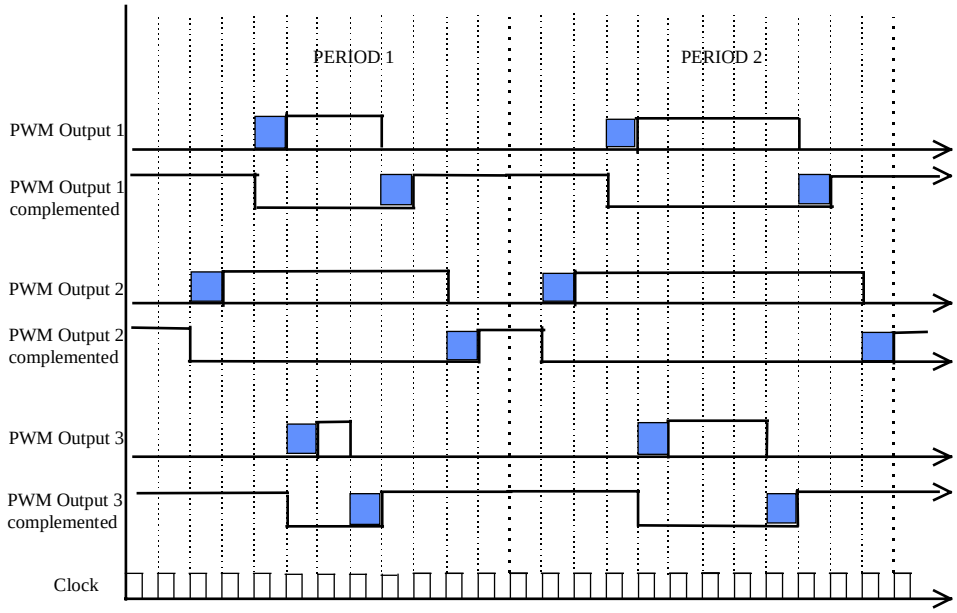


- To generate **three symmetrical PWM** plus **three complemented PWM** on the Full Compare outputs



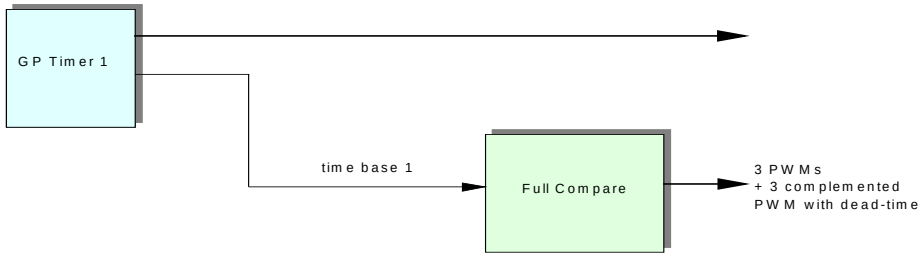
- To generate **three symmetrical PWM** plus **three complemented PWM with Dead-Time** on the Full Compare outputs.
  In this case, Dead Band values are the same for three pairs PWM.

For Dead-Band cf. application note "Dead-Band generation on the TMS320C24x"



2. Description : Event Manager Programming

2.1 Connection of Full Compare Units in the Events Manager



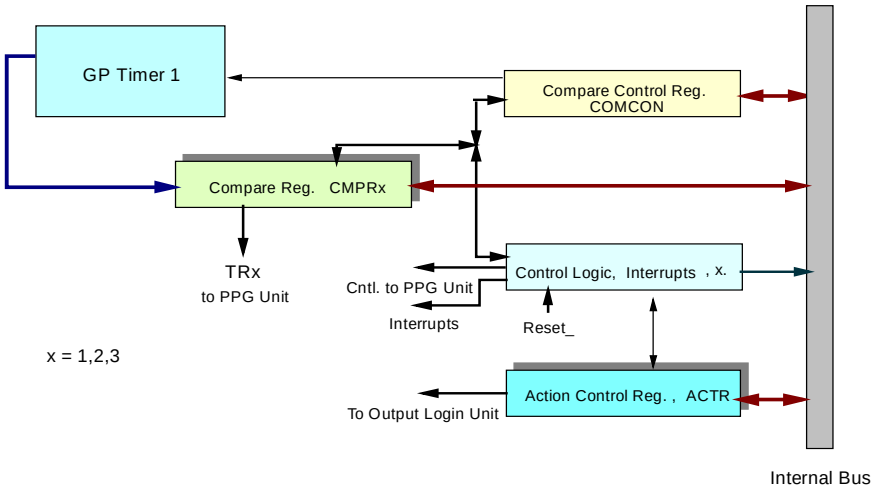
Three pairs PWM (Full Compare) are exclusively based on the Time Base One, but these PWM can be totally independent with the three PWM (Simple Compare) if these last PWM are based on Time Base Two.

The PWM connected to the Time Base One is dependent with the three pairs PWM.

Each pair PWM connected to Time Base One support:

- **Complemented PWM**, signals will be exactly opposite of each other.
- **Complemented PWM with Dead-Band**, signals will be opposite of each other with a time interval which separate transition edges.
- All PWM combinations, each output pin of pairs PWM can be programmed by user software to have the same transitions, to be complemented, to have one PWM set or reset and the other toggles.

Full Compare Unit composition



2.2 Preparation Phase to Configure the Three Full Compare Units

Two main modules have to be programmed to generate three pairs PWM:

- Full Compare Units programming:
  - to write ACTR : Action Control Register which controls the action on each of 6 compare output pins.
  - to write CMPR1 : Compare register 1
  - to write CMPR2 : Compare register 2
  - to write CMPR3 : Compare register 3
  - to write DBTCON : Dead-Band Timer Control Register
  - to write COMCON : Compare Control Register.
- Timer Base generation with General Purpose Timer 1:
  CF Application note "TMS320C24x General Purpose Timer 1 symmetric mode"
  - to write TPR1 : Timer Period register.
  - to write TCNT1 : Counter register initialization.
  - to write TCON1 with bit 6=0b (timer disable)

– : Control register to program Count Mode Selection, Clock Pre-scaler, Clock Source, compare reload condition, enable compare operation .

– to write TCON1 with bit 6=1b to start the timer.
: Control register to enable the Timer 1

2.3 Example

Generation of three pairs PWM, each pair has an output and a complemented output. PWM are symmetrical.

- free run, no emulation mode.
- Timer count mode in continuous Up/Down-Count Mode: symmetrical PWM.
- No timer input pre-scaler and internal clock.
- Reload the Full Compare shadow compare register when counter equal 0.
- PWM output Active High for uneven output and Active Low for even output.
- No dead-band
- Period 5 * 2 * 50ns.

Register programming:

```
ACTR          =  0666h
                 Bit 1&0      :10b  ,Active High for output 1
                 Bit 3&2      :10b  ,Active Low for output 2
                                    (output 1 complemented)
                 Bit 5&4      :10b  ,Active High for output 3
                 Bit 7&6      :10b  ,Active Low for output 4
                                    (output 3 complemented)
                 Bit 9&8      :10b  ,Active High for output 5
                 Bit 11&10    :10b  ,Active Low for output 6
                                    (output 5 complemented)
DBTCON        =  0000h              ,No deadband
CMPR1         =  3h
CMPR2         =  2h
CMPR3         =  4h

COMCON(1)     =  0307h
                 Bit 0        :1b   ,PWM mode for PWM2 and PWM1
                 Bit 1        :1b   ,PWM mode for PWM4 and PWM3
                 Bit 2        :1b   ,PWM mode for PWM6 and PWM5
                 Bit 9        :1b   ,Full Compare output are
                                    enabled.
                 Bit 11&10    :00b  ,Reload Compare register at
                                    TCNT1=0.
COMCON(2)     =  8307h
                 Bit 15       :1b   ,Enable Compare operations
```

CF Application note "TMS320C24x General Purpose Timer 1 in symmetric mode" for Time Base Generation

```
TPR1          =  5h
TCMPR1        =  3h
TCNT1         =  0h
TCON1 (first) =  a802h
                 Bit 1        : 1b   , Enable timer compare
                                       operation.
                 Bit 3&2      : 00b  , Compare Register reload
                                       when counter is zero.
                 Bit 5&4      : 00b  , Internal Clock source
                                       select.
                 Bit 6        : 0b   , Timer 1 Disabled and pre-
                                       scaler reset.
                 Bit 13,12&11 : 101b , Continuous-Up/Down Count
                                       Mode.
                 Bit 15&14    : 10b  , GP timer not affected by
                                       emulation suspend.
TCON1 (second) = a842h
                 Bit 6        : 1b   , Timer 1 is enabled.
```

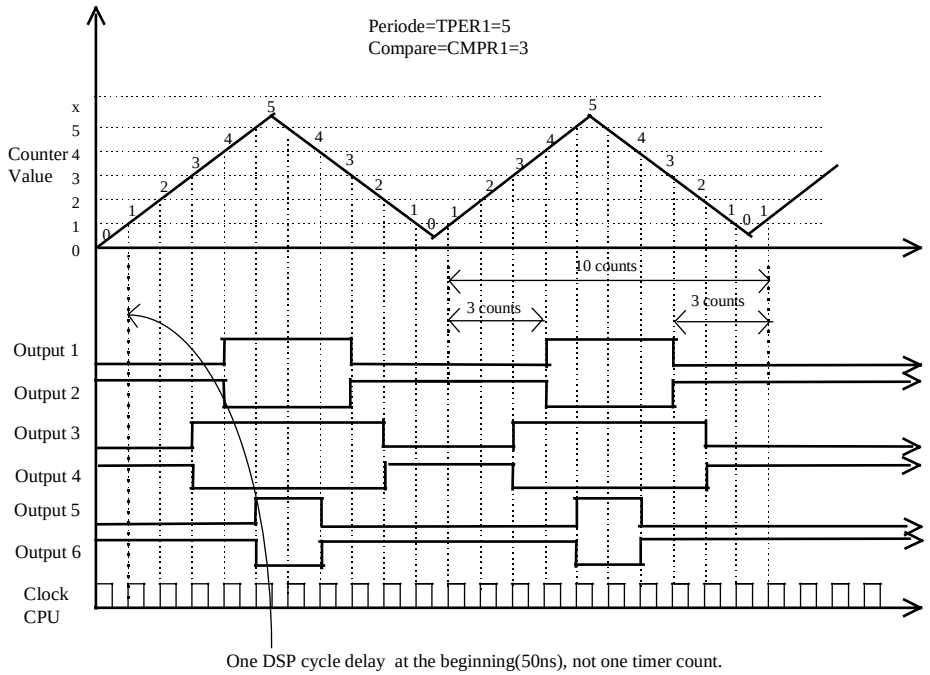
Initialization Assembly code:

```
        ;Note : registers are memory mapped.

GPTCON .set   7400h     ;General Timer Controls
TCNT1  .set   7401h     ;T1 Counter Register
TPR1   .set   7403h     ;T1 Period Register
TCON1  .set   7404h     ;T1 Control Register
COMCON .set   740dh     ;Compare Control Register
ACTR   .set   740eh     ;Full Compare Action Register
DBTCON .set   7410h     ;Dead-Band Timer control register
CMPR1  .set   7411h     ;Full Compare unit Compare register 1
CMPR2  .set   7412h     ;Full Compare unit Compare register 1
CMPR3  .set   7413h     ;Full Compare unit Compare register 1

        LDP    #232
        SPLK   #666h,ACTR
        SPLK   #0h,DBTCON
        SPLK   #3h,CMPR1
        SPLK   #2h,CMPR2
        SPLK   #4h,CMPR3
        SPLK   #307h,COMCON
        SPLK   #8307h,COMCON
        SPLK   #5h,TPR1
        SPLK   #0h,TCNT1
        SPLK   #0a802h,TCON1
```

Result of this Example



Note:
The first period of a continuous up/down count is 1 DSP cycle longer and is not totally symmetrical (see diagram above).

2.4 Modification of the Active Width during Running

When new compare values in the Full Compare registers are written, new values are loaded in a shadow register and are active at the end of the period, when TCNT1=0 (for this configuration).

Example:
CMPR1 switch from 3 to 4 during the second period
CMPR2 switch from 2 to 3 during the second period
CMPR3 stays at the same value

Results will be