TMS320C24x
General Purpose Timer 1
Asymmetric Mode

Application Report
SPRA367

Texas Instruments

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Overview

There are three General Purpose (GP) timers in the Event Manager of the ‘C240. These timers can be used as independant time base in applications such as:

- generation of sampling period in a control system,
- providing time base for quadrature encoder sensor signal processing in a motor control system,
- providing time base for the operation of Full and Simple Compare Units and associated PWM circuits to generate PWM outputs in a motor control system.

This application report present one application of the GP timer: Time base and PWM generation using GP Timer One in asymmetric mode.

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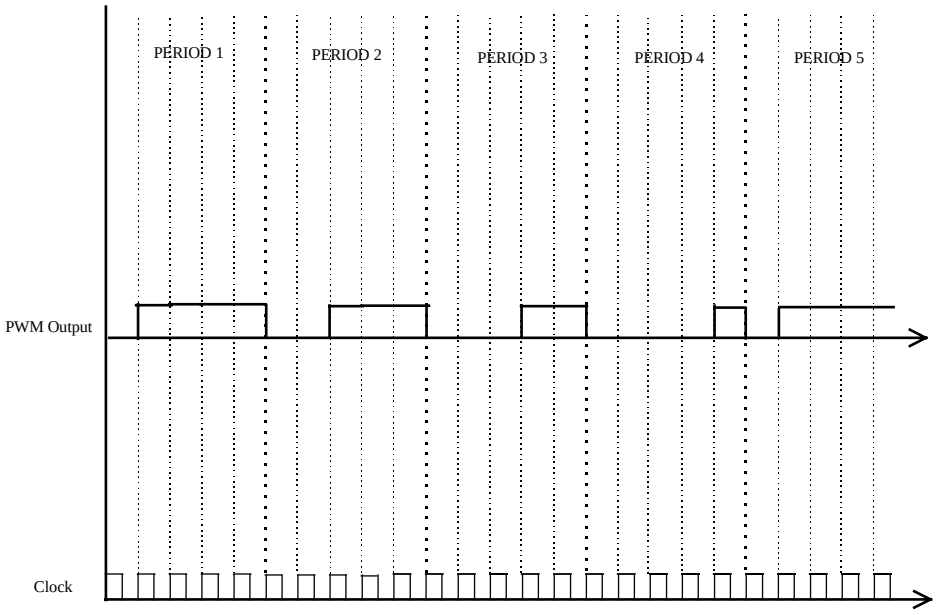
Note:
General Purpose Timer 2 and General Purpose Timer 3 have same functionalities than Timer 1 except for Time Base generation for Full or Simple Compare.

1. Possibilities of GP Timer 1 in Asymmetric Mode

General Purpose Timer 1 in asymmetric mode can be used:

- To generate one **non symmetrical PWM** on the GP Timer 1 output with the following features :
  - this PWM connected to Time Base One is Time Base dependent (Counter and Period) on the three pairs PWM (Full Compare) connected exclusively to Time Base One.
  - this PWM could be totally independent of the three PWM (Simple Compare) if these three PWM are based on Time Base Two.

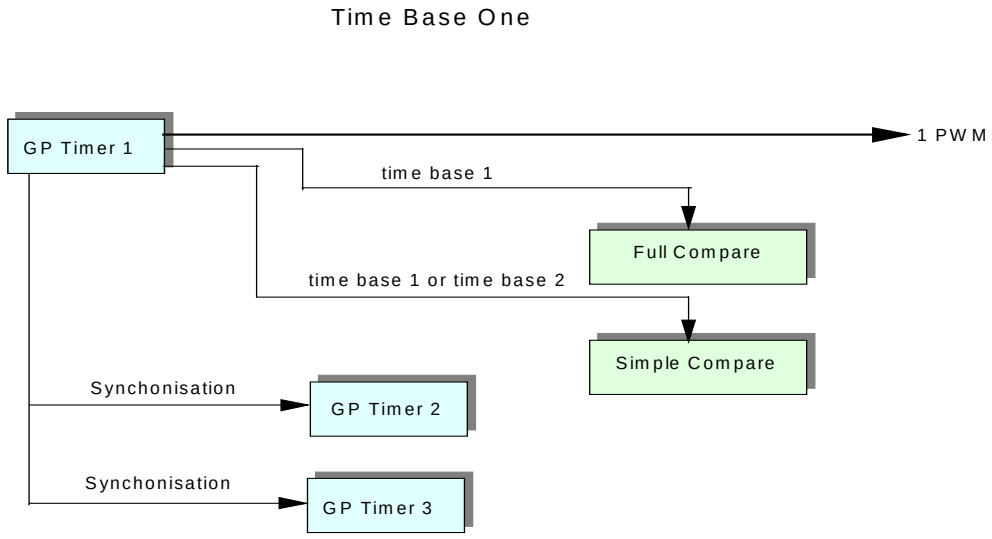


- To generate a time base for the Compare and/or the Simple compare module.

Three pairs PWM (Full Compare) are exclusively based on the Time Base One. Three PWM (Simple Compare) can be connected to the Time Base One or Time Base Two.

- To generate a time base for GP Timer 2 and GP Timer 3.

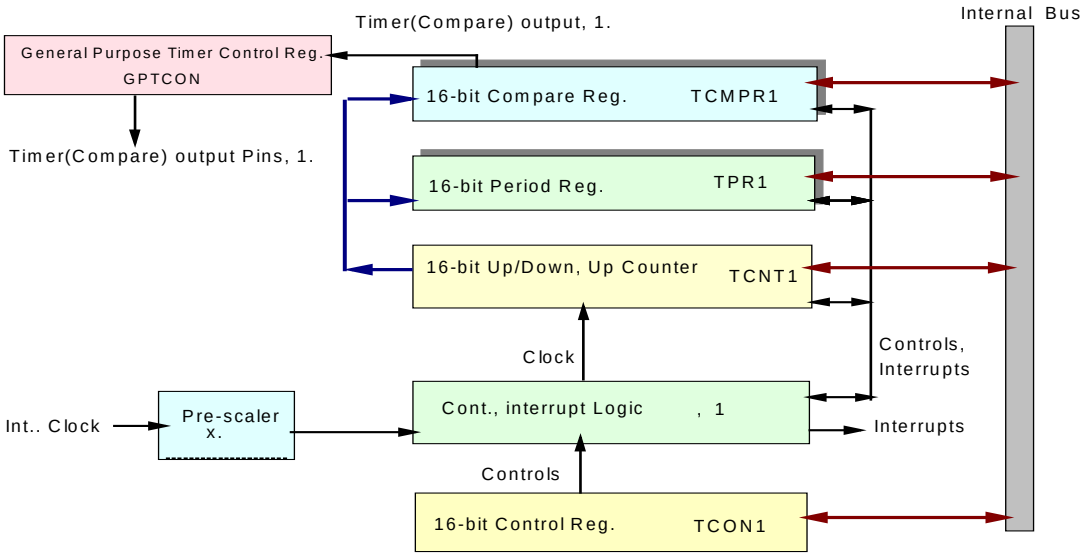
Time Base Two or Three can be independent or both synchronous to Time Base One.



- To generate a time base with Period modification on the fly.
- To generate a **time base for QEP, Capture, ...**

2. Description : Event Manager Programming

2.1 Timer Composition



2.2 Preparation Phase for Timer Configuration

The preparation phase for timer configuration is to:

- write GPTCON to determine action on GP Timer 1 compare output pin (active low, active high, forced low, forced high)
- write TPR1 : Timer Period register.
- write TCMPR1 : Compare Period register.
- write TCNT1 : Counter Period register.
- write TCON1 with bit 6= 0b (timer disable)
  : Control register to program Count Mode Selection, Clock Prescaler, Clock Source, compare reload condition, enable compare operation .
- write TCON1 with bit 6 =1b to start the timer.
  : Control register to enable the Timer 1

2.3 Calculation for the Time Slots in the Asymmetric Case

Calculation for the timer slot in the asymmetric case is defined by the following equation:

- **PWM cycle time**: T_{PWM}=TPER+1 timer counts. TPER is the value programmed into the period register for the PWM time base counter.
- **ACTIVE pulse width**: Ton=TPER-CMPR+1 timer counts. This equation is only true for any CMPR value up to TPER+1. If CMPR is 0, the output is active for the entire PWM cycle. If CMPR is equal to TPER, the output will be active for one timebase count. If CMPR is equal TPER+1 or greater, the output will remain in its INACTIVE state.
- **INACTIVE pulse width**: Toff=CMPR timer counts.

2.4 Example

Timer 1 is programmed to generate an Up Count with an asymmetrical PWM.

- Free run, no emulation mode.
- Timer count mode Continuous Up-Count Mode.
- No timer input pre-scaler and internal clock.
- Reload the shadow compare register when counter equal 0.
- PWM output Active High.

- Period: 6 * 50ns.
- Compare: 4 * 50ns.

```
GPTCON          =  042h
                Bit 1&2          : 10b  ,State of GP Timer 1
                                        compare output active High.
                Bit 6            : 1b   ,All 3 GP Timer outputs are
                                        enabled (no High Impedance
                                        State).
TPR1            =  5h
TCMPR1          =  3h
TCNT1           =  0h
TCON1 (first)   =  9002h
                Bit 1            : 1b   ,Enable timer compare
                                        operation.
                Bit 2&3          : 00b  ,Compare Register reload
                                        when counter is zero.
                Bit 4&5          : 00b  ,Internal Clock source
                                        selected.
                Bit 6            : 0b   ,Timer 1 Disabled and
                                        prescaler reset.
                Bit 11,12&13: 010b      ,Continuous-Up Count Mode.
                Bit 14&15        : 10b  ,GP timer not affected by
                                        emulation suspend.
TCON1 (second) = 9042h
                Bit 6            : 1b   ,Timer 1 is enabled.
```

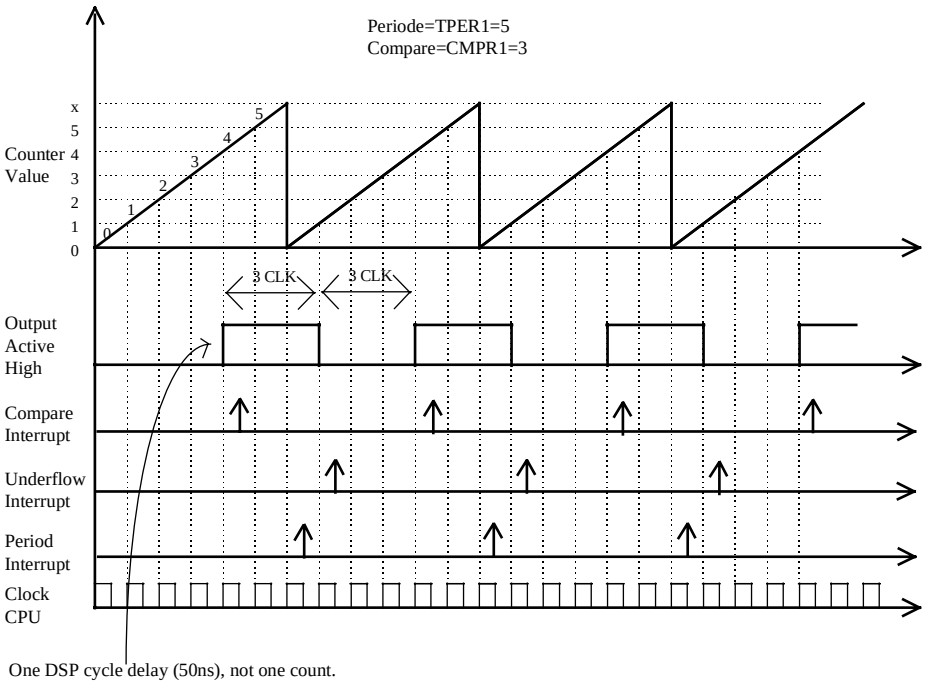
Initialization Assembly code:

```
        ;Note : GP timer registers are memory mapped.

GPTCON .set   7400h      ;General Timer Controls
TCNT1  .set   7401h      ;T1 Counter Register
TCMPR1 .set   7402h      ;T1 Compare Register
TPR1   .set   7403h      ;T1 Period Register
TCON1  .set   7404h      ;T1 Control Register

        LDP    #232
        SPLK   #42h,GPTCON
        SPLK   #5h,TPR1
        SPLK   #3h,TCMPR1
        SPLK   #0h,TCNT1
        SPLK   #9002h,TCON1
        SPLK   #9042h,TCON1
```

Result of this Example:



Note:
The first period of a continuous Up Count is 1 DSP cycle longer.

2.5 Modification of the Active Width During Running

When a new compare value in the CMPR1 register is written, the new value is loaded in timer register and is active at the end of the period, when TCNT1=0 (for this base configuration).

Example:
CMPR1 switches from 3 to 4 during the second period the result will be: