TMS320F206 DSP Development Board

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Nico Lee

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TEXAS INSTRUMENTS

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Abstract

This application report describes the configuration of the Texas Instruments (TI™) TMS320F206 development board (DVB). The standalone DVB allows TMS320 DSP users to evaluate TMS320F206 (’F206) DSP pin-compatible devices and determine if the ’F206 meets their application requirements.

TI’s ’F206 is the first DSP with on-chip flash memory available at an attractive price for volume products. The ’F206 features 32K words of non-volatile re-programmable flash memory with coefficient on-chip storage. Flash memory is more flexible than ROM, costs less than SRAM, and allows the design to reduce board size as well. The ’F206 is fabricated with static CMOS integrated-circuit technology and is optimized for low power operation.

The ’F206 architecture is based on TI’s TMS320C2xx series design. The new TMS320C2xx (’C2xx) generation offers the power of digital signal processing to designers of high-performance, cost-sensitive, and emerging applications. The ’C2xx generation is based on TI’s C2xLP core with different configurations depending on the choice of on-chip memory size and peripheral options.

The ’F206 DVB is also an excellent platform from which to develop and verify the software code for the ’C2xx DSP family. Customers can design their specific development system through the board-to-board expansion connector that offers the on-board signals.

Product Support

Related Documentation

TMS320C2xx User's Guide, Literature number SPRU127B

TLC320AC01 Data Sheet, Literature number SLAS057D

TLE2064, TLE2064A, TLE2064B, TLE2064Y Excalibur JFET-Input High-Output-Drive µPower Quad Operational Amplifiers, Literature number SLOS48D

TMS320F2xx Data Sheet, Literature number SPRS050

World Wide Web

Our World Wide Web site at www.ti.com contains the most up-to-date product information, revisions, and additions. New users must register with TI&ME before they can access the data sheet archive. TI&ME allows users to build custom information pages and receive new product updates automatically via email.

TMS320F206 DVB Overview

The ’F206 DVB consists of a 100-pin PQFP (plastic quad flat pack) layout and 100-pin evaluation socket . Both low-cost and device-changeable configurations are available. Users can utilize all of the available ’C2xx software tools (compiler, assembler, etc.) as well as hardware tools such as the TI XDS-510 emulator through an on-board JTAG port.

The ’F206 DVB includes a design option for an on-board clock input source or external clock source (through an expansion connector) used to implement the power-down function. In addition, a jumper switch is available to disconnect the on-board analog interface circuit (AIC) chip from the DSP and enable the external AIC chip.

Key Features

The ’F206 DVB offers the following key features:

- TMS320F206 fixed-point DSP with optional 100-pin evaluation socket
- Up to 40 MIPS (25 ns instruction cycle time)
- On-board 32K words data memory and 32K words program memory
- On-chip 32K words Flash memory for the ‘F206
- On-chip timer
- Programmable, voice-quality TLC320AC01 AIC (DAC, ADC interface)
- Socketed oscillator
- Phase-locked-loop (PLL) clock generator
- On-board UART with RS232 driver
- External RESET signal for the watchdog type reset feature
- External clock source option to the ’F206 DSP for clock-down function
- 96-pin expansion connector of I/O and control signals for external designs
- On-board IEEE 1149.1 JTAG connection for optional emulation
- Single 5 V only operation

- Standard 1/8-inch mono mini-jacks for analog I/O (microphone and multimedia speakers)

Key Features of the TMS320F206 DSP

The ’F206 DSP includes the following key features:

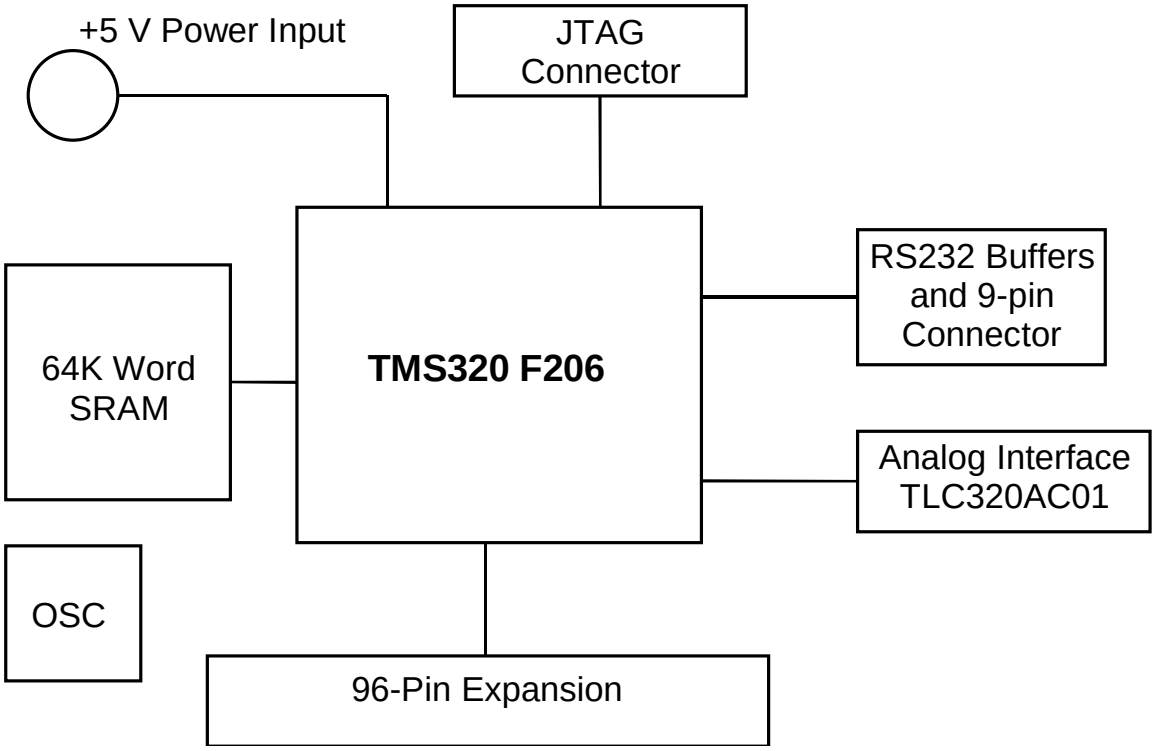
- Peripherals
  - On-chip 16-bit timer
  - On-chip software-programmable wait-state (0-7) generator
  - On-chip oscillator
  - On-chip PLL
- Integrated memory
  - 544 x 16 words of on-chip, dual-access data RAM
  - 32K x16 words of on-chip Flash memory
  - 4K x 16 words of on-chip, single-access program RAM
- 224K x 16-bit maximum addressable memory space
- On-chip PLL
- 32-bit ALU/accumulator
- Input clock option: x1, x2, x4, and /2
- Power-down idle mode
- Source compatible with TMS320C25 and upwardly compatible to TMS320C5X

TMS320F206 DVB Configuration

Figure 1 shows a block diagram of the basic DVB configuration, including the following major interfaces:

- ’F206 DSP
- ’F206 socket
- JTAG connector
- On-board program and data memory
- Analog interface
- Target UART
- Expansion interface

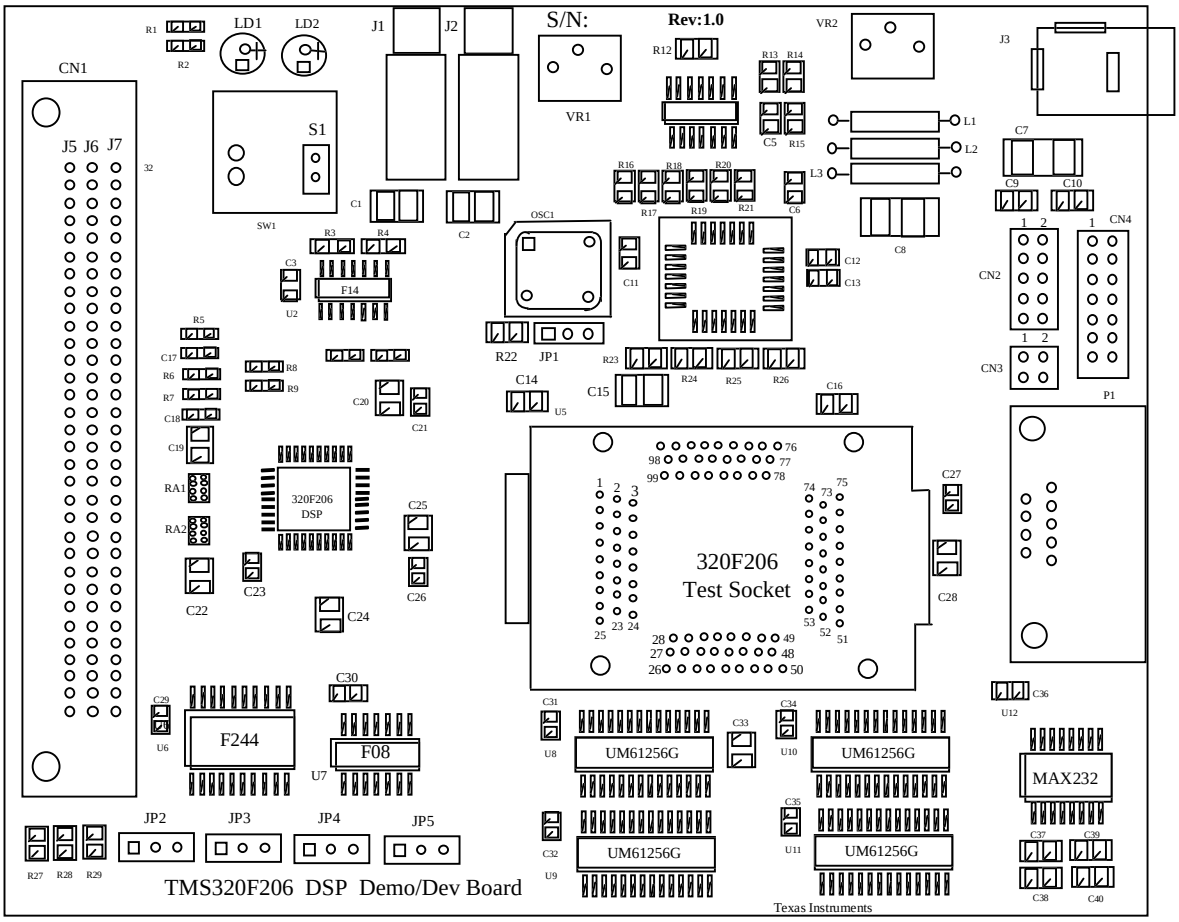
Figure 1. TMS320F206 DVB Block Diagram



Board Outline

The DVB measures 110 mm by 117 mm (see Figure 2).

Figure 2. TMS320F206 DVB Outline



Power Supply

The DVB requires at least 950 mA powered by a 5 V only, 3.3 A external power supply. Power is supplied via a 2 mm jack (**J3**).

NOTE:
If expansion boards are connected to the DVB, a higher amperage power supply may be necessary.

The onboard power LED (**LD2**) helps users identify the power on-off status. The board is designed with a cold reset button to allow users to reset all system components.

Clock Source Options and Oscillator PLL Selection

The DVB is designed with an internal clock source or external clock source option. For the internal clock source, the board is equipped with a 10 MHz oscillator with a multiply-by-two PLL option for the system clock. However, you can change the divide or multiply option via the jumper block, as defined in Table 1.

Table 1. Jumper Settings for the Internal Clock Divide or Multiply Options

Jumper JP3 (DIV1)	Jumper JP4 (DIV2)	PLL Options
1-2	1-2	0.5X
2-3	1-2	1X
1-2	2-3	2X
2-3	2-3	4X

Use the jumper settings listed in Table 2 to select the clock source for CLKIN of the ’F206 DSP.

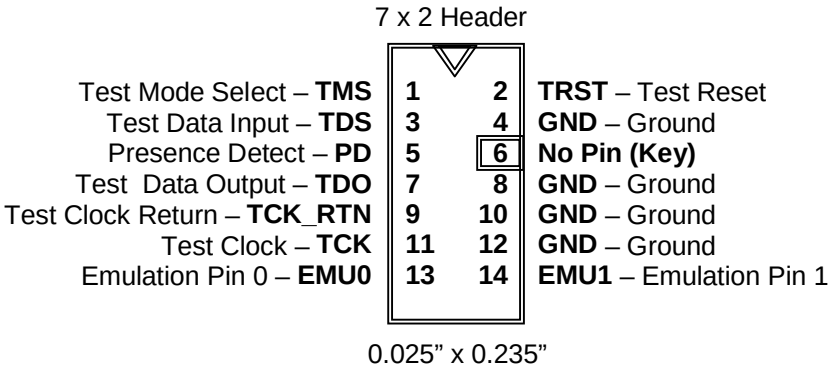
Table 2. Jumper Settings for CLKIN Clock Source Selection

Jumper JP1	Clock Source Selection
1-2	External clock source from expansion slot
2-3	Internal clock source from on-board OSC1

JTAG Interface

The DVB is designed with a 14-pin header to connect the DSP with an external standard IEEE 1149.1 interface used by JTAG emulators (such as the TI XDS-510 emulator). Figure 3 shows the header pin assignments.

Figure 3. DVB Header Pin Assignments



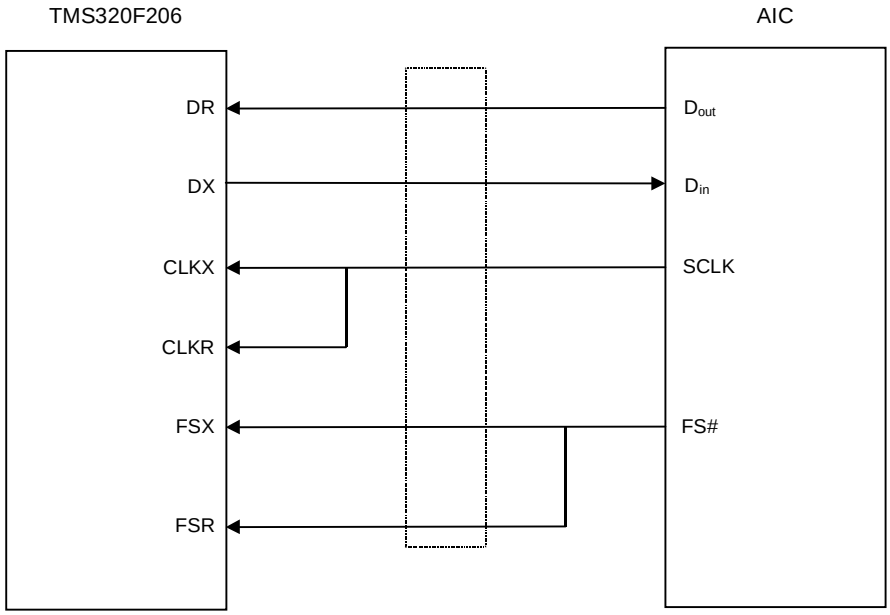
Analog Interface

Use the ’F206 synchronous serial port to access either the on-board TLC320AC01 AIC or an audio-band codec, or use it to jumper to an external codec through the expansion connector. This feature offers you an additional choice for specifying codecs in your application. The 5-position jumper platform (**CN2**) interconnects the serial port to AC01. Set the jumper in the disconnecting configuration to select the external codec.

Connecting the TMS320F206 DSP and TLC320AC01 AIC

Figure 4 shows the signal connections between the ‘F206 DSP and the AIC.

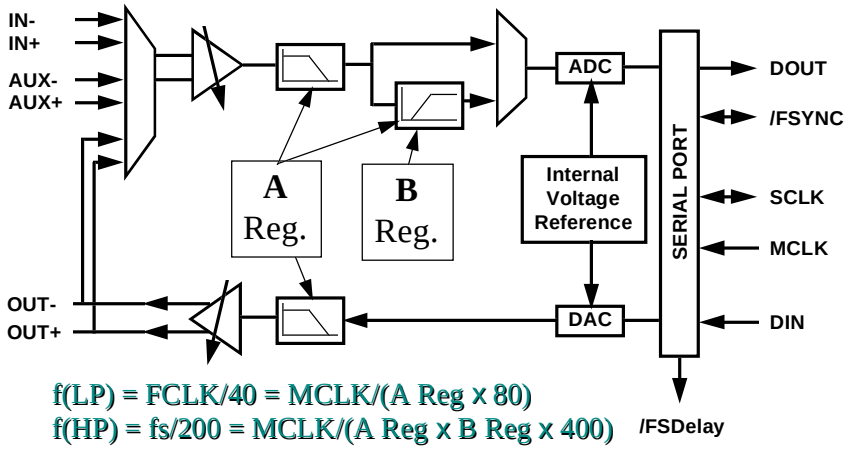
Figure 4. Block Diagram for the TMS320F206 DSP and AIC Connections



Basic TLC320AC01 AIC Features

The TLC320AC01 AIC is an audio-band signal processor that integrates a band-pass switched-capacitor anti-aliasing input filter, a 14-bit-resolution ADC (analog-to-digital converter), a 14-bit DAC (digital-to-analog converter), a low-pass, switched-capacitor, output-reconstruction filter, (sin x)/x compensation, and a serial port for data and control transfers. The AIC operates on a single 5 V power supply with a programmable output gain of 0 dB, -8 dB, -18 dB, and squelch. Figure 5 shows the functional block diagram:

Figure 5. AIC Functional Block Diagram



Analog Input and Output

The analog input is driven by either a standard mini-jack (**J2**) (used for a microphone connection) or an expansion connector. The analog output is driven either to another standard mini-jack (**J1**) (used for a multimedia speaker) or to an expansion connector.

Expansion Bus

The ’F206 DVB is designed with a 96-pin board-to-board DIN connector to interface with another board. The expansion bus executes the TMS320C2xx powered-up condition with seven wait states. However, the ready signal can be asserted if a longer access time is required.

Table 3 lists the pin assignments for the expansion bus.

Table 3. Pin Assignments for the Expansion Bus

Pin	Signal	Signal	Signal
1	+5 V	+5 V	+5 V
2	Data 0	Data 1	Data 2
3	Data 3	Data 4	Data 5
4	Data 6	Data 7	Data 8
5	Data 9	Data 10	Data 11
6	Data 12	Data 13	Data 14
7	Data 15	Address 0	Address 1
8	Address 2	Address 3	Address 4
9	Address 5	Address 6	Address 7
10	Address 8	Address 9	Address 10
11	Address 11	Address 12	Address 13
12	Address 14	Address 15	XRESET#
13	GND	GND	GND
14	XRW#	XDS#	XIS#
15	NC	NC	READY
16	INT2	RESETI#	FSX
17	XCLKOUT	FSR	CLKIXR
18	DR	DX	NC
19	BR	AUXIN+	AUXIN-
20	INT1	HLDA	NC
21	NC	NC	IO 3
22	NC	NC	NC
23	GND	GND	GND
24	IO 0	IO 1	IO 2
25	NC	NC	XF
26	NC	BIO	NC
27	ADCIN+	NC	NC
28	GND	NC	DACOUT+
29	XCLK	XSTRB	NC
30	GND	GND	GND
31	XRD#	XWE#	XPS#
32	GND	GND	GND

Asynchronous Serial Port

The ’F206 DSP has an on-chip asynchronous serial port interface (**P1**) that consists of an RS232 female connector (DB9). P1 connects to a computer or instrument external to the DVB. Figure 6 shows the pin positions for P1 viewed from the edge of the DVB.

Figure 6. P1 Pin Positions (DVB Edge View)

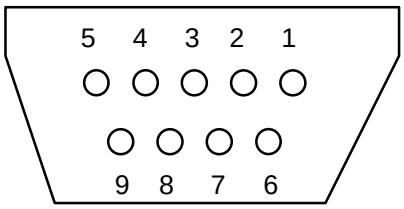


Table 4 lists the pin numbers and corresponding signals between the ’F206 and P1.

Table 4. P1 Pin Assignments

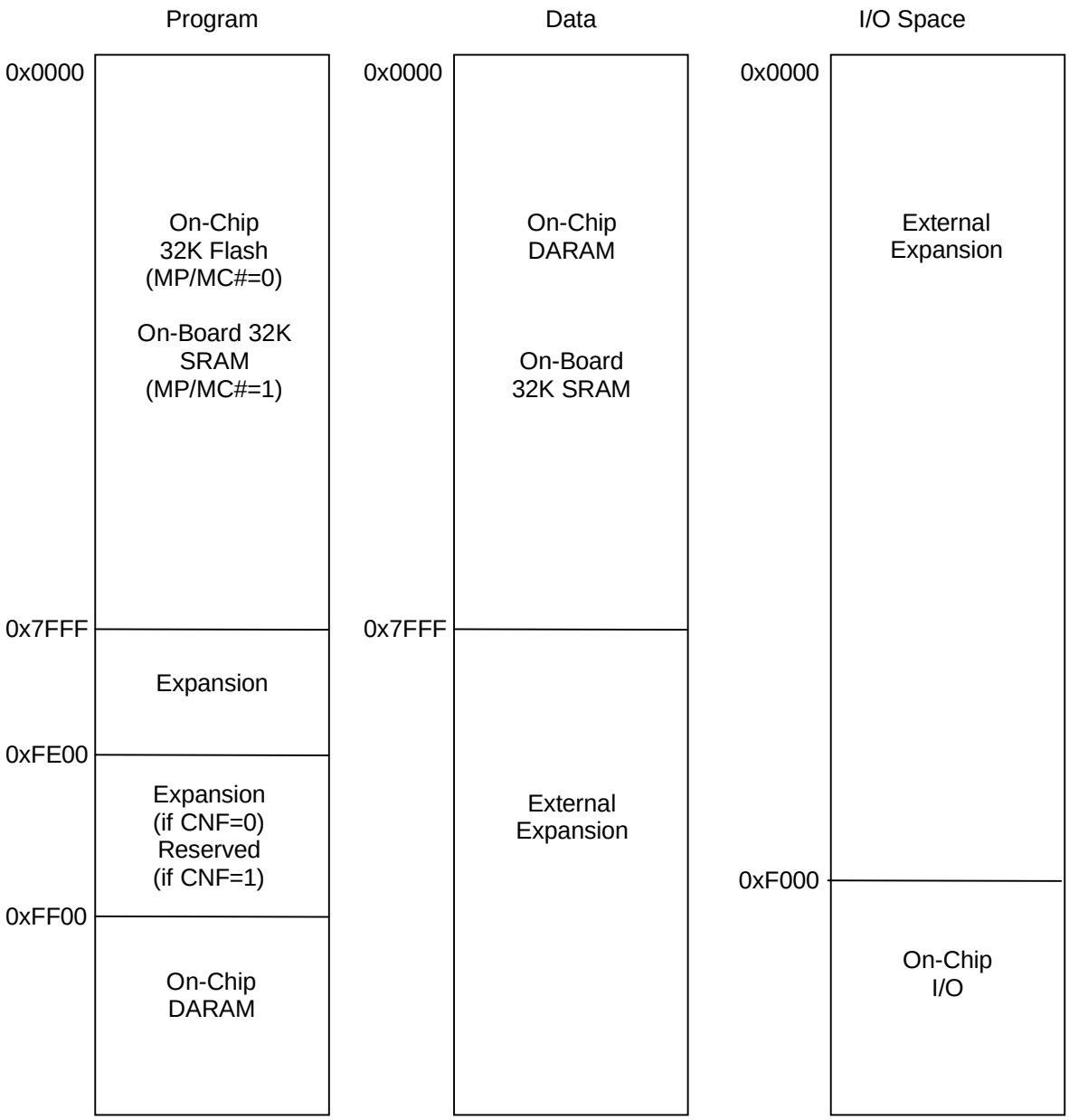
Pin #	Signal	F206 Signal	Direction
1			
2	TX	TX	OUT
3	RX	RX	IN
4			
5	GND		
6			
7	RTS-	I/O 1	OUT
8	CTS-	I/O 0	INT
9			

Memory and I/O Space

The ’F206 DVB implements three separate address spaces for program memory, data memory, and I/O, as shown in Figure 7. Each space accommodates 64K words.

The DVB includes 32K words of program memory on board and 32K words of data memory in an off-chip configuration. In this configuration, the **JP2** jumper must be at 1-2 close (that is, Pin MP/MC# = 1). The on-chip 32K words of Flash memory are enabled as the program memory space if the **JP2** jumper is in 2-3 close configuration during reset.

Figure 7. TMS320F206 DVB Address Spaces



On-Chip Flash Memory Programming

The ’F206 has built-in 32K 16-bit words Flash memory, which makes an external ROM design unnecessary and thus increases board space. For the Flash programming scheme, TI offers two approaches (with software utilities) that allow you to download the program into the Flash space.

First, the Flash memory can be programmed through the JTAG port with the XDS-510 hardware emulator. The programming procedures are:

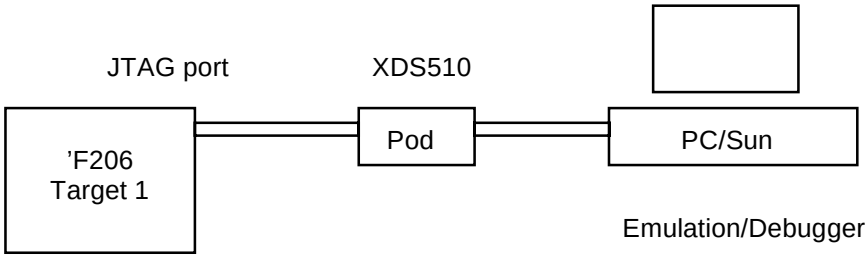
1) Clearing to 0 in all bits

2) Erasing to 1 in all bits

3) Writing 0 in selected bits

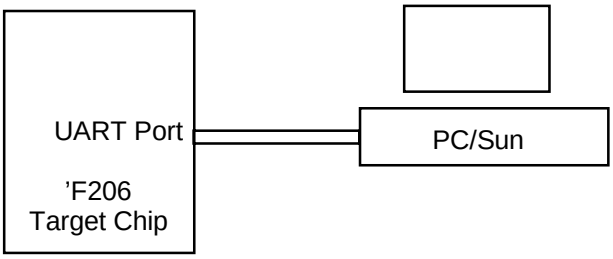
Figure 8 shows the on-chip Flash programming interface connection.

Figure 8. On-Chip Flash Programming Interface



Second, the Flash array can be programmed through the asynchronous serial interface from the UART port of the host station (see Figure 9). TI provides the Flash serial loader and PC/host serial communication utility (for updated software and documentation, see the *World Wide Web* section in this document).

Figure 9. TMS320F206 Serial Loader Interface



General Purpose LED

The on-board LED (**LD1**) allows you to monitor the state of the BF pin easily. You can also use it for test or development purposes.

Appendix A. Bill of Materials

Table 5 lists the TMS320F206 DVB Bill of Materials (BOM).

Table 5. TMS320F206 DVB Bill of Materials

Item	Quantity	Reference	Part	Manufacturer
1	3	CN1-C,CN1-B,CN1-A	CON32	AMP 650473-5
2	1	CN2	Header 5x2	
3	1	CN3	Header 2x2	
4	1	CN4	Header 7x2	
5	2	C2,C1	15 µF, ceramic	
6	19	C3,C6,C9,C12,C13,C14,C16, C18,C21,C23,C26,C27,C29, C30,C31,C32,C34,C35,C36	0.1 µF, ceramic	
7	9	C4,C7,C15,C19,C20,C24, C25,C28,C33	4.7 µF/16 V, tantalum	
8	2	C22,C8	10 µF/16 V, tantalum	
9	2	C10,C11	470 pF, ceramic	
10	1	C17	27 pF, ceramic	
11	4	C37,C38,C39,C40	0.1 µF, ceramic	
12	1	D3	Diode, 1N914A	
13	5	JP1,JP2,JP3,JP4,JP5	Header 3	
14	2	J2,J1	mini-jack	Shiua-Chuyan Co. SCJ-0352-1
15	1	J3	DJ005A	Shiua-Chuyan Co. SCD-014
16	2	LD2,LD1	LED, MLED71	
17	3	L1,L2,L3	Inductor, 800 Ohm/ 100 MHz	
18	1	OSC1	10 MHz	
19	1	P1	DB9	
20	2	RA1,RA2	4.7 KX4	
21	14	R1,R2,R7,R9,R10,R11,R20, R23,R24,R25,R26,R27,R28, R29	4.7 K	
22	11	R4,R5,R12,R13,R14,R15, R16,R17,R18,R19	10K	
23	1	R3	47	
24	2	R6,R22	22	
25	1	R8	0	
26	1	SW1	Toggle switch	
27	1	U1	Operational amplifier, TLC2274C	Texas Instruments
28	1	U2	74F14	Texas Instruments
29	1	U3	TLC320AC01/AC02	Texas Instruments

30	1	U4	TMS320F206	Texas Instruments
31	1	U6	74F244	Texas Instruments
32	1	U7	74F08	Texas Instruments
33	4	U8,U9,U10,U11	UM61256G	
34	1	U12	MAX232	Texas Instruments
35	2	VR2,VR1	100K	

Appendix B. TMS320F206 DVB Schematics

This appendix design contains the set of DVB schematics.

Figure 10. TMS320F206 DSP Schematic

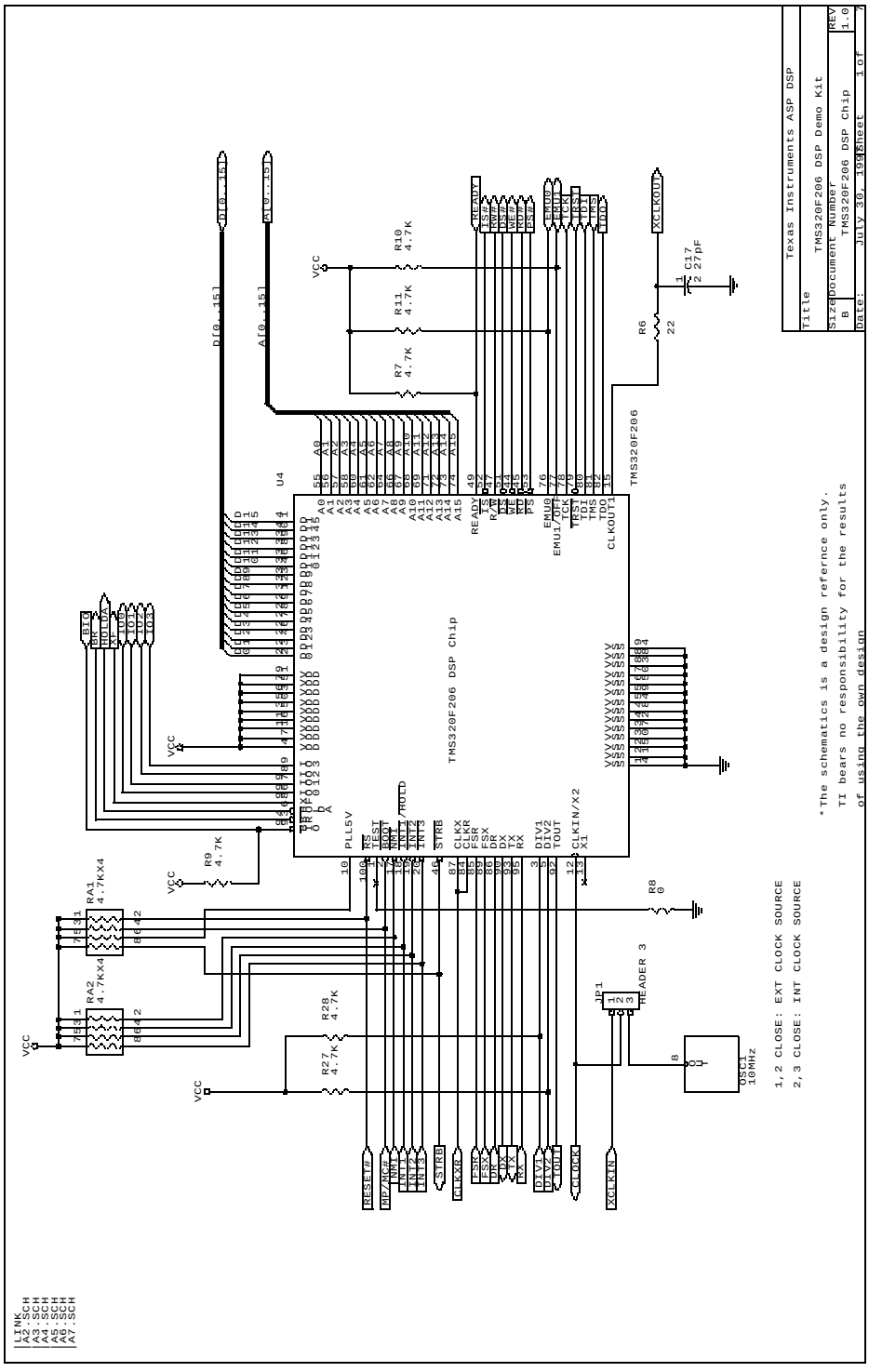


Figure 11. DVB 5 V Power Supply System Schematic

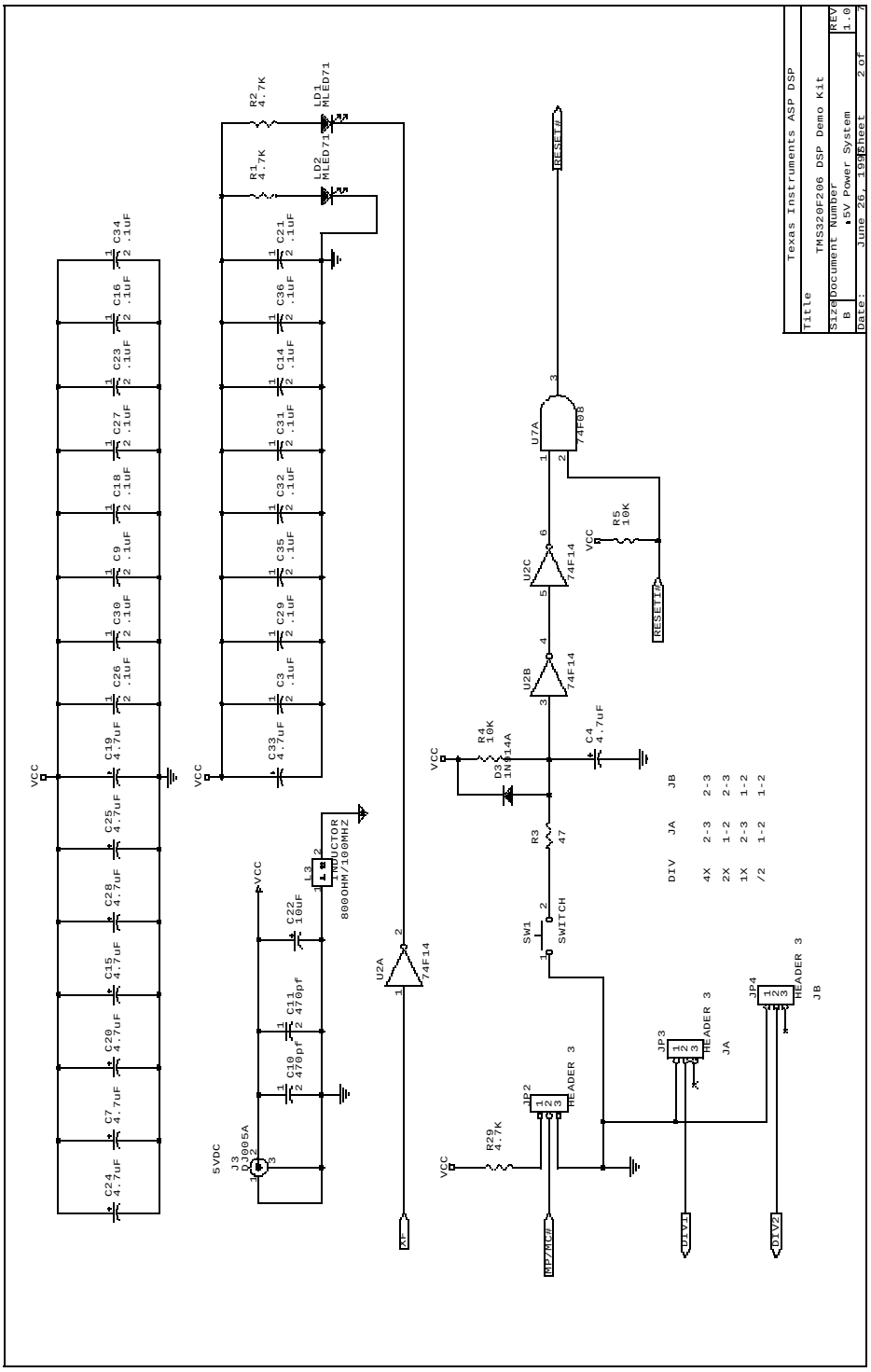


Figure 12. TLC320AC01 AIC and TLE2064 Operational Amplifier Schematic

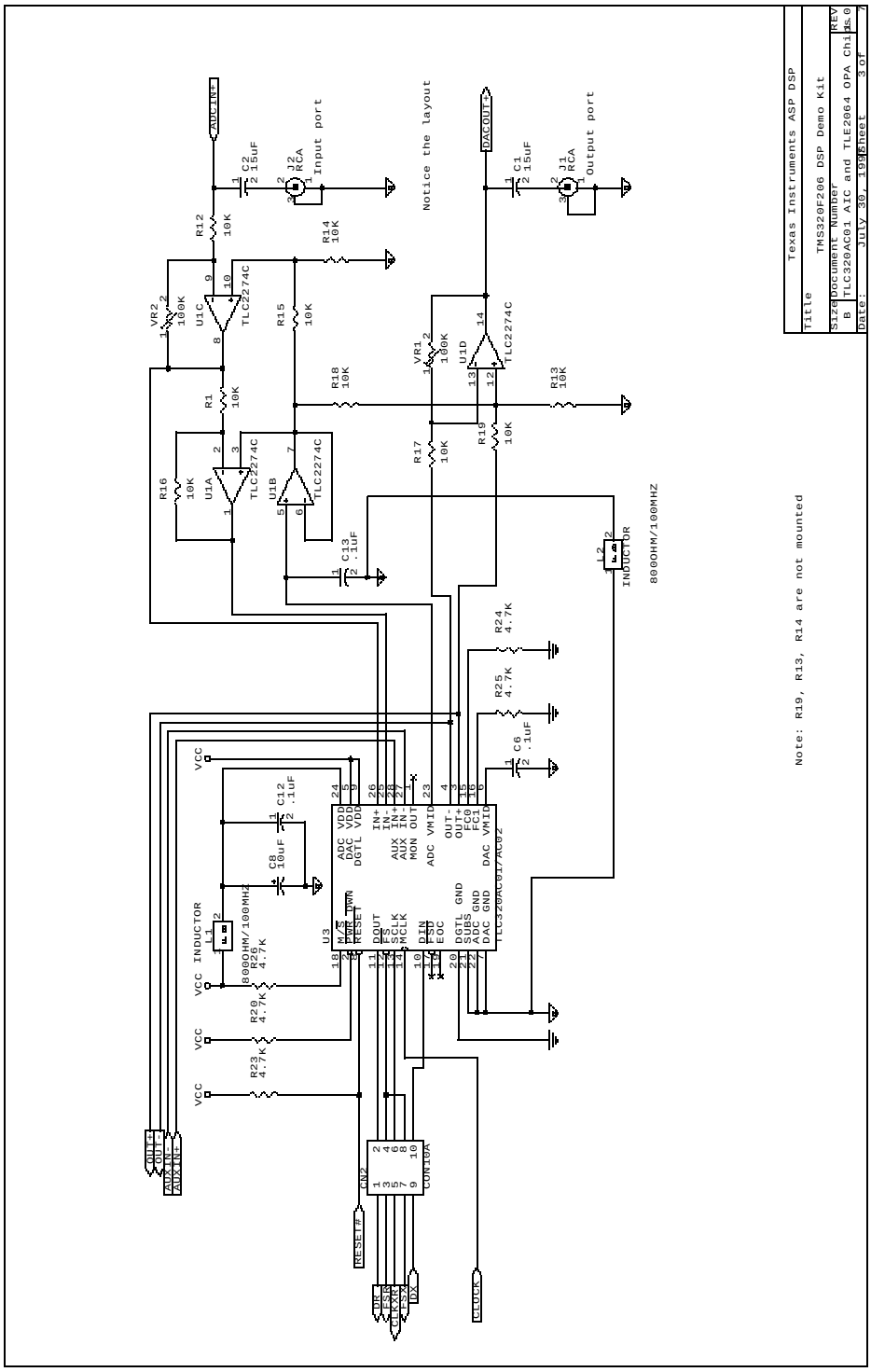


Figure 13. On-Board SRAM Schematic

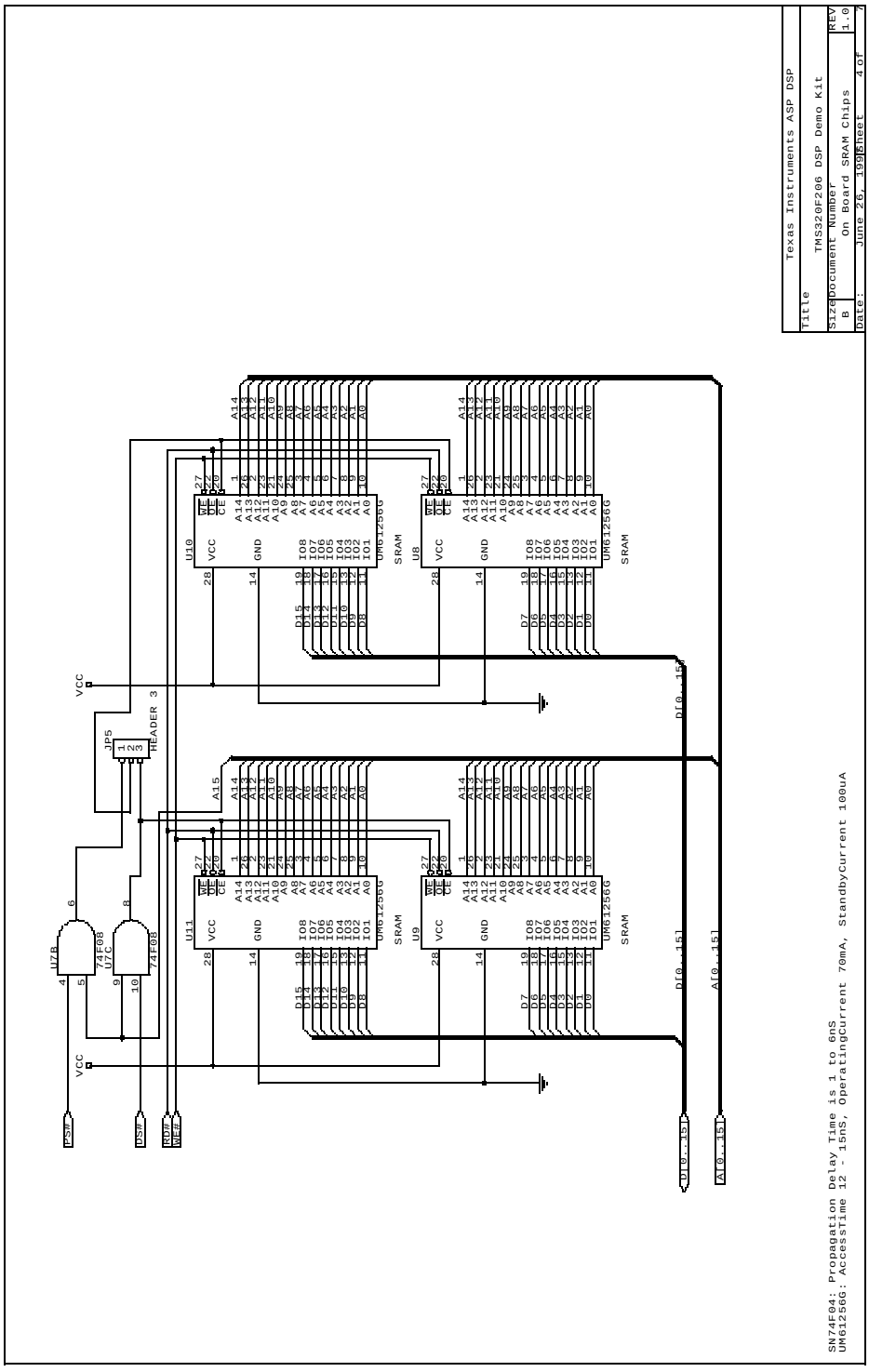


Figure 14. JTAG 7x2 Header Schematic

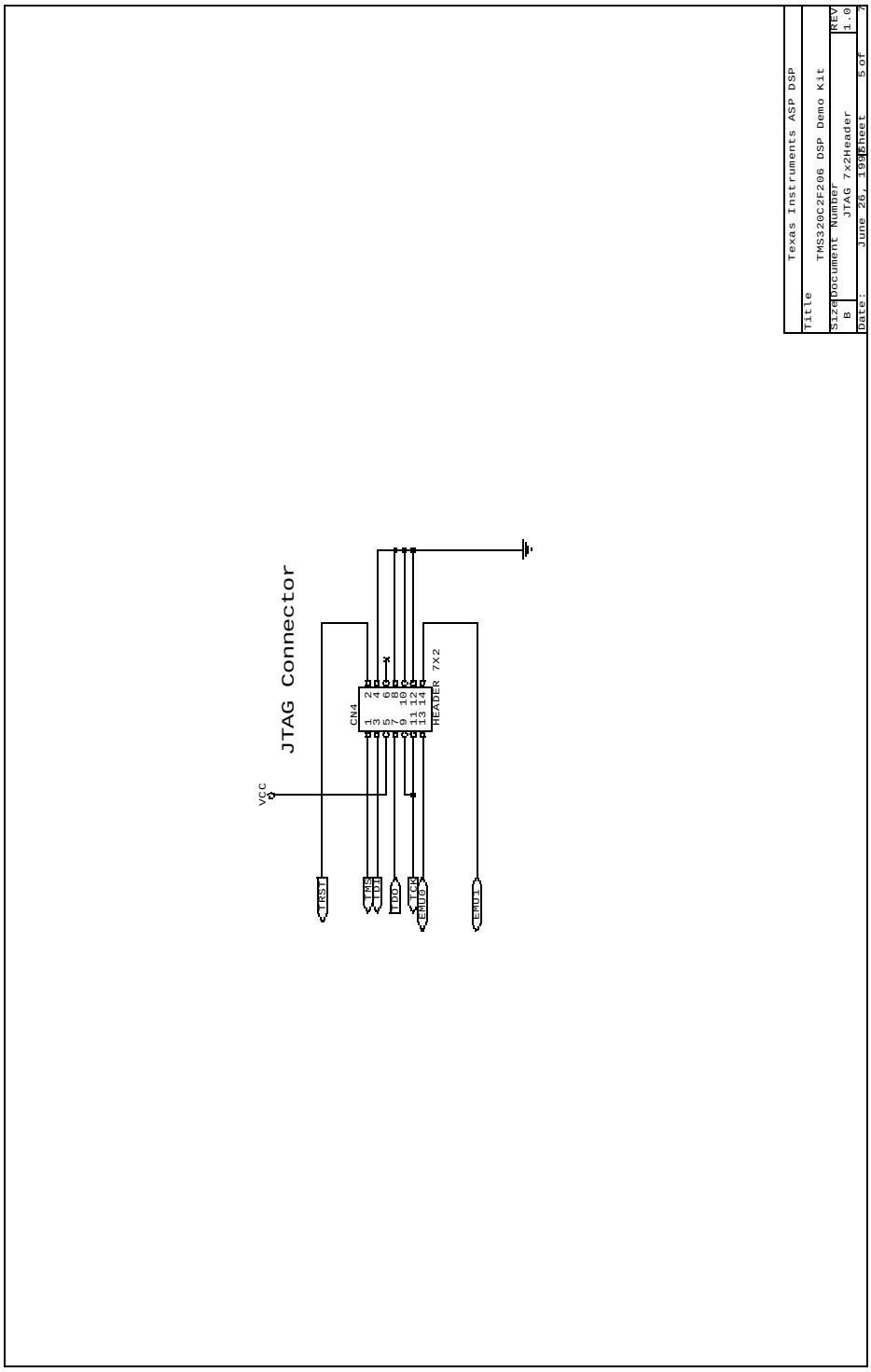


Figure 15. RS232 Connector (DB9) Schematic

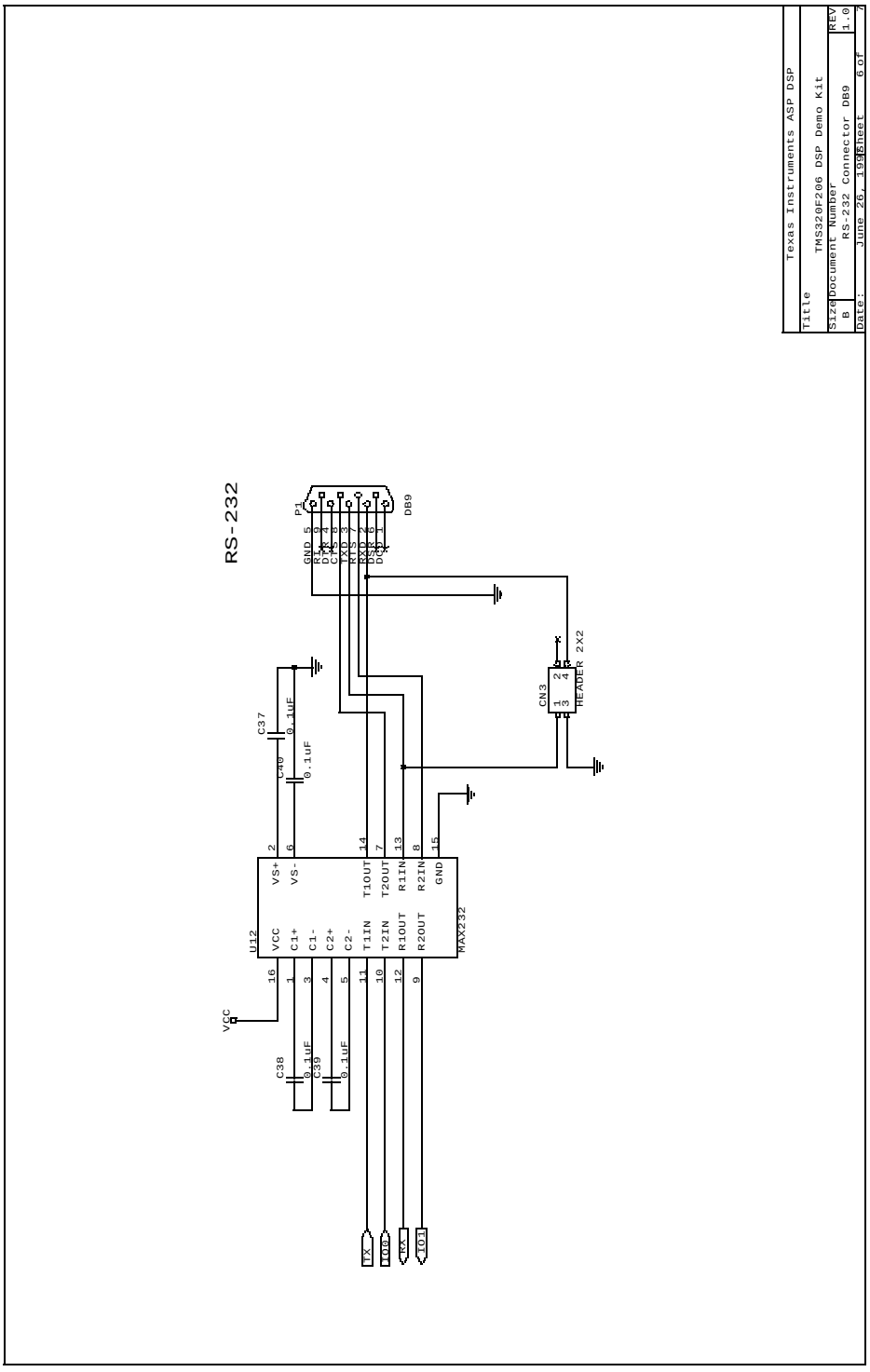
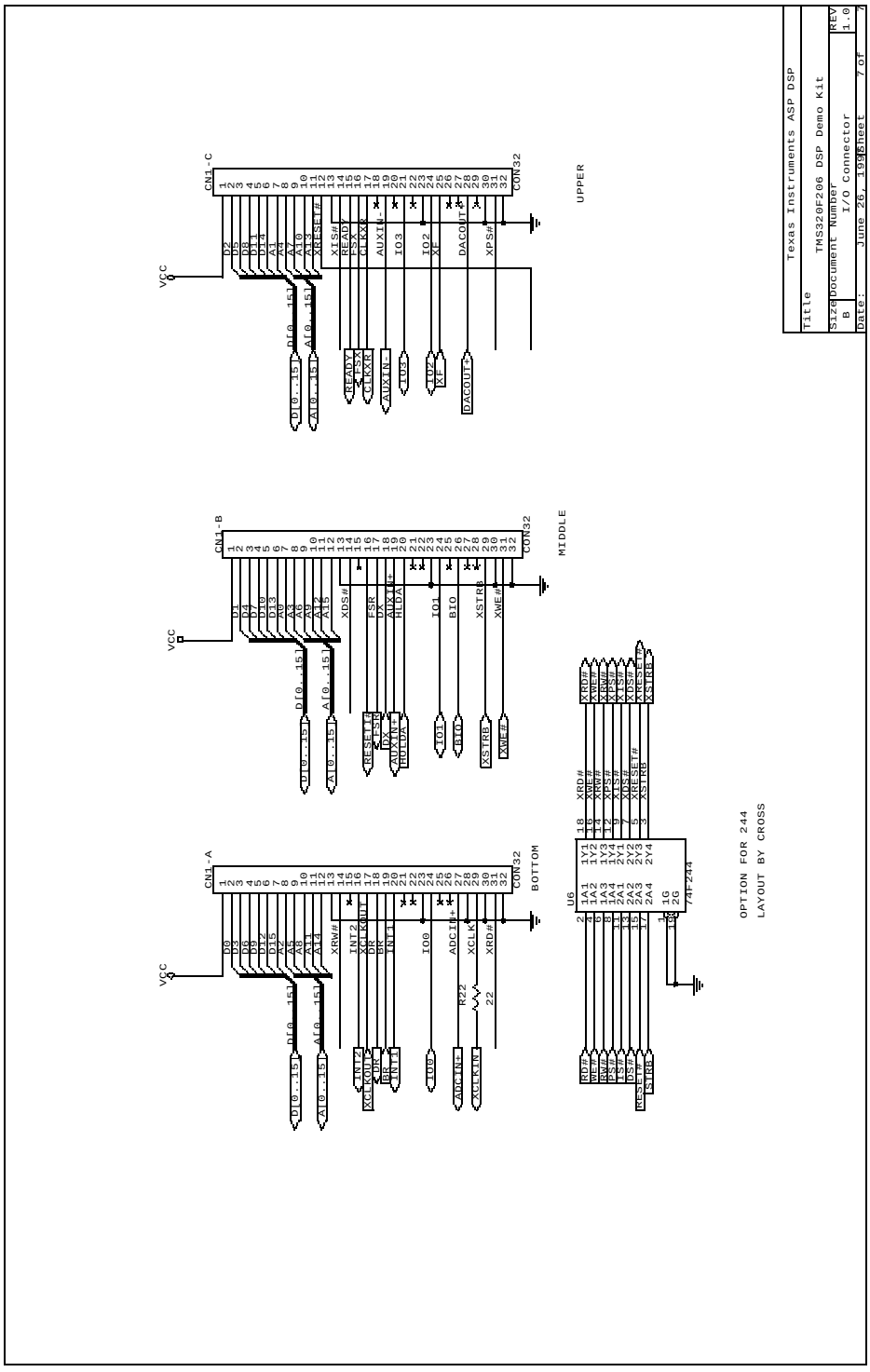


Figure 16. I/O Connector Schematic



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