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Digital Signal Processors vs. Universal Microprocessors

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ESIEE, Paris

September 1996
SPRA344

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Digital Signal Processors vs. Universal Microprocessors

Abstract

Digital Signal Processors have approximately the same level of integration, the same clock frequencies as general purpose microprocessors. Even usually general purpose microprocessors have advantage in these fields. But on signal processing tasks DSPs overtake them from 2 to 3 order in speed. This is because of architectural differences. Among them are

- Arithmetic Unit architecture
  - specialized units (multipliers, etc.)
  - regular instruction cycle (RISC-like architecture)
  - parallel processing
- Harvard Bus architecture
- Internal memory organization
- Multiprocessing organization
  - local links (TMS320C40)
  - memory banks interconnection (TMS320C80)

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Introduction

Digital signal processing requires a large amount of real-time calculations. For example it needs about 0.3 sec to fulfil Fast Fourier Transform for N=1024 using Turbo Lab program on personal computer IBM PC/AT-386. With the help of TMS320C30 crystal the (approximately of the same generation as 386 microprocessor) such transform can be implemented at 1.5 ms.

Digital Signal Processors have approximately the same level of integration, the same clock frequencies as general purpose microprocessors. Even usually general purpose microprocessors have advantage in these fields. But on signal processing tasks DSPs overtake them from 2 to 3 order in speed. DSPs speed advantage over universal microprocessors is achieved due to optimization of their architecture to specific tasks.

It must be said that some features of DSP in some time are included in more resent universal microprocessors but not vice versa. In all cases because of there more complex tasks DSPs leads universal processors in technical innovations.

This is a part of DSP chapter of the lecture course "Signal Processing Fundamentals" for the 5th year students from Radio Engineering and Cybernetics Dep. of Moscow Institute of Physics and Technology.

Arithmetic unit

The most common operation in digital signal processing is the sum of products calculation $S=\Sigma a_i b_i$. Among such operations are well known convolution and Discrete Fourier Transform. The most complex arithmetic operation in digital technique is multiplication. For example in universal 8086 microprocessor an addition takes 3 clocks, rather than (fixed point) multiplication 134-160 clocks. In usual tasks multiplications make up to 1% of overall operations. For this reason such complex arithmetic device as multiplier is not usually included into universal microprocessors. But for digital signal processors multiplication is a major task - and a multiplier is a necessary component of any DSP.

To increase the speed, digital signal processors usually have many specialized arithmetic units, which can operate simultaneously. To calculate the sum of products, typical DSP operation, all DSPs have multiplier and accumulator and two operations multiplication and addition can be implemented during one cycle. Some DSPs can fulfil simultaneously even FFT butterfly. All DSPs contain shifter to shift operands without loss additional time.

Universal CISC (complex instruction set computer) microprocessors have a large variety of command cycle duration. In 8086 microprocessor addition - 3 clocks and multiplication - more 100 clocks. Digital Signal Processors are designed for real-time calculation. Fixed sampling rate leads to necessity to have regular instruction cycle. Such regular instruction cycle is achieved in RISC (reduced instruction set computer) microprocessors by restricting the instruction set. But in DSP the same is achieving by hardware increasing the speed of important complex instructions, for example multiplications.

Bus architecture

Universal microprocessors were designed simple and cheap personal computers. They have the simplest Von-Newman bus architecture: common command and data space, single data and address bus. When microprocessor performs any instruction it must read it from memory, decode it, then read operand, then perform calculation. It takes a large amount of time. Each command can have only one operand from memory (second from register).

All Digital Signal Processors have Harvard architecture with different program and data buses. DSPs can read instruction and data from memory simultaneously and improve the speed of calculation. Almost all DSPs have modified Harvard architecture with three buses: one program and two data. It allows DSPs read instruction word and two operands simultaneously. In signal processing applications necessity of two operands from memory is a usual case.

Addressing

Digital signal processors are designed to process a large data arrays. In some cases address calculations takes more time, than arithmetic operations on data itself. In 8086 microprocessor (register-register) addition takes 3 clocks, but the calculation of executive address - 5-12 clocks. DSPs as a rule have hardware support data array calculations. They contain specialized arithmetic units - address generators. Due them address calculation need no additional time.

Modem microprocessors as a matter of fact also have separate address generator. In particular, autoincrementation or autodecrementation can be made ,without time loses, but DSPs have advanced address generators. The can operate with arbitrary, but not only a unit step. Some DSPs have hardware support for binary inverse addressing, which is convenient for FFT. Besides Harvard architecture require many address generators.

Memory

Arithmetic operations usually require less time than memory transfers. In 8086 microprocessor register-register addition takes 3 clocks, rather than register-memory addition - 14-21 clocks. This is under condition that memory is faster enough to avoid waiting cycles, which is not a fact as a rule. Modern universal microprocessors usually contain advanced cache, but don't have any ROM or RAM for programs or data. It is because of the wide variety of huge programs, used by universal microprocessors. Some times even hard disc is not enough for generally used programs. DSP algorithms while require a huge calculations are very simple as a rule. Corresponding programs are comparatively short and can be located straight on chip, which can decrease transfer time. DSPs are usually highly specialized which permit to locate programs in ROM (PROM). Besides ROM for programs DSPs contain data RAM. ROM and RAM are usually integrated in one-crystal microcomputers, but the main reason there is to decrease the cost rather than to increase the speed.

Multiprocessing

Digital Signal Processors are designed for real-time calculations and sometimes the number of operations is very large and more than one microprocessor is needed. Universal microprocessor based systems have a single common bus structure. All units (memory, controllers, etc.) are connected to processor data and address bus. Such architecture is simplest and fully adequate to common purpose microprocessors designed for cheapest systems. When you increase the number of microprocessors, connecting them to the common bus, such common bus restricts the possibility of information exchanging between microprocessors. It must be said that parallel implementation of DSP algorithms requires as many transfers as arithmetic operations. For this reason the performance of common bus architecture is not proportional to the number of microprocessors or doesn't grow at all. It is very difficult to develop multiprocessor system based on common purpose microprocessors without many additional hardware.

Signal processor TMS320C40 has 6 local links for processors interconnection. Due to local links any two microprocessors can make data exchange separately from another DSPs. Such local links technique is development of transputer technology.

In TMS320C80, containing 5 microprocessors, data exchange is organized through common memory (RAM), divided by 25 blocks. Processors can be switched between them. Each processor at any moment works with its own memory bank and don't interfere with other processors.