Implementing a Multi Signal Processing System for High Speed Monitoring of FACTS-Equipment in Electrical Power Systems Using the TMS320C50 DSP

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Implementing a Multi Signal Processing System for High Speed Monitoring of FACTS-Equipment in Electrical Power Systems Using the TMS320C50 DSP

Abstract

Flexible AC Transmission Systems (FACTS) are thyristor based means for highly dynamic load flow control in electrical power supply and distribution. These new appliances have an impact on network parameters like transmission angle, node voltage, line current and harmonics. Thus the control of FACTS equipment provides a highly dynamic view of these parameters. For this purpose we developed the digital prototype of a Network Online Monitoring System (NOMS) which is based on a multi-signal processing architecture to monitor the influence of FACTS-equipment on the power system. It includes the recording and analogouse processing of test input signals, A/D and D/A conversion and various methods of digital signal processing such as complex digital filtering, space phasor blocking and discrete Fourier transformation. Real-time signal processing requires high calculation power that is provided by the parallel processing architecture of TMS320C50 with a flexible global and local memory management, high-speed bus arbitration and a smart PC/AT-interface for long-term investigations and controls. The software algorithms are specified, for power systems and comprise several levels of processing priorities optimizing the available calculating time. A prototype of a NOMS has been successfully tested in a Transient Network Analyzer (TNA) of power supply and distribution systems at our University.

This document was an entry in the 1995 DSP Solutions Challenge, an annual contest organized by TI to encourage students from around the world to find innovative ways to use DSPs. For more information on the TI DSP Solutions Challenge, see TI's World Wide Web site at www.ti.com.

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Introduction

To fulfil the increasing requirements of power supply and distribution systems, the aspects of economy, reliability and quality are becoming more important. In modern public power networks of power supply the node voltage and line current signals are distorted or not sinusoidal at least. For example, the following reasons can be stated:

- Application of modem FACTS-equipment for static var compensation, transmission angle control and load flow dispatching.

Figure 1. Examples of FACTS Devices

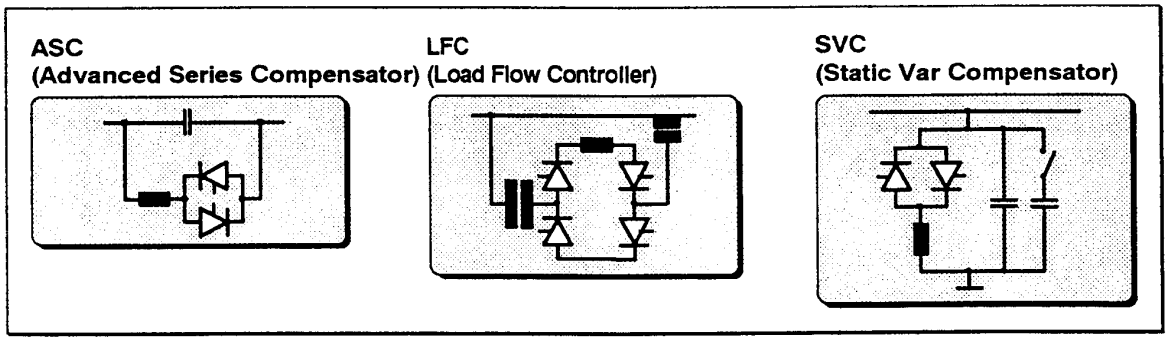


Figure 1 shows examples of FACTS devices. The advanced series compensator is employed to control and to reduce the transmission angle in long distance transmission lines. With a LFC system you can get a suitable power dispatch in interconnected networks like the European UCPTE- network. The SVC improves the reactive power management for voltage control. All FACTS devices are based on thyristor or GTO valves. Thus these devices influence the network with switching actions and transient responses. Dangerous resonance phenomenon occur.

- Supply and feeding of a not sinusoidal current signal with non linear means as HVDC back-to-back or long distance and industrial appliances
- Single phase loads produce negative sequent rotating systems in the network distorting the symmetrical conditions,
- Speed controlled motor drives based on modern power electronic equipment.

The resulting transient responses, non-symmetrical conditions, flicker and harmonics produce interactions and instabilities reducing the quality and reliability of power systems considerably. The NOMS should record the distorted signals and analyze them to find a way to improve network conditions. There are many kinds of network distortions. Therefore, the NOMS must be based on different test methods to investigate the network troubles. Following types of methods are necessary:

- Analysis of network harmonics and distortion with state phasor blocking
- Measurement of line power with complex phasors of the momentary power flow,
- Synchronous subtraction of absolute value and phase angle of complex voltage phasors at several nodes in the network
- Selective acquisition of voltage and current values in a three-phase system
- On-line calculation of the network conditions
- On-line influencing and output of new parameters for the FACTS control

These features were taken into account developing the NOMS. The following chapters will show how these requirements were realized with a prototype that is based on the digital signal processor TMS320C50. Especially in this process we have attached importance to the accuracy of the hardware components and on-line calculations and furthermore to varied test methods.

Description of the Network Online Monitoring System

Peripheral Components and Interfaces

Structural Overview

This chapter deals with the development, test and realization of the peripheral components of the NOMS. In this phase the main task was to create the interface circuits between the high voltage network and the control console and on the other hand side the signalprocessing system. For this aim, high speed A/D-converter systems for floating measurement of voltage and current state phasors and homopolar values are built up. The documentation of the test results was carried out with D/A-converter systems and a LCD-matrixdisplay. The on-line parameter control was managed by external keyboard system.

Figure 2. Schematic Diagram of the Peripheral Components of the NOMS

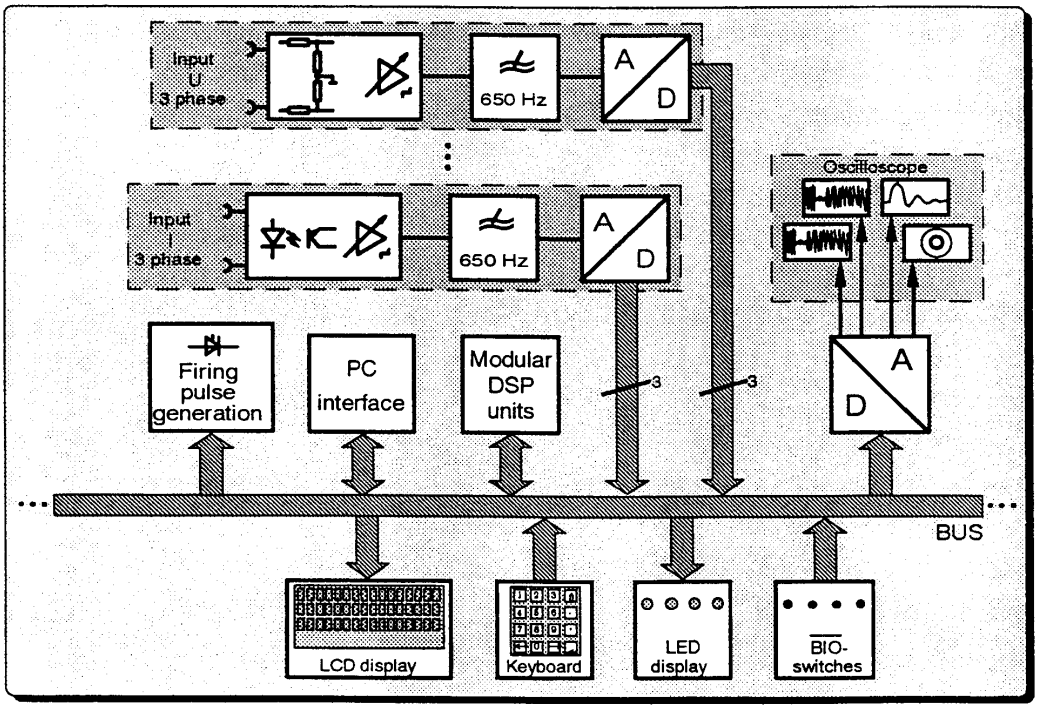
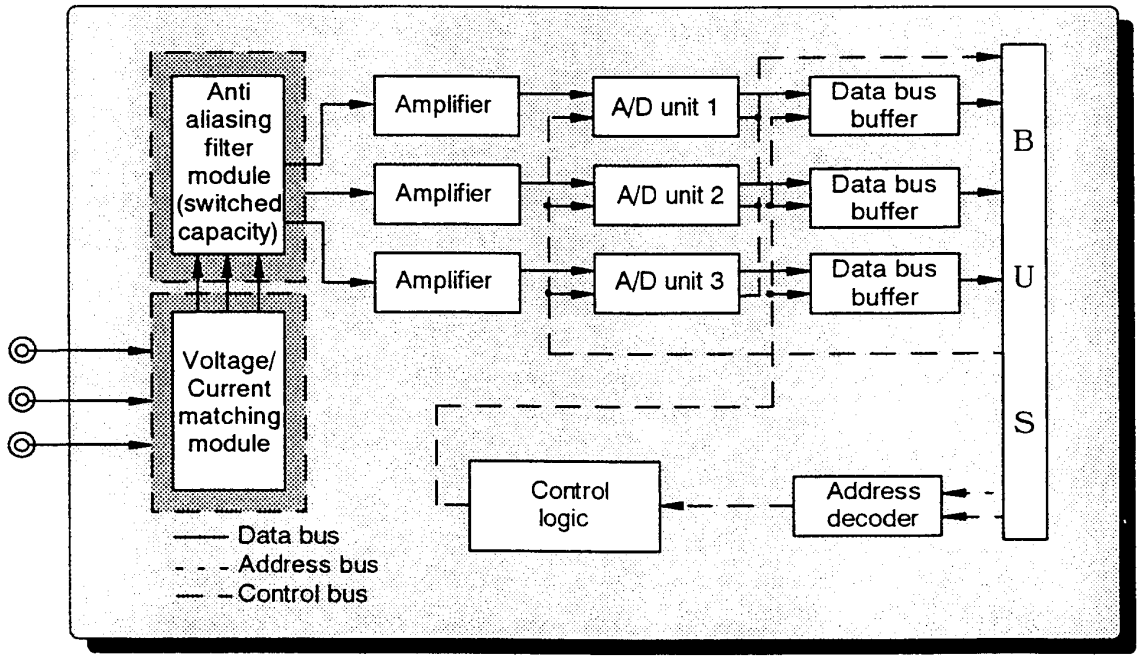


Figure 2 shows the schematic diagram of the peripheral components of the NOMS. The DSP units are based on the TMS320C50 digital signal processor. Up to seven units can be provided. To acquire the network information, there are up to eight available A/D-converters systems with active filtering for voltage and current acquisition. The PC-interface is used for data recording of long-term investigations and will provide an additional capability for controlling the NOMS. The test procedure can also be operated by the keyboard and BIO-switches and can be adjusted to special problem areas. The LED-indications show the topical state of the NOMS. The firing pulse generation system, which sends out the on-line calculated firing data from the signalprocessing system, is created to influence and to control the FACTS devices to a more stable operation point.

A/D Converter Systems

The A/D interface circuits are very important components of the NOMS. The accuracy of the A/D conversion of the voltage and current signals determines the quality and the reliability of the calculated results. Each A/D interface circuit consists of three input channels. After signal matching, the module with an optimized OP-amplifier circuit the signals are digitized and delivered to the data bus with high speed advanced BICMOS driver technology. An address decoder and a control unit provide for an faultless data transfer.

Figure 3. Schematic Diagram of the A/D Converter Systems



The scanning raster of all installed channels of the NOMS is synchronized to get an accurate subtraction result of the phase angle measurement in a power supply network. It is very important for a digital measurement in a power supply network to provide a sample data control unit adjusting the topical sample rate of the NOMS to the variable frequency of the power supply network. With the proper combination of sample control signals, it is possible to apply A/D circuits with a variable timing behavior.

The A/D converter system can be changed from a voltage acquisition system to a current acquisition system easily with a replacement of a plug and socket connected module circuit. The anti-aliasing filter circuit is available as a plug and socket connected module circuit. Later expansions or improvements of the NOMS can be comfortably integrated with additional plug and socket connected module circuits.

The voltage acquisition module provides a floating measurement for high voltage signals up to 2 kV with a simple differential amplifier circuit. There is no need for an optical isolation amplifier. Therefore we have no problems with non-linearity and pink noise. The test inputs can be changed from symmetrical to non-symmetrical voltage conditions.

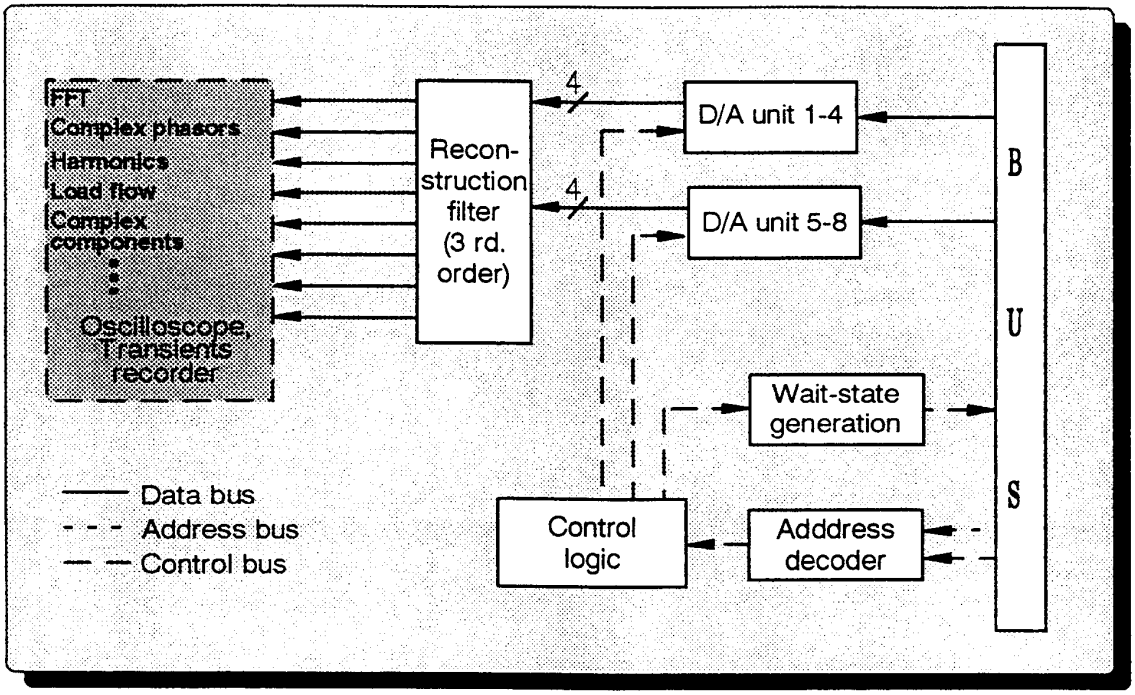
The current acquisition module is based on a series connected sensing device in the network transmission line. The isolation and amplification of the current signal is managed by a low-noise and linear OP-circuit. Thus we get accurate and original current signals on a very simple way. Both modules have an input protection circuit which prevents destruction of the interface circuits by dangerous voltage (above 2 kV) and current (above 100 A) levels.

D/A Converter Systems

The D/A converter system is much simplified when using high integrated four-in-one circuits. The D/A converter circuit contains an on-chip data latch. Thus, data bus transfer can be effected with a simple control unit very comfortable. The simple address decoder circuit (74F138) is enough for high-speed bus arbitration. A wait-state circuit provides a suitable timing between the D/A converter system and the signalprocessing system. Normally we are running our bus data transfer system with one wait-state. For each channel it also provided a reconstruction filter reducing signal distortions and glitches.

One D/A converter system is able to send out eight output signals synchronously. With the quadruple multiplexed D/A converter circuits, we can maintain a relatively low bus loading. This is very important for such a large input-output system. Besides the alternatively switchable wait-state circuit helps to avoid accidental data transfer errors when running the high-speed (up to 50 MHz) digital signal processors from Texas Instruments.

Figure 4. Schematic Diagram of the D/A Converter System



Keyboard/Display Interface

The keyboard as well as the display interface are connected to the signalprocessing unit with latch circuits. In this way the very short access time of the signalprocessing unit can be used and the relatively long access time of the keyboard/display circuit are decoupled and independently. A control unit is managing the right timing. The bus loading is reduced using advanced BICMOS bus drivers. Furthermore, the interface consists of an address decoder, the terminals for the display and keyboard, Flag-indication and BIO-switches.

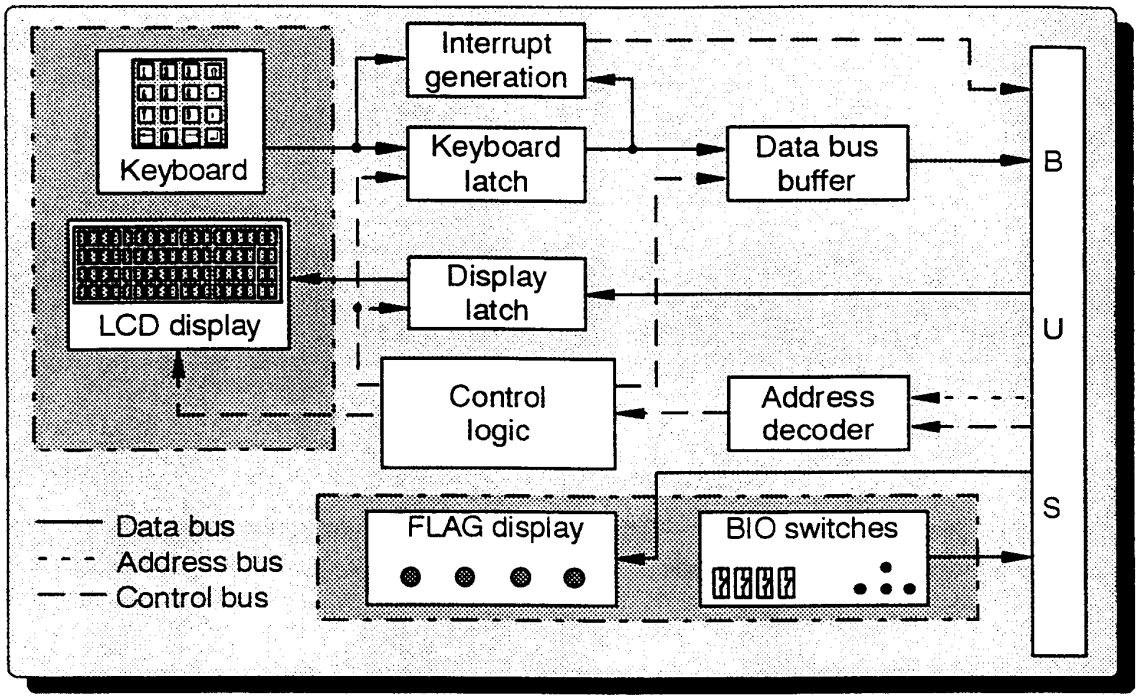
The keyboard can be interfaced by polling or interrupt. We have chosen the interrupt mode because polling produces a high bus load and, with the interrupt mode, we can enter keyboard data asynchronously. In addition, the TMS320C50 signal processor provides a software tool to handle the management of interrupts very comfortable.

There is also a circuit provided which makes the keyboard switches chatter-proof. The interrupt signal of the keyboard is also delayed to prevent input data errors. Consequently there is a decoupling of asynchronous inputs and output from the high-speed signalprocessing unit. To realize the varied facilities of the NOMS, in spite of the complex structure of the software program, and to get a simple handling of them, we have created a consistent on-line parameter input system. This user interface consists of the keyboard and the display described above. With them you can carry out an on-line entering of configurations data for measurement and analysis. It is possible to switch over to the features as:

- Selective acquisition of voltage and current values in a three-phase system
- On-line calculation of the network conditions
- On-line influencing and output of new parameters for the FACTS control
- Analysis of network harmonics and distortion with state phasor blocking
- Measurement of the line power with complex phasors of the momentary power flow
- Synchronous subtraction of absolute value and phase angle of complex voltage phasors at several nodes in the network

without interrupting the signalprocessing system. The documentation of the D/A output channels is normally provided by oscilloscope screens.

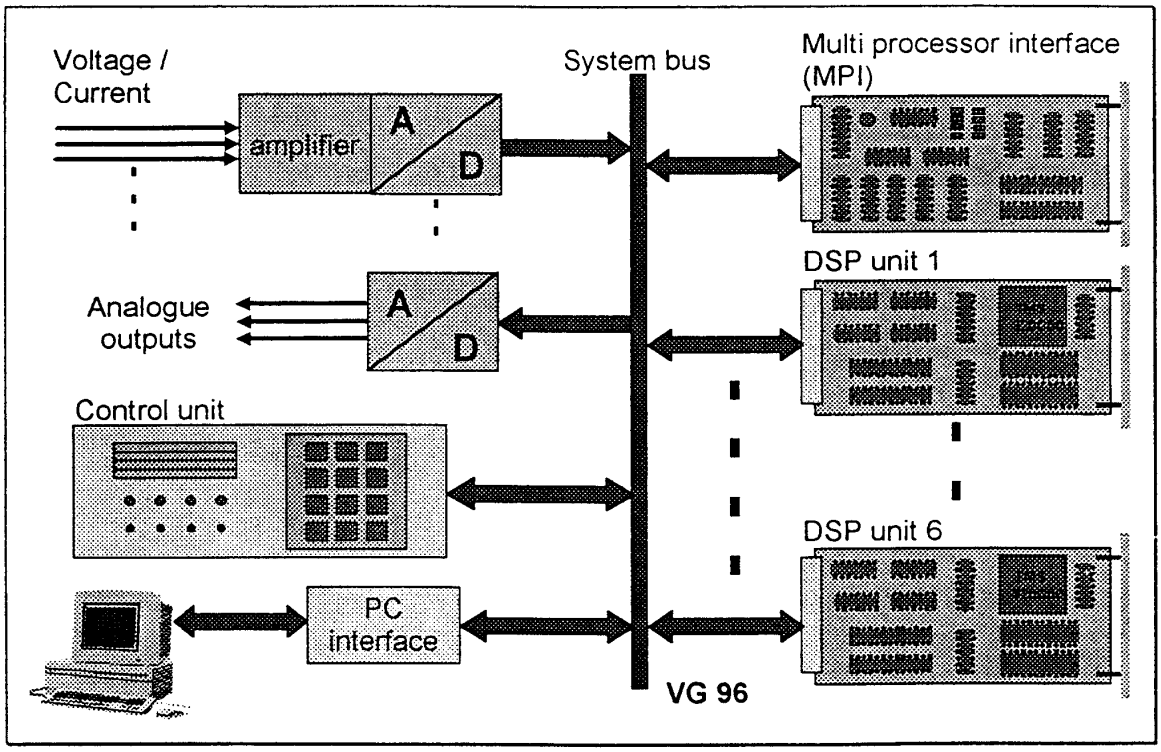
Figure 5. Schematic Diagram of the Keyboard/Display Interface



Multi-Signal Processing Architecture

It was an aim of our application to realize a system of independent DSP units without reducing the single processor performance noticeably. Thus we decided for a realization with up to seven equal DSP-applications which work as independent bus masters and are able to communicate via a common system bus. For communications there's a suitable interface, we called it Multi Processor Interface (MPI), with global memory (up to 32 kWord data RAM), a global 16 bit flag register and several unique functional units that will be described later. Accesses to the global data memory are performed in burst mode. This means that the MPI has its own address counter which is loaded by writing to a base address. Each following access only transfers data to the memory by increasing the base address on each access. This is realized by using different I/O-ports of the TMS320C50 which are decoded in a GAL (20V8) of the MPI.

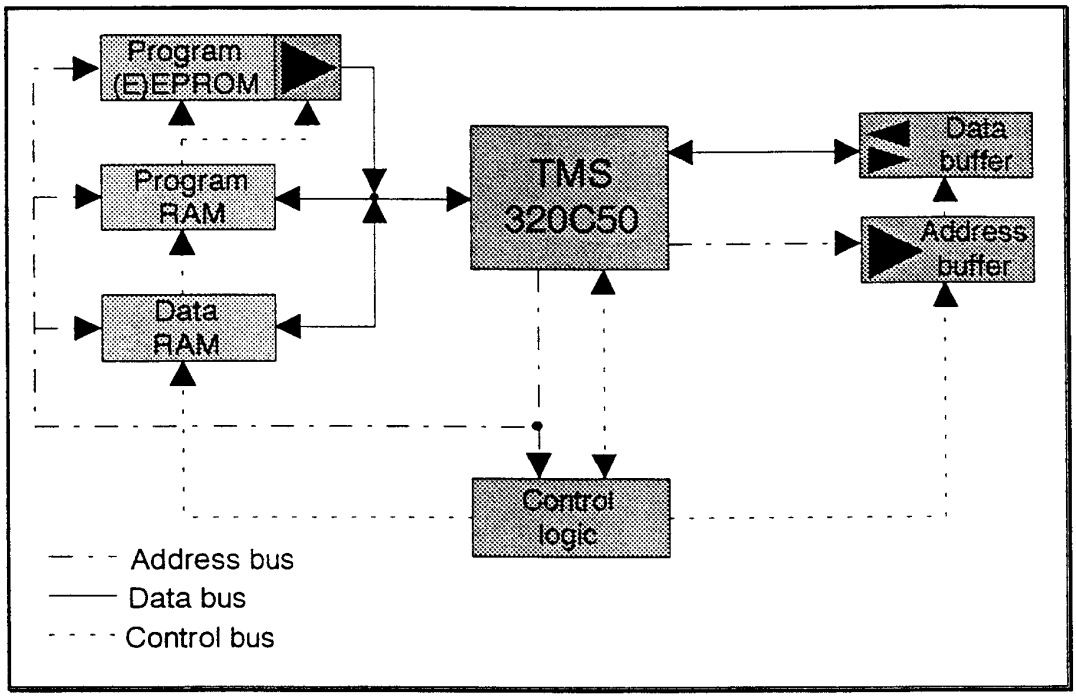
Figure 6. Overview of the Central Processing Components



Each DSP unit (Figure 7) is developed for stand-alone and communication mode. This means you can drive all 7 DSP units parallel without data transfer between the DSPs. So you can realize 7 independent functions. In this mode the DSP is using only its local bus and local memory. Local memory is provided with a 32 kWord program and 10 kWord of on chip RAM. Because of the high amount of on chip RAM, the TMS320C50 is an excellent match for this application. Consequently, for most kinds of applications in electrical power supply we do not need an external memory chip. Additionally, the internal bus allows full 16 bit data and 16 bit addresses so there's no need for address-data multiplexing. So we get a very good and cheap solution for the realization.

If the application needs more memory, external data and program memory accesses are realized by using the data-select or program-select outputs of the TMS320C50. There is also an additional feature: during the boot-procedure the program memory is selected in two buffered EPROM's which contain the program code. After this, a software variable called FLAG, is set to HIGH, which disconnects the program EEPROMS and enables the chip select of the program RAM. In this way, after the boot procedure with EPROM's we can use the whole program address area, from 0000h to FFFFh, and not just the usual higher memory addresses.

Figure 7. Architecture of the DSP Unit



The application was designed for different independent duties like controlling of external A/D and D/A conversion, performing communication with an external interface to PC and internal system control (Figure 6). A reliable bus accesses the different devices and avoids bus conflicts by using a bus arbitration unit based on the independent request method (Figure 8). So for external bus accesses, there is a single pair of wires that are used for bus request and for receiving the bus grant signal.

On the other hand you can communicate via the MPI with other bus masters. This is provided by the independent request bus allocation system (Figure 8) where the bus arbiter on the MPI grants the bus to the requesting master when there is no other use for it. The bus grant signal is connected to the internal READY-logic of the allocated DSP. This means if the DSP is going to perform an external bus access it sets its I/O select signal (/IS) LOW. So via the READY-logic, READY for the DSP stays LOW (not ready) until the bus grant signal, /ISB, is given by the arbiter logic. If more than one master is going to perform bus accesses at the same time the arbiter offers bus use to the requesting master. If bus access to one of the requesting masters is granted its local I/O select wire is switched to the bus. So this master can perform its accesses. All other requesting bus masters must then perform wait states while the bus is reserved. After this access is completed, the arbiter will store the release to the last master if there's a further bus access. The masters have different bus access rights depending on their logical number. But a bus master keeps the bus rights during his accesses. This option was also very important because one master who performs a series of data transfers to the global memory (burst mode) has to own the bus rights during this.

Figure 8. Independent Request Bus Arbitration Method

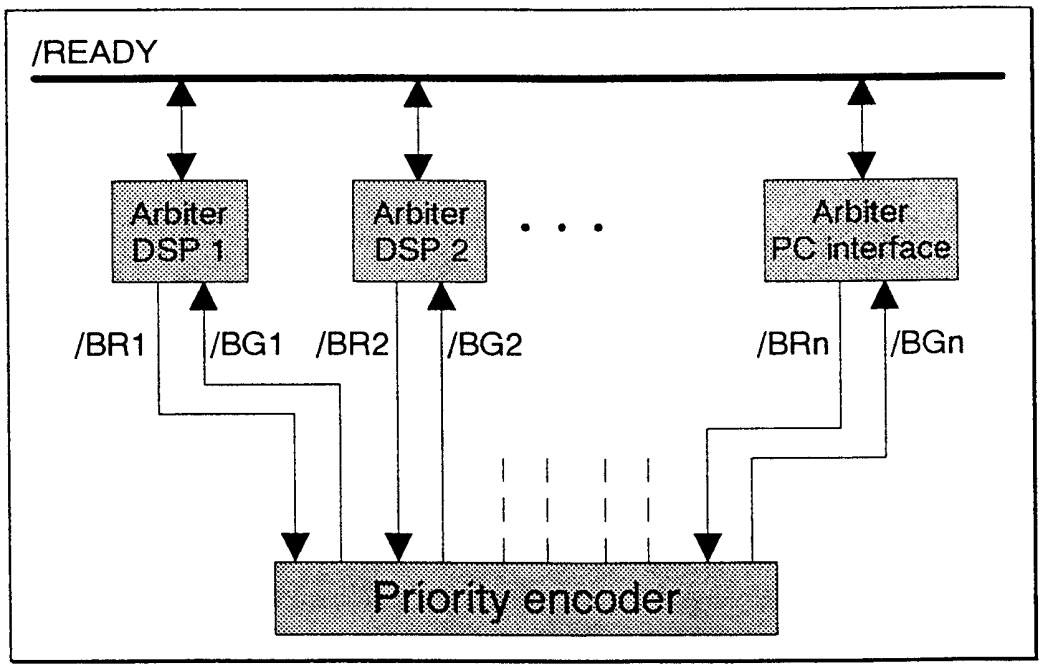
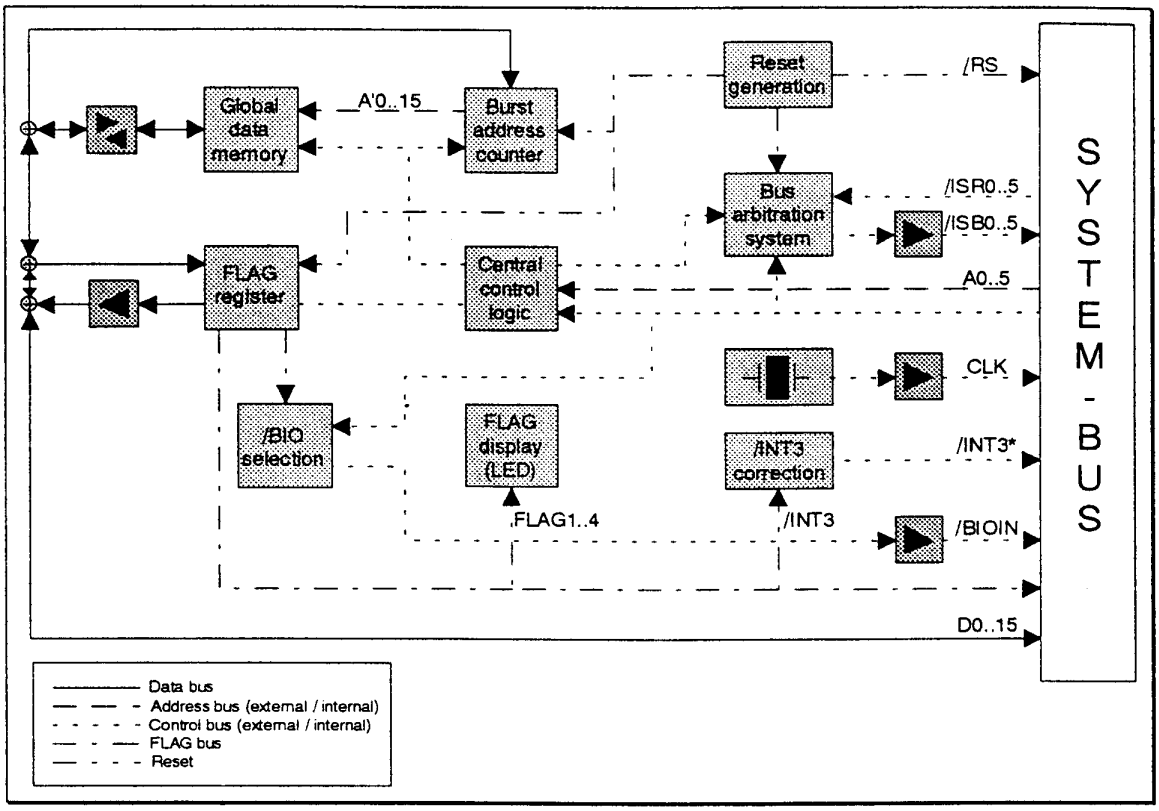


Figure 9. Schematic Overview of the Multiprocessor Interface MPI



As noticed before, there is a 16-bit flag register on the MPI, which stores control bits, interrupts and also 3 bits (MPIO_3) for master to master communication. If one master is going to communicate with another master he will perform an access to the flag register and set the 3 communication interrupt bits. These will be decoded from the other master DSP unit and will trigger the non-maskable interrupt for this CPU. On overview of several functions of MPI is shown in Figure 9.

The MPI also contains additional functions they are needed unique. So it generates the system clock CLK with a buffered crystal oscillator it is used by the DSP units. It also generates a central asynchronous RESET. This RESET signal will be synchronized to the system clock CLK on every DSP unit by using a D-flip-flop, so one can start and reset all units exactly at the same time.

Finally we have identified some key features of this development:

- low cost solution
- modular design for high flexibility
- independent and combined performance of the DSP units

- DSP performance of 28 MIPS
- fast global memory access in burst mode
- optional external program and data memory of 32 kWord available

Scalable Software Architecture

The following are the requirements of the software architecture:

- real-time processing and filtering of all input signals
- measurement for calculation of power, absolute values and phase difference in at least two nodes
- online selection of the complex space phasor of voltage, current or power
- flexible Fast Fourier Transformation for spectrum analysis
- simultaneous analysis of several input signals
- easy-to-use user interface
- modular structured software and expandable for multiprocessor operation

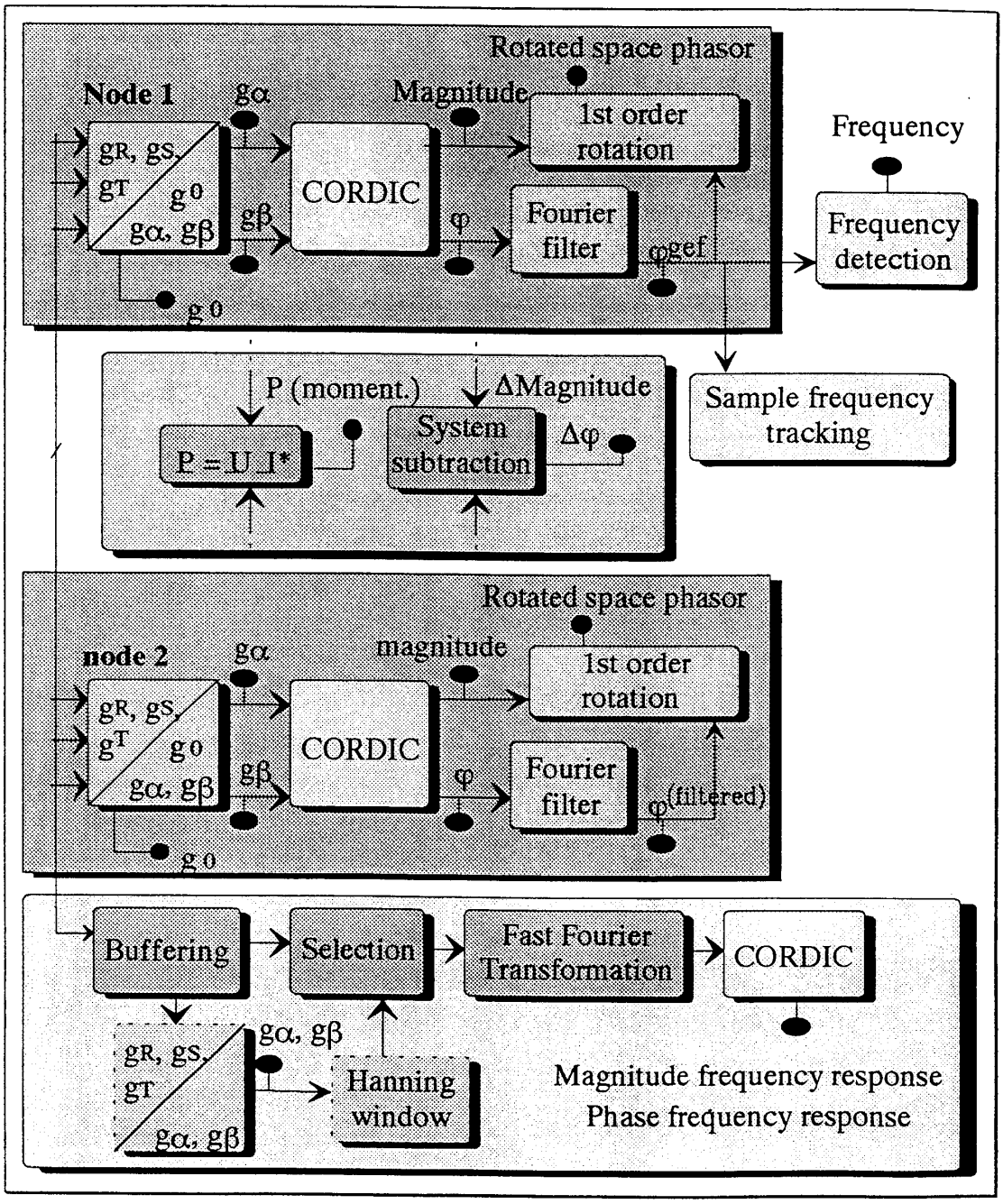
To accomplish these requirements this application uses the TMS320C50 from Texas Instruments. The hardware system allows to measure four power nodes of voltage and current in two network nodes. From this a great variety of network characteristic can be calculated like the space phasor in each node as well in coordinates and in absolute value and phase. By combining the four nodes (current and voltage) the momentary complex power and the difference in absolute value and phase can be detected. The phase of the space phasor is also used to detect the net frequency and to track the sample frequency. One special novelty of this application is the real-time output of the rotated space phasor. The rotation can be set to any given multiple of the net frequency.

Another mode is used to calculate the Fast Fourier Transformation of the input signals or of the complex space phasor. The FFT can be variable, calculated over a flexible number of samples with the maximum at 1024. A Hanning window can be added.

This application is implemented as several modules using structured programming techniques. Algorithms for transcendental functions, filtering, controlling and I/O functions are recorded in libraries.

Trigonometrical function are implemented using fast algorithms with high resolution, e. g. the often called arc-tangent function uses the fast cordic algorithm.

Figure 10. Software Architecture of the NOMS (2 of 4 Nodes)



An oscillograph screen and a display make the measuring results visual. A keyboard supports the flexibility of this system. Program modes and variables can be changed online. Therefore lengthy downloads are not necessary. Controller parameters can be easily optimized and user defined output signals selected.

At this time, the software of the whole system, consisting of 12 AD (reading the test signals in the four nodes), 16 DAs (oscillograph output), a keyboard (user defined online selection) and display (communication with the user and output signals), can be administrated by two TMS320C50 DSP only.

The interrupt system is used to control peripheral elements in a background process. The timer interrupt starts the input and output from and to the AD and DA converters in equal time distances. This interrupt has the highest priority to avoid jittering of the sampled signals. Also, the display output uses this interrupt. Therefore an external buffering of display data is not necessary. Keyboard changes release an interrupt and are processed by a mixture of polling and interrupt processing.

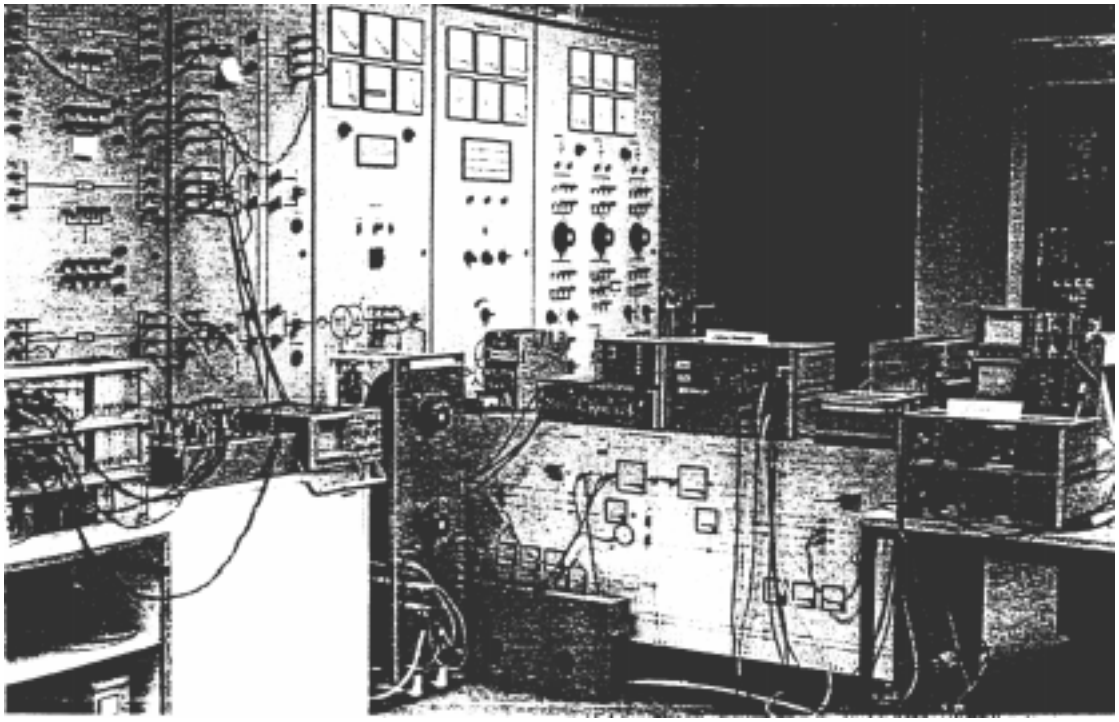
The high level of flexibility of this system is based on a user interface that allows communication with the user and user-defined changes while processing. This possibility simplifies and accelerates the development and is also proved as good for a complex and variable real-time analyses of the supply network characteristics.

Test Environment and Results

Transient Network Analyzer Test Installation

Figure 11 shows the test installation of our transient network analyzer at the University of Erlangen. There we have tested the NOMS under nearly real conditions. We have built up a 220 kV test network which consists of two overlayed networks N_I and N_{II} (see Figure 12) connecting a meshed subsystem with a modem UPFC (FACTS) device and a synchronous generator. We have got the ability to analyze different nodes of the complete network in steady-state operation and to investigate the transient behavior, especially with FACTS device, under normal and fault conditions.

Figure 11. TNS Test Installation



Test Results

Figure 12 depicts the schematic diagram of the entire test installation. Node M is fed by the network N_I using a transformer. The measurement encloses the 3 phase voltages and line current signals in node M and A_3 where a generator stands for a complete power plant.

During two different fault conditions (3 phase short circuits with 100 ms or 1 s duration) the NOMS is monitoring the node and line signals at A_3 and M. Using multi-channel oscilloscopes (time and/or X/Y scaled) the processed momentary signals can be investigated. Further analysis is possible using transient recorders to store the measured and processed data.

Figure 12. Schematic Diagram of TNA Test Installation

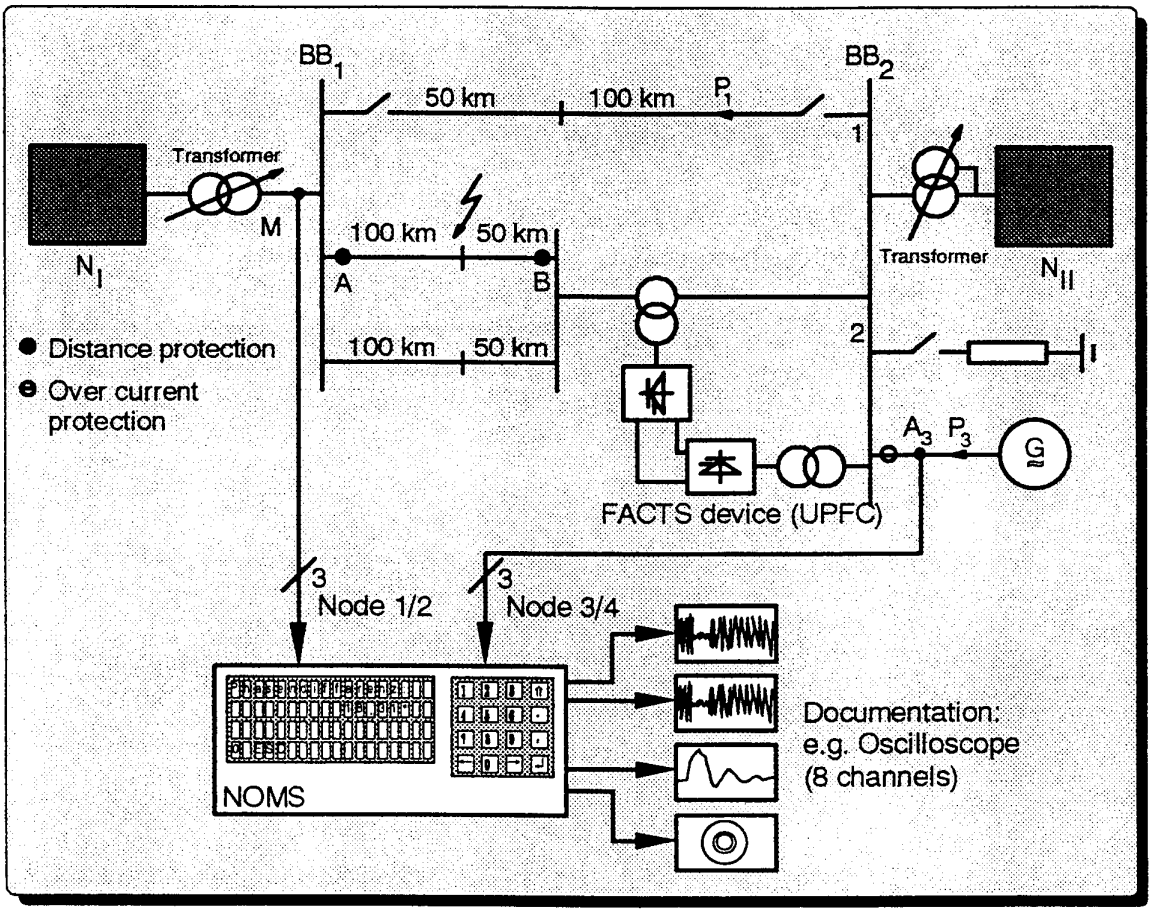


Figure 13 and Figure 14 show the orthogonal components of the voltage V_α and V_β in node M, the corresponding complex space phasor and the momentary phase difference of the voltage in node M and A_3.

After 0.3 s the fault occurs and the voltage drops. At 0.6 s the distance protection relays in B trips and opens the 50 km line. After another 50 ms the distance protection relays in A trips and separates the line A-B completely from the surrounding network. Now the network and supply conditions are faultless again.

Figure 13. Test Results of a 3-Phase Short Circuit (100 ms)

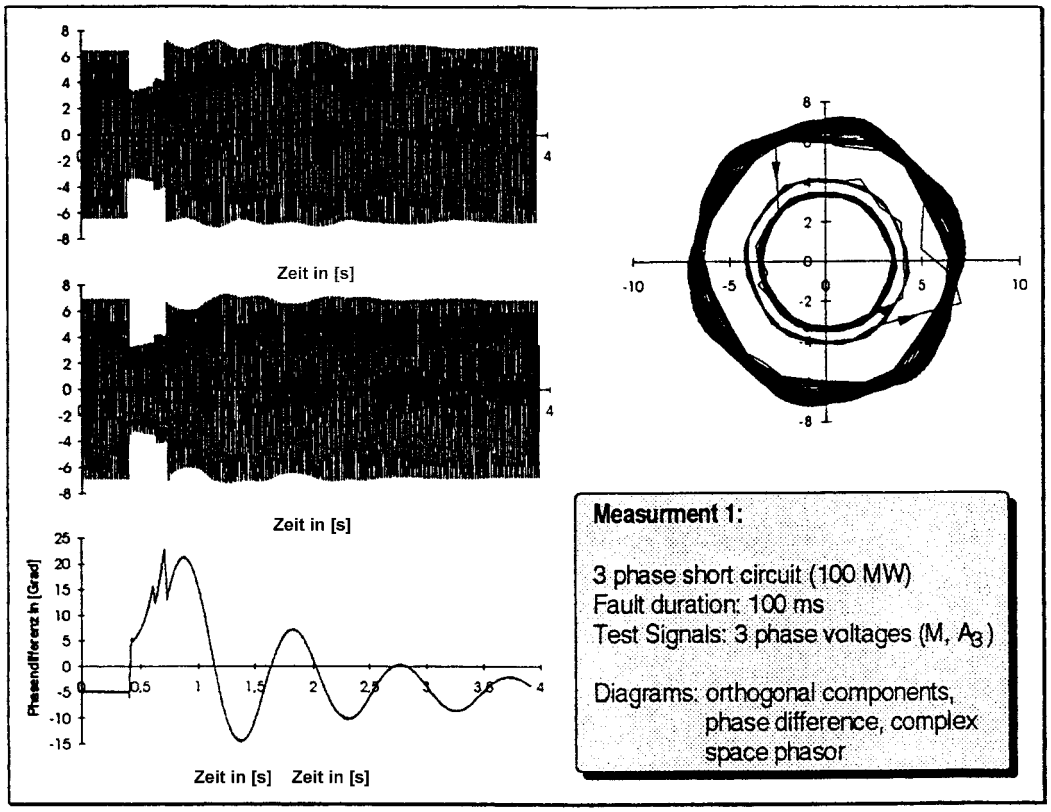
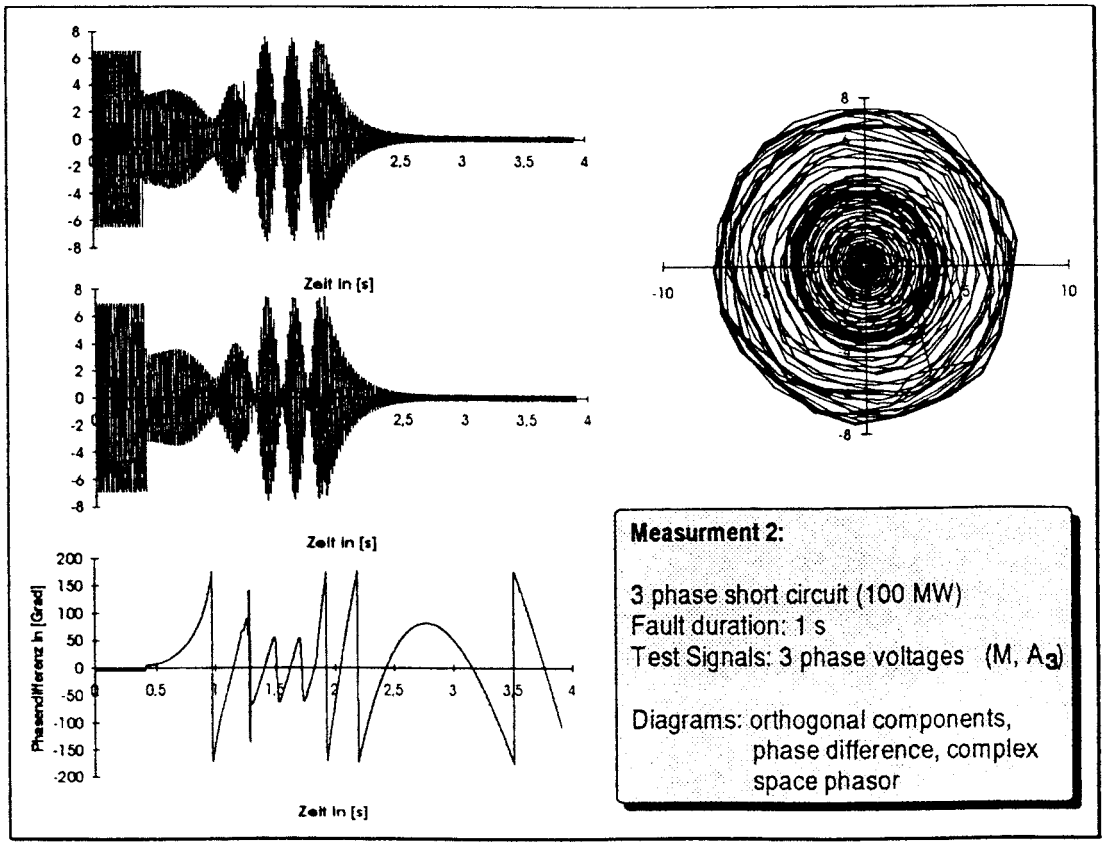


Figure 14. Test Results of a 3-Phase Short Circuit (1 s)



After increasing the fault duration to 1 s, the generator falls out of synchronism because it is slowed down by the high short circuit currents. The generators protection system opens the connecting line at 1.6 s. So the generator is accelerated again reaching, at 2.8 s, the synchronous net frequency.

The phase difference values are calculated by a highly efficient CORDIC algorithm. Therefore the phase information is correct at every moment and also during low distance error conditions.

This example clearly demonstrates some of the facilities and analyzing properties of the NOMS. Network states, fault condition, FACTS operation and stability analysis can be investigated on a much higher level than with previously available tools.

Summary

Analyzing power supply networks is an interesting task for the future and necessary wherever different networks are interlinked. The development of digital signalprocessing systems make it possible to measure different characteristic network parameters allowing a fast detection of network disturbances which can cause damage to electronic facilities. It can also be used to analyze and to control FACTS devices. The FACTS usage will increase in the near future in the modern power supply systems.

Above we have presented an complete solution for a multi-signalprocessing system that is optimized for the application in electrical power supply systems. The digital signal processor TMS320C50 of Texas Instruments is an excellent match for this application because of its hardware and software architecture.

The new key features of our solution can be stated as follows:

- floating voltage measurement with a simple differential OP amplifier circuit (page 13)
- suitable sample rate control unit for power supply systems (page 13)
- low address and data bus loading (BICMOS technology, highly integrated D/A circuits, etc.) (page 13)
- decoupling of asynchronous inputs and outputs from the high-speed DSP units (page 14)
- consistent on-line parameter input system without an interruption of the on-line data processing (page 15)
- each DSP unit represents a independent bus master in a common bus system (page 16)
- multiprocessor interface (MPI) for high-speed communication on a single bus system (page 16)
- optimized use of the on-chip memory of the TMS320C50 (page 17)
- no need of internal address-data multiplexing (page 17)
- integration of a parallel addressed, transparent and high speed cache memory program space after the boot procedure with EEPROM (page 17)
- communication with other bus master units is provided by a global memory space (burst mode access), global registers and a bus allocation system for data consistency (page 19)

- fast bus arbitration via the MPI unit using the independent request method (only two wires for each bus master required) (page 19)
- real-time FFT calculation and output of the complex rotating space phasors (page 21)
- all software is modular and stored in libraries (page 21)
- trigonometrical functions are implemented by optimized CORDIC and/or linear interpolating table based algorithms (page 22)
- on-line user interface enables a flexible control over the software flow (page 23)
- all external interrupts are managed by background processes (page 23)
- the software architecture realizes suitable access timings to slower peripheral components (e.g. display controllers) no buffering or wait-states are required (page 23)
- highgrade of flexibility for on-line analysis and further developments (page 23)

In the near future there will be a big demand for such systems in power supply utilities. Therefore we will continue our successful development with the Texasx Instruments digital signalprocessor components.