TMS320 DSP
DESIGNER'S NOTEBOOK

Initializing the TLC32046 AIC on the TMS320C5x EVM Board

APPLICATION BRIEF: SPRA274

Agnès Delaurière and Olivier Grislain
Digital Signal Processing Products
Semiconductor Group

Texas Instruments
July 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

TRADEMARKS

CONTACT INFORMATION

US TMS320 HOTLINE	(281) 274-2320
US TMS320 FAX	(281) 274-2324
US TMS320 BBS	(281) 274-2323
US TMS320 email	dsph@ti.com

Contents

Figures

Initializing the TLC32046 AIC on the TMS320C5x EVM Board

Abstract

This document discusses the proper way to initialize the registers of the AIC given certain specifications. Details of the setup criteria, equations defining the acceptable options, and calculated data are presented to illustrate the solution.

Design Problem

What is the proper way to initialize the registers of the AIC given certain specifications?

Solution

The main problem encountered involves setting the correct parameters allowing the DSP to run at a fixed rate.

Introduction

The purpose of this Designer's Notebook page is to provide an easy and efficient way to:

- Study the effects of anti-aliasing according to the sample frequency and the low bandpass cutoff frequency.
- Adapt a given prototype defined by its bandpass to the hardware specifications of a development tool based on a TMS320 DSP ('C50 EVM board).

The programs enclosed in the appendices consist in sampling an analog input signal issued from a function generator and sending it back to the analog output of the AIC, for visualization on an oscilloscope.

Overview

The initialization of the system can be divided into three distinct parts:

- Initialization of the DSP (software wait states, sign extension mode, global interrupt register, etc.)
- Initialization of the timer and serial port (e.g., Master Clock frequency, receive and transmit registers, etc.)
- Initialization of the AIC (sampling frequency, low passband cutoff frequency, and other parameters, etc.)

The initialization of the TMS320C5x DSP status and control registers (for wait-states generation, interrupt flags settings, etc.) as well as the initialization of the timer and serial port are explained in details in the TMS320C5x User's Guide (SPRU056), specifically chapters 3 and 5.

The initialization of the AIC is based on three parameters:

- The AIC control register (to set up gain, synchronization, loopback, etc.)

- The Tx counter A register (and Rx counter A if synchronous mode is disabled).
- The Tx counter B register (and Rx counter B if synchronous mode is disabled).

The above parameters, in turn, are based on the two following frequencies specified by the system:

- the sampling frequency, f_s
- the low passband cutoff frequency, f_c

In this example, Tx counter A and Tx counter B (also named TA and TB) AIC registers are used in synchronous mode to determine the D/A (and therefore A/D) conversion timing. Both conversion timings are driven by the MSTR CLK supplied by an external quartz oscillator on the EVM board.

The low bandpass cutoff frequency is determined by the approximate formula below:

$$f_c = \frac{f_{MCLK}(kHZ)}{288kHz} \times \frac{1}{2 \times TA} \times 7.6kHz$$

The high bandpass cutoff frequency is determined by the approximate formula below:

$$f_{cHP} = \frac{f_{MCLK}(kHZ)}{288kHz} \times \frac{1}{2 \times TA} \times 300Hz$$

Method to Determine TA and TB Values According to the f_s and f_c Inputs

The user can read the TLC32046 analog interface circuit data sheet (literature number SLAS028) for further information concerning the protocol of transmission between the DSP and the AIC.

The TLC32046 AIC integrates a low-pass, switched-capacitor, output-reconstruction filter. As explained in the TLC32046 analog interface circuit data sheet, in order for the switched-capacitor lowpass filter to meet its transfer function specifications, the frequency of the clock inputs of the switched-capacitor filters must be 288 kHz. If the frequencies of the clock inputs are not 288 kHz, the filter transfer function frequencies are scaled by the ratio of the clock frequencies to 288 kHz, as it appears in the two formulas above.

The sampling frequency is given by the following formula:

$$f_s = \frac{f_{MCLK}}{2 \times TA \times TB}$$

Once f_{MCLK} is fixed, f_s depends on the TA $\times$ TB product and f_c depends only on TA with the following constraints:

1. TA is an integer in the range 4 to 31 (5 unsigned bits).

2. TB is an integer in the range 2 to 63 (6 unsigned bits).

3. f_C as near as possible, but less than f_s / 2, to satisfy the Shannon criteria.

The procedure to determine TA and TB parameters is the following:

Step 1: Calculate TA $\times$ TB related to the desired sampling frequency (note that if the sampling frequency is not a constraint for your application, then it has to be chosen at least 2f_c according to the Shannon criteria and so that TA $\times$ TB is an integer).

Step 2: Considering that TA $\times$ TB is an integer, within the list of all possible integer values of TA and TB, only some of them satisfy the two first conditions.

Step 3: You must then choose between these results with the one that satisfies the third condition, on calculating f_c.

Example

The quartz oscillator which handles the conversion rate of the AIC on the EVM board provides a master clock frequency of f_{MCLK} = 10.368 MHz. For an application requiring a sampling frequency f_s of 9.6 kHz and in order to satisfy the Shannon criteria, the bandwidth must be limited to 4.8 kHz. Hence, it is recommended to filter the input signal by a lowpass filter with a cutoff frequency

$$f_c = \frac{f_s}{2} = 4.8kHz$$

According to the explanations above, the results are:

$$f_c = \frac{f_{MCLK}}{2 \times TA} \times \frac{7.6}{288} = \frac{136.8kHz}{TA}$$

$$TA \times TB = \frac{f_{MCLK}}{2 \times f_s} = 540 = 2^2 \times 3^3 \times 5$$

And the constraints are: $31 \geq TA \geq 4$
$63 \geq TB \geq 2$

The easiest way to study the different possibilities to obtain the desired sampling frequency and the appropriate cutoff frequency is to fill up a table as shown in Figure 1. The fixed parameter is f_s = 9.6 kHz, which involves a product $TA \times TB = 2^2 \times 3^3 \times 5$. First, fill the first column by giving to TB all the possible combinations of the prime factors.

Figure 1. Possible values of TA and TB according to desired f_c and f_s

TB	TA	TA x TB	f_C (kHz)
2	270 > **31**		
4	135 > **31**		
3	180 > **31**		
6	90 > **31**		
12	45 > **31**		
9	60 > **31**		
18	**30**	**540**	**4.56**
36	**15**	**540**	**9.12**
27	**20**	**540**	**6.84**
54	**10**	**540**	**13.68**
108 > **63**			
5	**108 > 31**		
10	**54 > 31**		
20	**27**	**540**	**5.07**
15	**36 > 31**		
45	**12**	**540**	**11.4**
135 > **63**			
30	**18**	**540**	**7.6**
90 > **63**			
270 > **63**			
60	**9**	**540**	**15.2**
180 > 63			
540 > 63			

Only eight combinations are acceptable:

1) TA=30 and TB=18 giving a cutoff frequency of 4.56 kHz

2) TA=15 and TB=36 giving a cutoff frequency of 9.12 kHz

3) TA=20 and TB=27 giving a cutoff frequency of 6.84 kHz

4) TA=10 and TB=54 giving a cutoff frequency of 13.68 kHz

5) TA=27 and TB=20 giving a cutoff frequency of 5.07 kHz

6) TA=12 and TB=45 giving a cutoff frequency of 11.4 kHz

7) TA=18 and TB=30 giving a cutoff frequency of 7.6 kHz

8) TA=9 and TB=60 giving a cutoff frequency of 15.2 kHz

To select one of these sets of values, you have to consider the desired cutoff frequency of your antialiasing filter and, then, choose the most appropriate. For the 9.6-kHz sampling frequency, the ideal antialiasing filter rejects all frequencies above 4.8 kHz. Hence, you will have to adopt the first combination: TA=30 and TB=18 and to satisfy with a f_c = 4.56 kHz.

According to the Shannon criteria, the optimized operating conditions are obtained when: $f_s / 2 \geq f_c$. Therefore in most of the cases, we recommend to have f_c as near as possible, but less than: $f_s / 2$.

In case of filtering a signal under aliasing conditions, we let the user choose the most appropriate values for TA and TB registers which depend on the nondisturbed passband authorized for the application.

For instance, for a sampling frequency of f_s = 8 kHz, we permit you to choose TA=27 and TB=24, in order to obtain: f_c = 5.07 kHz and a minimum aliasing.

Besides the three steps of establishing the communications between a DSP and the TLC32046 AIC, interrupt service routines must be defined to set up the action to follow after a data word has been received by the AIC or transmitted to it.

The main program calls the different routines corresponding to the initialization process, enables or disables the interrupt registers when needed, then waits for data to be handled by the receive interrupt service routine.

This program called AICEVM50.ASM can be downloaded from the TI BBS and ftp site mirror. It can be compiled and linked by the tools supplied while purchasing the TMS320C50 EVM. The following procedure tells you how to assemble and link this program to have it run on your board.

DSPASM v50 AICEVM50.ASM

DSKLNK AICEVM50.CMD

EVMRST.EXE

EVMLOAD AICEVM50.OUT

Operating Recommendations

Analog Input: Maximum Absolute Input Voltage: 3V
Frequency range: 150 Hz–4560 Hz

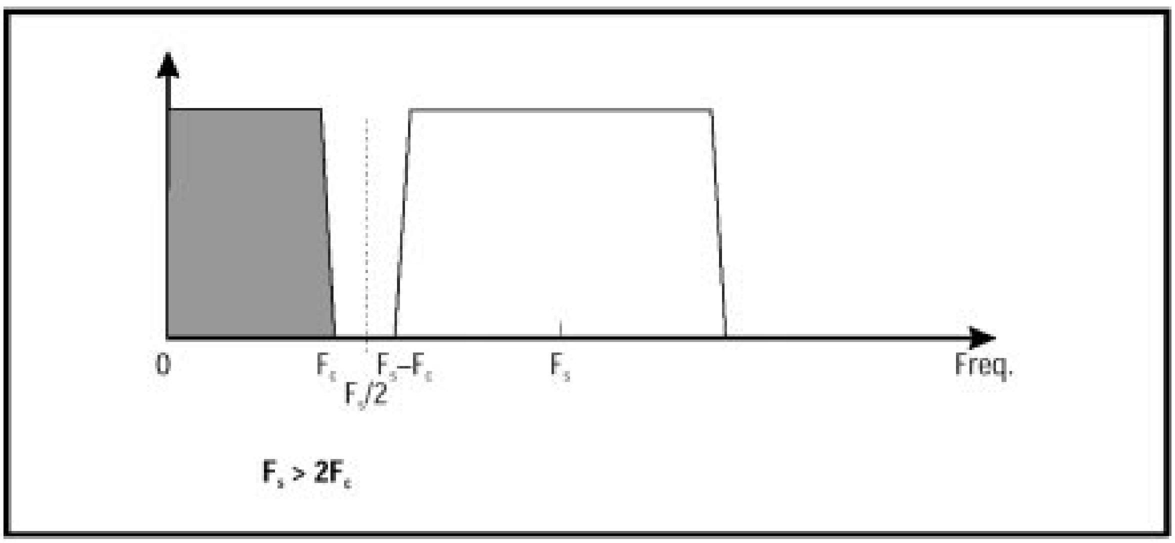
Experimental Results

The tests have been done on an EVM board:

Software				Hardware	
F_s (in kHz)	**TA**	**TB**	**F_c (in kHz)**	**Band Pass (f_c)**	**Aliasing**
8	24	27	5.7	100 – 2200 Hz	Yes
8	27	24	5.07	100 – 2700 Hz	Yes
9.6	30	18	4.56	150 – 4500 Hz	No
16	18	18	7.6	140 – 7600 Hz	No

The last two results obtained correspond to the case where $F_s > 2F_c$ (see Figure 2).

Figure 2. Shannon criteria satisfied



The Shannon criteria are satisfied. The bandpass obtained matches with the values of the cutoff frequencies calculated by the formulas above.

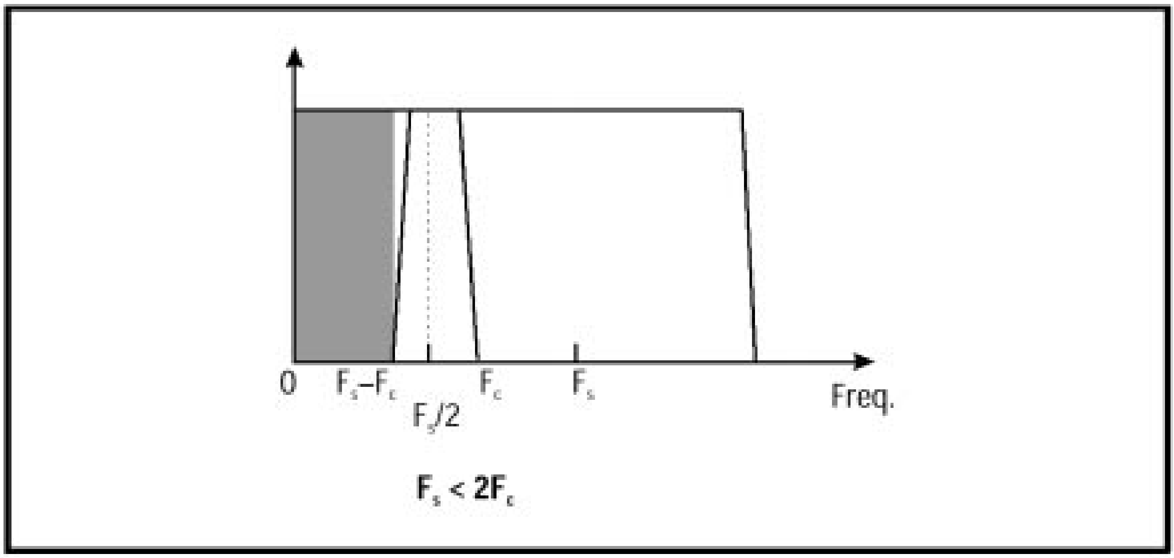
The first two results correspond to the case where $F_s < 2F_c$.

The results obtained for these values of TA and TB confirm the presence of aliasing in the output signal respectively in the range [2.7; 5.7 kHz] and [2.2; 5.07 kHz]. The output signal is not stable on the screen of the oscilloscope, when synchronized by the input signal.

Interpretation

Theoretically, let us consider a lowpass filter instead of a bandpass filter to simplify the reasoning (see Figure 3). Then, all the frequencies between 0 and $F_s/2$ are sampled according to the Shannon rule, but the frequencies in $[F_s/2, F_c]$ are under aliasing. Because of the resulting superposition in the spectrum, the resulting nondisturbed bandwidth is actually $[0, F_s - F_c]$ (as represented in the shaded portion on Figure 3).

Figure 3. Shannon criteria unsatisfied: presence of aliasing



In the last example, $f_c > f_s/2$, the results confirm the presence of aliasing in the output signal. The signal is not stable on the screen of the oscilloscope. All the frequencies between 0 and $f_s/2$ are sampled according to the Shannon rule, but the frequencies in the range of $f_s/2:f_c$ are under aliasing in the spectrum $[f_c\ ;\ f_s - f_c]$:

For the first case, the bandwidth [100–2200 Hz] is not at all modified by aliasing. Theoretically, according to the Shannon criteria, the signal is not altered in the range [100–2300 Hz].

For the second case, the bandwidth [100–2700 Hz] is not at all modified by aliasing. Theoretically, according to the Shannon criteria, the signal is not altered in the range [100–2930 Hz].

This Designer's Notebook page should be used in conjunction with Designer's Notebook page #25, TMS320C2x/'C5x EVM AIC Initialization and Configuration, for more information concerning the way to initialize the AIC.