TMS320 DSP
DESIGNER'S NOTEBOOK

Clocking Options on the TMS320C5x

APPLICATION BRIEF: SPRA245

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TEXAS INSTRUMENTS

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Abstract

There are three speed versions available on most TMS320C5x devices—50 ns, 35 ns, and 25 ns. If you desire to run these devices at full speed, the clock input required is 20 MHz, 57 MHz, and 80 MHz, respectively. In a standard configuration, the input clock is divided by two to get the internal machine cycle: 40 MHz/2 = 20 MHz = 50 ns. The CLKOUT1 pin will run at the same speed as the internal machine rate. This document discusses how a designer can reduce the frequency of the input clock rate.

Design Problem

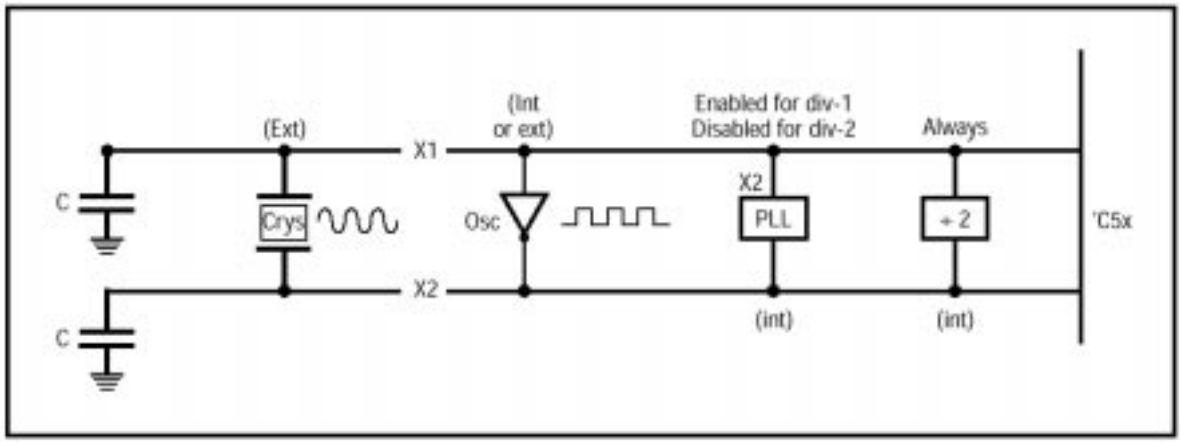
There are three speed versions available on most TMS320C5x devices—50 ns, 35 ns, and 25 ns. If you desire to run these devices at full speed, the clock input required is 20 MHz, 57 MHz, and 80 MHz, respectively. In a standard configuration, the input clock is divided by two to get the internal machine cycle: 40 MHz/2 = 20 MHz = 50 ns. The CLKOUT1 pin will run at the same speed as the internal machine rate. How can I reduce the frequency of the input clock rate?

Solution

The Flow of the Clock (from External to Internal)

Let's look at the flow of clock information from external to internal. This flow will help us understand the options we have in configuring the pins and modes.

Figure 1. Clock Information Flow



The TMS320C5x has five pins (CLKMD1, CLKMD2, X1, X2/CLKIN, and CLKIN2) that can be used to configure the proper mode and hook up the crystal or can oscillator. The state of the CLKMD pins determine the internal clock options such as whether the PLL is enabled or disabled and the type of divide down ratio (div 1, div 2, etc.).

The first item you must decide is whether a crystal or can oscillator (crystal + oscillator) will be used in the system. Then, you must decide whether a divide-by-one or divide-by-two is required. Based on these decisions, the TMS320C5x can be properly configured. The following information will detail the hardware hookups and the state of the CLKMD pins required to properly hook up your system clock.

External Can Oscillator, Divide-by-2

This is probably the most popular option. The PLL will be disabled for this mode because it is only used for the divide-by-1 option. The can oscillator output is connected directly to the X2/CLKIN pin. The only decision left is whether you want the internal oscillator enabled or disabled. But, wait a minute, why would you want the internal oscillator enabled?

This takes power and is not necessary. In most cases, you will want the internal oscillator disabled to reduce power and it's really not necessary. However, if you would like the option of replacing the can oscillator with a crystal, all you have to do is make the replacement. No other changes are necessary. The CLKMD values needed for this mode and operating with just an external crystal are the same.

Figure 2. Hardware Hookup

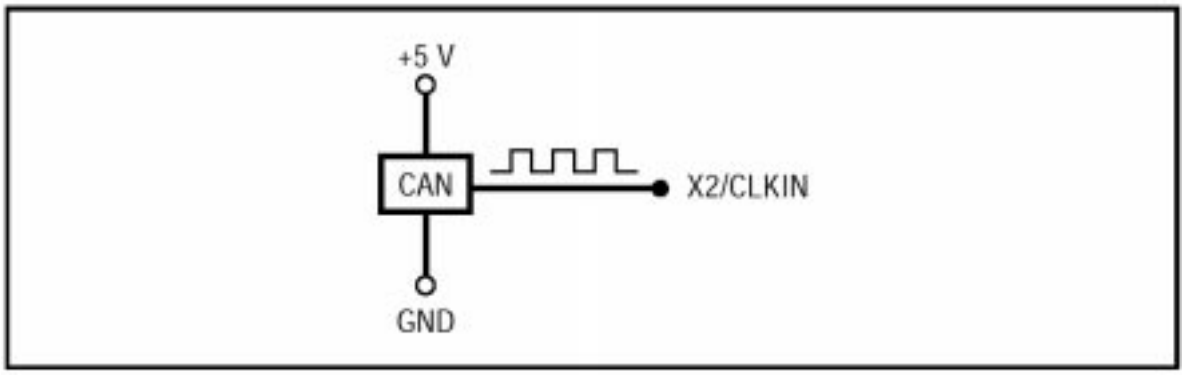


Table 1. Clock Modes

CLKMD1	CLKMD2	Comments
0	0	Internal oscillator disabled, lower power mode for external can oscillator, divide-by-2, PLL disabled.
1	1	Internal oscillator enabled, higher power than above, but allows swap of can oscillator with a crystal with no change in CLKMD1/2 values.

External Can Oscillator, Divide-by-1

This option is preferred when a 40-MHz clock is undesirable because of EMI effects, cost, etc. You can provide a 20-MHz clock on the input, select the divide-by-1 option, and the internal machine rate will be 20 MHz or 50 ns. Internally, the 20-MHz input is actually multiplied by two, then divided by two to create a divide-by-1 result. The PLL must be enabled in this option to accomplish the multiply-by-2 internally. The can oscillator output is hooked directly to CLKIN2 and +5 V is hooked to X2/CLKIN.

Figure 3. Hardware Hookup

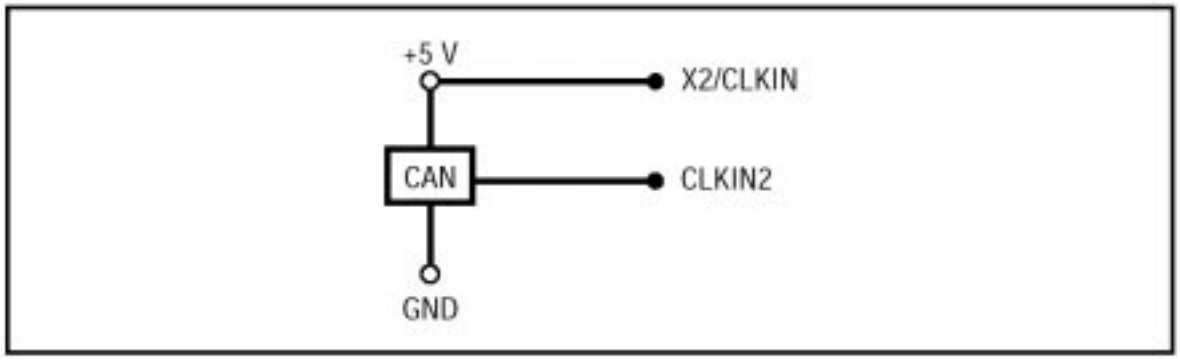


Table 2. Clock Modes

CLKMD1	CLKMD2	Comments
1	0	PLL is enabled (required for X2 of input), internal oscillator is disabled (not needed), lower EMI, X2/CLKIN must be connected to +5 V.

External Crystal, Divide-by-2

This is the only option available for crystal users. The internal oscillator must be enabled to convert the output of the crystal to a square wave. The outputs of the crystal are hooked to the X1 and X2/CLKIN pins.

Figure 4. Hardware Hookup

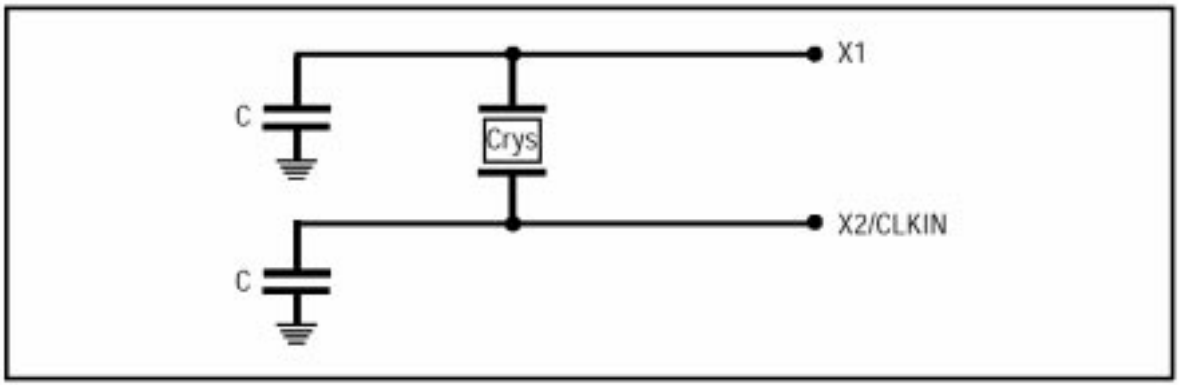


Table 3. Clock Modes

CLKMD1	CLKMD2	Comments
1	1	Internal oscillator is enabled to convert crystal output to a square wave; PLL is disabled (not needed).

Clock Summary

Given below is a summary of all the options.

Table 4. Clock Option Summary

Ext. Crystal	Ext. Can Osc.	Divide-by-?	CLKMD1	CLKMD2	X1	X2CLKIN	CLKIN2	PLL	Int. Osc.
No	Yes	2	0	0	NC	Osc. out	NC	No	No
No	Yes	2	1	1	NC	Osc. out	NC	No	Yes
No	Yes	1	1	0	NC	+5 V	Osc. out	Yes	No
Yes	No	2	1	1	Crystal Output		NC	No	Yes
			0	1	Reserved				