TMS320 DSP
DESIGNER'S NOTEBOOK

TMS320C5x Wait States

APPLICATION BRIEF: SPRA244

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TEXAS INSTRUMENTS

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Abstract

This document discusses the differences between hardware and software wait states. It includes references to the 1993 ’C5x User’s Guide, which describes how wait states are treated on the ’C5x. (Note that many references below are from this manual.) Some additional, useful information helps to tie it all together.

Design Problem

What is the difference between hardware and software wait states?

Solution

The 1993 ’C5x User’s Guide describes how wait states are treated on the ’C5x. (Note that references below are from this manual.) But some additional information is useful to tie it all together.

Two types of wait states are often spoken of:

1) Hardware wait states,

2) Software wait states.

H/W wait states are generated by external logic and connected to the ’C5x READY pin. The ’C5x polls this pin on the falling edge of CLKOUT1 as shown in A-16 and A-17. The setup and hold times shown on these pages should be followed. Table A-13 gives these timings in relation to both RD/WE strobes and CLKOUT1. Following either set is sufficient depending on which set of memory interface signals are used (see Designer’s Note #45). But as the note on the table describes, external ready is only sampled after S/W wait states are completed.

The S/W wait state generator is described in Section 5.3 of the 1993 ’C5x User’s Guide. It is a very flexible on-chip peripheral that eliminates the need for external wait state logic. (Note that any internal access is always 0 wait state).

In general, the ’C5x takes one cycle for a read and two cycles for a write. But in the case of READ-WRITE, WRITE-READ combinations, the write will take three cycles. Also, there is a subtle difference between S/W- (using on-chip S/W wait-state generator) and H/W- (using READY line) based wait states and their bus cycles.

In the case of S/W wait states, “... the addition of a single wait state generated by the on-chip software wait-state generator only affects the read cycle...”. Thus for S/W wait states, the memory R/W cycle for 0 wait state is 1⁄2, for l W/S is 2⁄2, for 2 W/S is 3⁄3, for 3 W/S is 4⁄4. Page 4-25 in the ’C5x User’s Guide talks in detail about this. But since H/W wait states are done by ready line polling, the memory R/W cycle for 0 wait states is 1⁄2, for l W/S is 2⁄3, for 2 W/S is 3⁄4, and for 3 W/S is 4⁄5.

In summary:

Table 1. Wait States

Number of Wait States	H/W Wait State Read	H/W Wait State Write	S/W Wait State Read	S/W Wait State Write
0	1	2	1	2
1	2	3	2	2
2	3	4	3	3
3	4	5	4	4
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