TMS320 DSP
DESIGNER'S NOTEBOOK

TMS320C5x Clock Modes

APPLICATION BRIEF: SPRA243

Joe George
Digital Signal Processing Products
Semiconductor Group

Texas Instruments
May 1994

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

TRADEMARKS

TI is a trademark of Texas Instruments Incorporated.

Other brands and names are the property of their respective owners.

CONTACT INFORMATION

US TMS320 HOTLINE	(281) 274-2320
US TMS320 FAX	(281) 274-2324
US TMS320 BBS	(281) 274-2323
US TMS320 email	dsph@ti.com

Contents

Figures

Tables

TMS320C5x Clock Modes

Abstract

This document explains the TMS320C5x clock modes and how they relate to the internal phase lock loop (PLL).

The clock options and the fully static design of the TMS320C5x provide great flexibility to the designer. This document describes these modes, explains how the designer can take advantage of them and provides references to the primary manuals for more detailed information.

Design Problem

Please explain the TMS320C5x clock modes and how they relate to the internal phase lock loop (PLL).

Solution

The clock options and the fully static design of the TMS320C5x give the user a lot of flexibility. As can be seen in Appendix A-10 of the TMS320C5x User's Guide, two pins CLKMD1 and CLKMD2 select which clock mode in which the part is operating. These modes should not be changed unless the part is in reset (RS =0). A common mode is to run the CPU at a rate that is a divide-by-two of the input clock. The divide-by-two option and the associated CPU speeds for each TMS320C5x device are shown below. Note that the CPU speed is given in nanoseconds. Due to the various ratios between the clock mode input frequency to instruction cycle frequency, it makes the most sense to refer to the instruction cycle time or MIP rate rather than frequency.

Table 1. Divide-by-Two Mode

Part Name	Oscillator	CPU Speed
TMS320C5x	40 MHz (25 nsec)	50 nsec (20 MIPS)
TMS320C5x-57	57 MHz (17.5 nsec)	35 nsec (28.5 MIPS)
TMS320C5x-80	80 MHz (12.5 nsec)	25 nsec (40 MIPS)

Note: Refer to the electrical specifications for specific details.

There are two ways of achieving the divide-by-two clock mode: external crystal or external oscillator. Option 3 (divide by two) on page A-10 in the TMS320C5x User's Guide allows both inputs. If one chooses to use an external crystal, then set CLKMD1=1, CLKMD2=1, and place the crystal across X2/CLKIN1 and X1 pins (see page 2-6 for location and function of these pins). This is the only CLKMD option that allows the use of the crystal in a divide-by-two manner. The internal oscillator generates a clock based on the crystal overtone. Option 3 also has the ability to accept an external square wave from a crystal oscillator. In this particular case, the CLKMD pins remain set to 1 and 1, but the X2/CLKIN1 pin is used as an input and X1 is left unconnected. As a result, the internal oscillator is running needlessly and consuming power. Unless you plan on switching between a crystal and a crystal oscillator (which is pretty remote), it makes more sense to use the CLKMD option 4 with an external crystal oscillator (i.e., CLKMD1=0, CLKMD2=0). In this case, the internal oscillator is shut off and the CPU runs off the input on X2/CLKIN1 divided by two. Note in both cases that the CPU clock may be varied within the specified range all the way down to 0 MHz, if the clock remains clean. In other words, if the clock is shut off (cleanly), the device will retain its state.

As TMS320C5xs get faster, the external oscillators required for operation are very fast. High-frequency oscillators are not only expensive, but may also generate unwanted noise and increase power dissipation. The internal phase locked loop (PLL) helps arrest this problem. When CLKMD1=1 and CLKMD2=0 (PLL enabled), the internal PLL takes the input from the CLKIN2 pin to generate the CPU clock. On all devices except the TMS320C52, the PLL is a x1 multiply. On a TMS320C52, the PLL is a frequency doubler (x2 multiply).

Table 2. PLL Mode (Multiply-by-one):

Part Name	Oscillator	CPU Speed
TMS320C5x	20 MHz (50 nsec)	50 nsec (20 MIPS)
TMS320C5x-57	28.5 MHz (35 nsec)	35 nsec (28.5 MIPS)
TMS320C5x-80	40 MHz (25 nsec)	25 nsec (40 MIPS)

Note: All parts except TMS320C52

Table 3. PLL Mode (Multiply-by-two):

Part Name	Oscillator	CPU Speed
TMS320C5x	10 MHz (100 nsec)	50 nsec (20 MIPS)
TMS320C5x-57	14.25 MHz (70 nsec)	35 nsec (28.5 MIPS)
TMS320C5x-80	20 MHz (50 nsec)	25 nsec (40 MIPS)

One disadvantage of using the PLL mode is, like any PLL, it has a lock range. The lock range is listed on Appendix A-13 of the TMS320C5x User's Guide. As you can see, minimum frequency is not 0 MHz. Thus if clocks need to be shut off, the device must be put into IDLE2 mode.

By examining all three tables, we can see the CPU speeds of a particular device are identical, only the oscillator frequencies changed. In fact, the TMS320C5x's clock generation circuitry should be thought of as an external module to the CPU which sets the instruction cycle time/frequency based on the input clock and modes. The desired instruction cycle time (CPU speed) i.e., MIP requirement, is determined and the appropriate clock mode selected.

Figure 1. Optimal TMS320C5x 25-ns device design

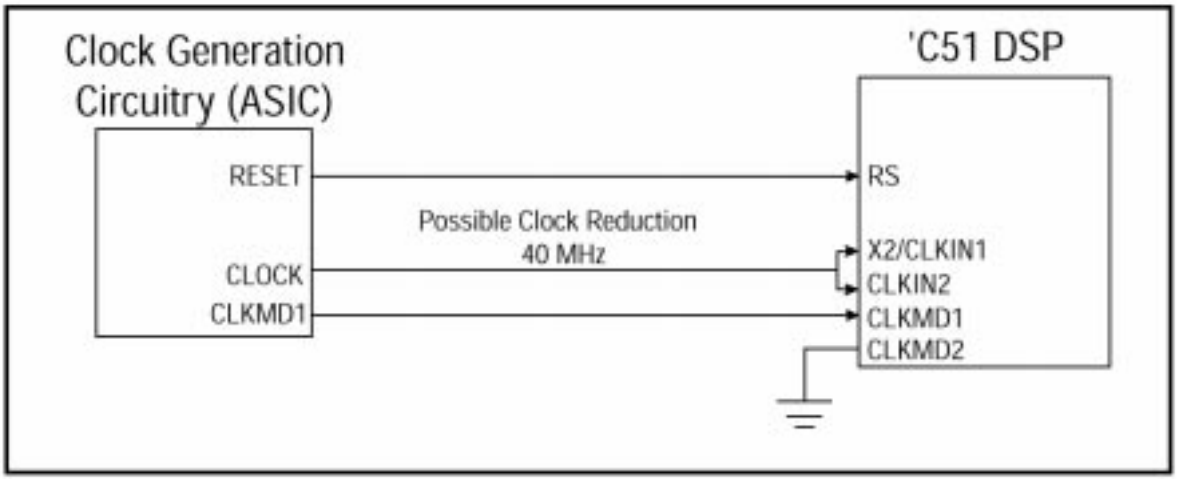

Figure 1 shows a flexible design for a 25-ns device that uses all features of the TMS320C5x clock modes.

Figure 1 shows a 25-ns TMS320C51 device that uses a 40-MHz oscillator. The CLKMD pins may be changed only while RESET is low. If placed in Option 4, then a 50-ns CPU speed is available with optional clock speed reduction supplied by the external logic. In PLL divide-by-one mode, the TMS320C5x operates as a 25-ns device, but must be in IDLE2 mode in order to shut off the clocks. Clock speed reduction must be within the PLL lock range.