TMS320 DSP
DESIGNER'S NOTEBOOK

Supporting External DMA Activity to Internal RAM for TMS320C5x Devices With the PZ Package

APPLICATION BRIEF: SPRA237

Jim Larimer
Digital Signal Processing Products
Semiconductor Group

Texas Instruments
May 1994

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

TRADEMARKS

TI is a trademark of Texas Instruments Incorporated.

Other brands and names are the property of their respective owners.

CONTACT INFORMATION

US TMS320 HOTLINE	(281) 274-2320
US TMS320 FAX	(281) 274-2324
US TMS320 BBS	(281) 274-2323
US TMS320 email	dsph@ti.com

Contents

Supporting External DMA Activity to Internal RAM for TMS320C5x Devices With the PZ Package

Abstract

This document discusses how to use the DMA capability of TMS320C5x devices with the thin-quad-flat package.

The problem is that when moving to the small outline and footprint of the thin-quad-flat package (TQFP) for TMS320C5x devices, some functionality is removed to reduce pin count. This move from the 132-pin quad-flat package (PQ package) to the 100-pin TQFP (PZ package) removes two functional pins: interrupt acknowledge (IACK) and instruction acquisition (IAQ). Aside from its traditional function, the IAQ pin is also used to acknowledge the bus request (BR) signal for external DMA access to the single access RAM.

Design Problem

When moving to the small outline and footprint of the thin-quad-flat package (TQFP) for TMS320C5x devices, some functionality is removed to reduce pin count. This move from the 132-pin quad-flat package (PQ package) to the 100-pin TQFP (PZ package) removes two functional pins: interrupt acknowledge (IACK) and instruction acquisition (IAQ). Aside from its traditional function, the IAQ pin is also used to acknowledge the bus request (BR) signal for external DMA access to the single access RAM.

How do I use the DMA capability with the thin-quad-flat package?

Solution

All ’C5x devices with single-access RAM (’C50, ’C51, and ’C53) offer a unique feature allowing another processor to read and write to its internal memory. The TMS320C51 and TMS320C53 are offered in a 132-pin quad-flat package (PQ pack-age) and a 100-pin TQFP (PZ package) for systems with size constraints. To use the DMA capability with the TQFP package, the following should be considered.

To initiate a read or write operation to the ’C5x single-access RAM, the Host or Master processor requests a hold state on the DSP’s external bus. When acknowledged with HOLDA, the Host can then request access to the internal bus by lowering the bus request line (BR). Unlike the hold mode, which allows the existing operation to complete and allows the CPU operation to continue (if status bit HM = 0), a BR-requested DMA always freezes the operation currently being executed by the CPU. Because of this, the time required to grant the access to the internal single-access RAM is deterministic and does not vary. Access to the internal bus is always granted on the third cycle after the bus request signal is received. Therefore, the IAQ signal is not an essential signal for external DMA activity to the single-access RAM. The host is required to wait two ’C5x cycles after driving the bus request line low. The host can then safely assume that access to the internal bus has been granted and begin the DMA operation.

All other signals and timing conditions required for DMA access are the same as those listed in the TMS320C5x Users Guide.