TMS320 DSP
DESIGNER'S NOTEBOOK

Using VRAMs and DSPs for System Performance

APPLICATION BRIEF: SPRA224

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Abstract

This document discusses how a designer can improve the performance of the DSP-based system Hard Disk Drive (HDD) memory. The case study approach is used to address issues of drive component integration. Problems and solutions are presented.

Design Problem

How can I improve my DSP-based system memory performance?

Solution

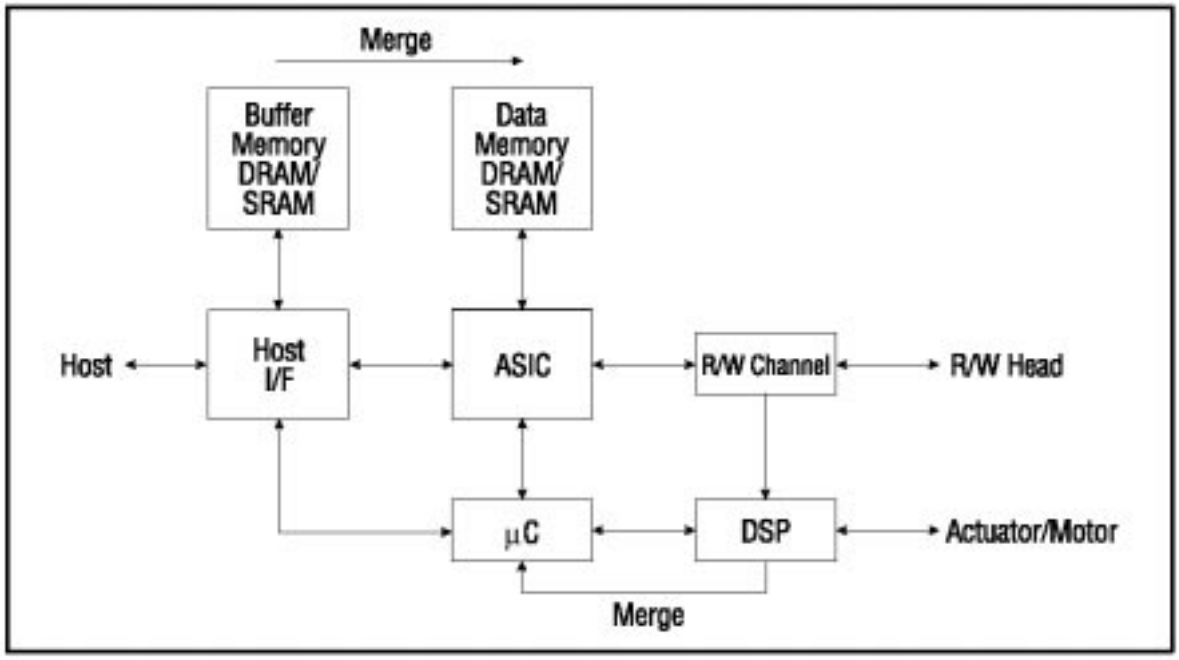
A Case Study

HDD designers talk about integration of drive components. Typically they have focused on integrating the glue logic in an ASIC and go from an analog to a digital servo and then reduce to a single processor drive. Also integration of the host I/F with the µC/DSP has been talked about. One area that has also gone through some integration is the memory on the drive. Ideally HDD designers would like to have one large memory buffer. However, they then run into performance bottlenecks because there is only one path into this memory that must be shared by many sources. Given that the drive performance is also increasing, the problem becomes even more serious. Below the problem is discussed in detail and we present a solution to the problem using the Video RAM technology as a basis.

Problem Description

“Today” a typical HDD block diagram looks like Figure 1.

Figure 1. Typical HDD Block Diagram



The buffer memory holds incoming or outgoing blocks of data to be written or read into the disk platter. The data memory would ideally hold the μC (or DSP) program and data structures. The μC would be masked with a boot program that would download the SCSI/AT code from the disk platter into the data buffer.

Ideally, HDD manufacturers would like to merge the μC and DSP functionality and the buffer and data memories. There are many other possible partitions, but the above are the most popular and would reduce system cost significantly.

A TI DSP makes a good solution for the DSP/μC integration.

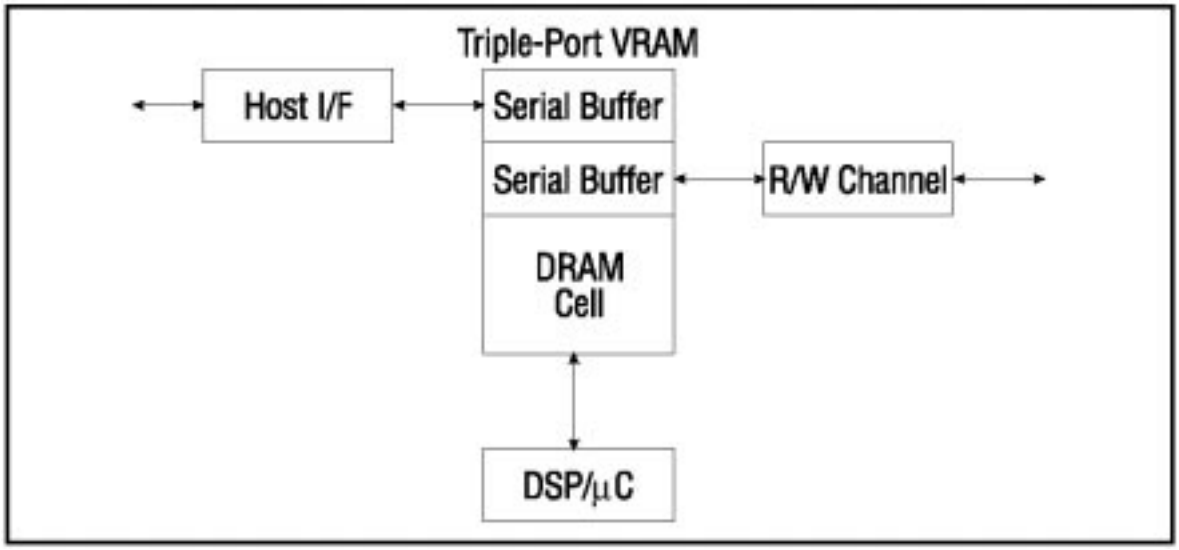
What the HDD designers are running into is performance bottlenecks when you merge the buffer/data memory blocks.

The merged buffer/data memory block would have three sources trying to read and write data via a single port. As data throughput increases, the arbitrator (built into the ASIC) must prioritize access. Eventually this will limit the data throughput and hence the performance of the HDD. HDD manufacturers are currently hitting these limits.

VRAM Solution

A Video RAM is the perfect solution for these data bottlenecks. For instance, a triple-port VRAM (depicted below), would greatly enhance the data throughput.

Figure 2. A Triple-port VRAM



The HOST I/F and the R/W channel can read and write data to the serial buffers at very high speeds without affecting the DSP/μC access to the data in the DRAM cells. When the serial buffer is full, the DSP/μC can transfer a block of data to the DRAM cell in a few cycles. The DSP/μC can therefore execute program from the VRAM without sacrificing performance.