*TMS320 DSP*
*DESIGNER'S NOTEBOOK*

# *Dual Access into Single-Access RAM on a 'C5x Device*

*APPLICATION BRIEF: SPRA215*

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*February 1993*

TEXAS INSTRUMENTS

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## Abstract

Using the TMS320C5x DSP, it is possible to make two accesses to Single-Access RAM (SARAM) in one cycle. This document discusses how this is done, and what limits exist. Also discussed are Dual-Access RAMs.

## Design Problem

How do I make two accesses to Single-Access RAM (SARAM) in one cycle?

## Solution

’C5x SARAM is NOT just one big RAM block where only one access per cycle is allowed. Instead, it is actually made up of 2K-word size independent RAM blocks, each one of which allows one CPU access per cycle. Hence, the CPU can read/write one 2K block while accessing another 2K block at the same time. All ’C5x processors support multiple accesses to SARAM in one cycle as long as they go to different RAM blocks. In the case where total SARAM size is not a multiple of 2, one block is made smaller than 2K words.

If you understand these restrictions, then you can appropriately arrange code and data to improve code performance.

*Table 1. SARAM Blocks vs. Device*

| Device | Number of SARAM blocks |
|---|---|
| ‘C50 | Four 2K blocks and one 1K block |
| ‘C53 | One 2K block and one 1K block |
| ‘C51 | One 1K block |

The details of ’C5x SARAM organization appear in Chapter 4 of the ’C5x User’s Guide (pp. 4-24, 6-2, C-2). Instruction cycle tables in Chapter 4 (pg. 4-24) cover all cases.

**’C5x Dual-Access RAM**

’C5x dual-access RAM is TRULY dual-access in the sense that it will let you access twice per cycle with no restrictions on what locations are accessed.