TMS320 DSP
DESIGNER'S NOTEBOOK

Interfacing the TMS320C31 to A/D and D/A Devices

APPLICATION BRIEF: SPRA210

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TEXAS INSTRUMENTS

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Abstract

The TMS320C3x DSPs are designed to easily interface with 16-bit A/D and D/A devices for audio and data acquisition applications. This document shows how to interface the TMS320C31 with zero glue-logic to Burr-Brown's DSP201/2 and DSP101/2 family of D/A and A/D devices. An example audio application circuit is used to illustrate the interconnections required. A schematic is included.

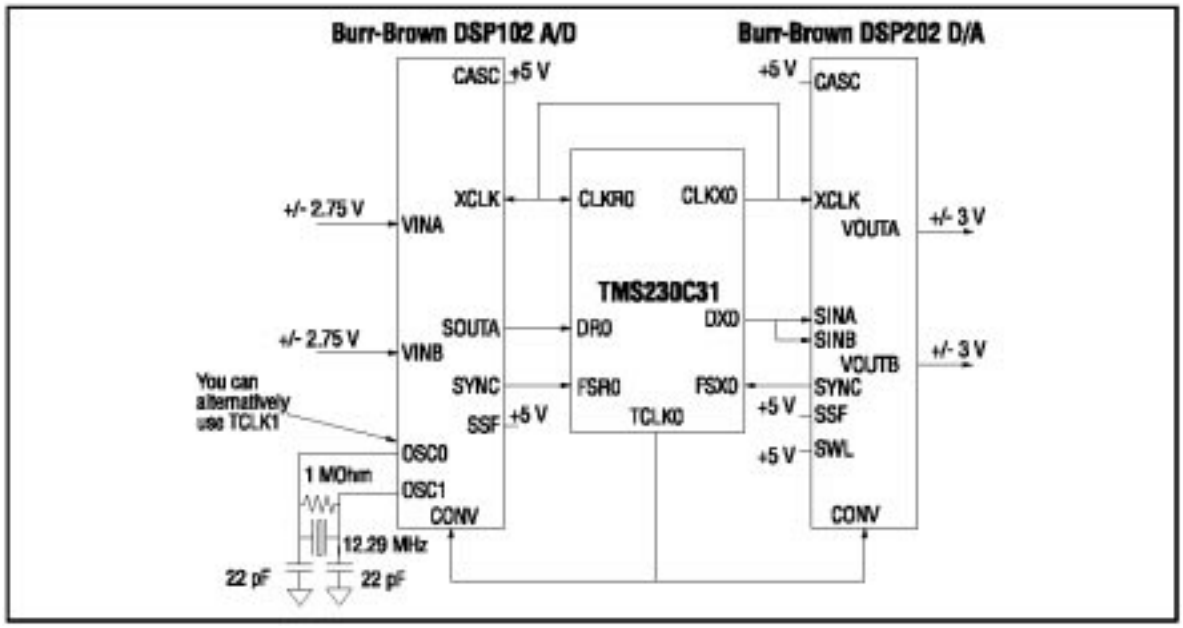
Design Problem

What interface circuitry is required to connect a ’C31 to A/D and D/A?

Solution

The TMS320C3x DSPs are designed to easily interface with 16-bit A/D and D/A devices for audio and data acquisition applications. The following figure shows how to interface the TMS320C31 with zero glue-logic to Burr-Brown’s DSP201/2 and DSP101/2 family of D/A and A/D devices. An efficient, low-cost, stereo, digital audio interface using a ’C31 and the DSP202 and DSP102 dual-channel D/A and A/D chips is shown in Figure 1.

Figure 1. TMS320C31 Zero Glue-logic Interface to Burr-Brown A/D and D/A



The DSP102 A/D is interfaced to the ’C3x serial port receive side; the DSP202 D/A is interfaced to the transmit side. The A/D and D/A are hard-wired to run in cascade mode. In this mode, when the ’C31 initiates a convert command (CONV) to the A/D via its TCLK0 pin, both analog inputs are converted into two 16-bit words which are concatenated to form one 32-bit word. The A/D signals the ’C31 that serial data from the last conversion is being transmitted via the A/D’s SYNC signal. The 32-bit word is then serially transmitted, MSB first, out the SOUTA serial pin of the DSP102 to the DR0 pin of the ’C31 serial port. The ’C31 is programmed to drive the analog interface bit clock from its CLKX0 pin. The bit clock drives both the A/D and D/A XCLK input.

The ’C31 transmit clock can also act as the input clock on the receive side of the ’C31 serial port. Since the receive clock is synchronous to the ’C31’s internal clock, the receive clock can run at full speed (even though it is an external clock).

Similarly, upon receiving a convert command (CONV), the D/A converts the last word received from the ’C31 and signals the ’C31, via the SYNC signal, to begin transmitting a 32-bit word representing the two channels of data to be converted. The data, transmitted from the ’C31 DX0 pin, is input to both the SINA and SINB inputs of the D/A.

The ’C31 is set up to transfer bits at the maximum rate of about 8 Mbytes/sec with a dual-channel sample rate of about 44.1 kHz by setting the following registers (assuming a 32 MHz CLKIN):

Serial Port:

Port global control register 0x0EBC0040

FSX/DX/CLKX port control register 0x00000111

FSR/DR/CLKR port control register 0x00000111

Receive/Transmit timer control register 0x0000000F

Timer:

Timer global control register 0x000002C1

Timer period register 0x000000B5

A synchronous receive interrupt service routine is sufficient for parsing and transferring data between the serial ports and memory. Source code for setting up the serial port and timers of the ’C31 for interfacing to the DSP102 and DSP202 can be found on the TI BBS, file name: C3XBB.EXE.