TMS320 DSP
DESIGNER'S NOTEBOOK

Reducing System Power Requirements

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Reducing System Power Requirements

Abstract

With the ever-growing need for battery-operated systems, the need for low-power designs has increased significantly in recent years. These low-power applications have expanded to include high-speed DSP designs. It is necessary to design with high-speed devices while maintaining an overall power reduction. This document discusses a number of ways to reduce your system power, ranging from the use of CMOS logic to varying the clock rates of the logic to powering down unused logic. Graphs are given, showing the resultant power savings.

Design Problem

What steps can I take to reduce overall power requirements of my system?

Solution

With the ever-growing need for battery-operated systems, the need for low-power designs has increased significantly in recent years. These low-power applications have expanded to include high-speed DSP designs. It is necessary to design with high-speed devices while maintaining an overall power reduction. There are a number of ways to reduce your system power, ranging from the use of CMOS logic to varying the clock rates of the logic to powering down unused logic.

Semiconductor processing in CMOS results in devices inherently lower in power dissipation than their BIPOLAR or NMOS counterparts. This is primarily due to the fact that once a CMOS gate has stabilized at a level, it requires little or no power to stay in that state. The equivalent NMOS or BIPOLAR gate requires power to maintain that level.

The TMS320 devices use fast buffers to improve the access time of external resources. These fast drivers can be a significant part of the total power used by the device if the care is not taken in the design. First, the on-chip ROM/EPROM and RAM of the TMS320 devices is inside the large drivers so it takes significantly less power when accessing these memories than when accessing external memories. In many applications there are segments of the code that are accessed significantly more often than the rest of the code. These segments can be masked into the ROM, programmed into the EPROM, or boot loaded into the RAM.

Second, minimizing the fanout drive of the output buffers will help minimize the power requirements. Collapsing the glue logic into PALs or ASICs will reduce the number of inputs these fast buffers must drive.

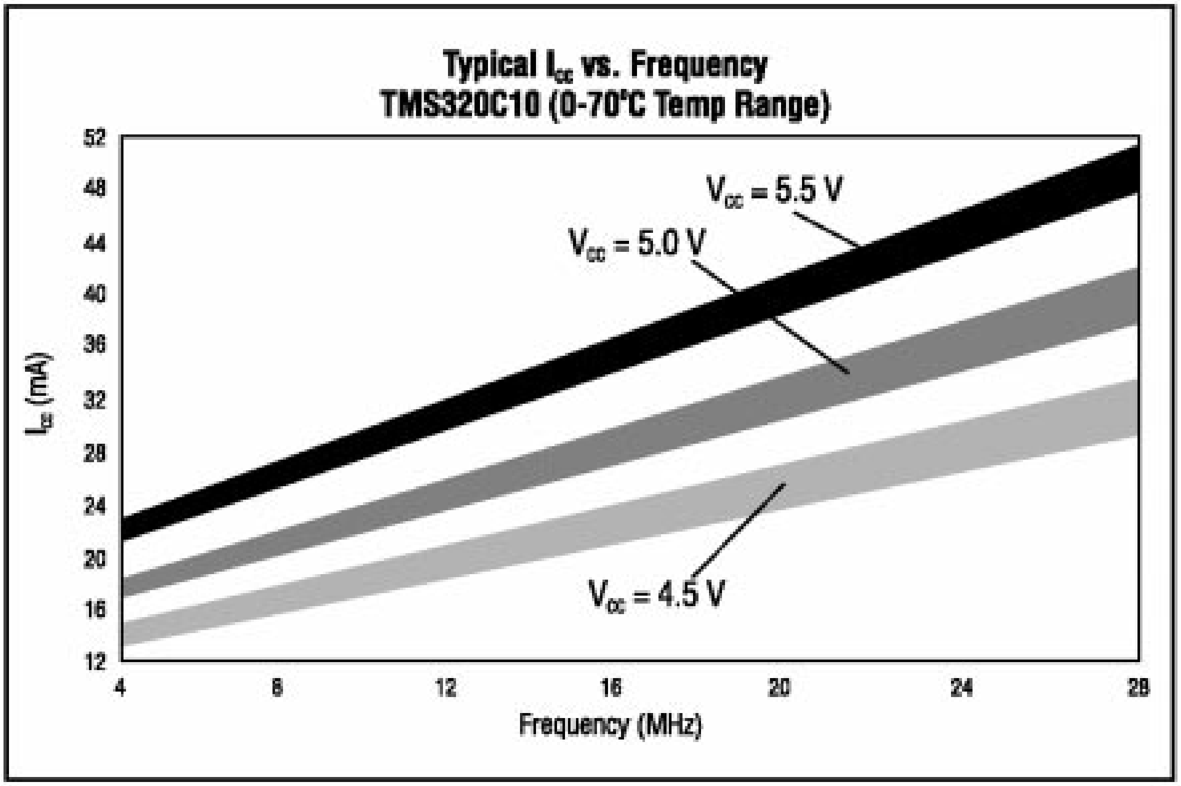
Third, power consumption is minimized when all unused input-only pins are connected to high voltage or ground. This ensures that the inputs to the CMOS gates of the device are not floating (not switching).

Power consumption varies with voltage level. If the V_{CC} is held between 4.75 V and 5.0 V the DSP device will consume less power than if it is run above 5.0 V. The TMS320 family also includes low-voltage devices like the TMS320LP1x family of 3.3 V devices. The TMS320C5x generation of devices also supports low-voltage operation. If the temperature environment of the system can be regulated to within a moderate range, the power consumption of the TMS320 devices can be reduced. In the case of hand held instruments, the fact that they are held in a hand indicates the temperature is likely well inside the operating range of the device, as 0°C and 70°C are both rather uncomfortable environments for your hands.

Some of the TMS320 devices have power-down modes. These modes include IDLE instructions, HOLD modes, and device power-down switches. The IDLE instructions shut down part or all of the CPU operations of the device, thus reducing the amount of logic that is switching. The TMS320C5x devices also include a second IDLE instruction that shuts down virtually all the logic on the device, thus reducing the required current to around 1 mA. The HOLD signal can also stop the internal CPU of the TMS320C2x and TMS320C5x devices if the HM status bit is set to one. The HOLD also puts all the memory interface signals in a high-impedance state.

The power required by the TMS320 device is directly proportional to the frequency at which is it operating (see Figure 1 and Figure 2). Therefore, if there are times when the system does not require the full computational capability of the DSP, then the input clock can be slowed to reduce the system power. A simple divide down of the input clock can significantly reduce the power. The TMS320C5x devices are implemented in static logic so the input clock can be stopped, reducing the required current to µAs. Some of the devices (such as the TMS320C28) include power-down transistors. These transistors remove power from the CPU while maintaining power to the on-chip RAM. This allows the system to save key registers in the RAM and power down the CPU while the system does not require the DSP. Then quickly restore the registers from the RAM once the system needs the DSP again.

Figure 1. Current vs. Frequency Graph for the TMS320C10



In summary, the guidelines below can be followed to reduce the active power:

- Use CMOS devices.
- Use on-chip memory.
- Minimize fanout via integration (ASIC or PAL).
- Lower voltage.
- Control temperature.

The guidelines below can be followed to reduce power when the system is inactive:

- IDLE the CPU.
- Slow down or stop the input clock.
- Switch off the power to dormant circuitry of system.

Figure 2. TMS320C5x Power Dissipation Characteristics