

*TMS320 DSP
DESIGNER'S NOTEBOOK*

TMS320C30 Addressing up to 68 Gigawords

APPLICATION BRIEF: SPRA201

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TMS320C30 Addressing up to 68 Gigawords

Abstract

The primary bus of the TMS320C30 has 24 address lines, which allows addressing of up to 16 megawords of memory. The expansion bus has 13 address lines, which allows addressing 8 Kwords. Using the techniques shown in this document, they can be used together to address a larger memory space of up to 68 gigawords.



Design Problem

The primary bus has 24 address lines, which allows addressing up to 16 megawords of memory. The expansion bus has 13 address lines addressing 8 Kwords. How can they be used together to address a larger memory space?

Solution

Figure 1, below, illustrates one solution to this problem. This technique uses the expansion bus address lines [XA(12-0)] simultaneously with the primary address lines [A(23-0)], to extend the address to 36 bits. The feature that is used is a power-saving feature of the 'C3x family that holds the past address bits on an external bus until a new external access occurs (i.e., the A-Bus works as a latch). The following parallel instruction accomplishes this task:

```
STI Rx,*ARn    ; address MSTRB while loading a
                ; value from STRB memory
|| LDI *ARp,Rq  ;
```

where:

Rx and Rq designate registers R0 to R7 (but not the same register) and ARn and ARp designate auxiliary registers AR0 to AR7 (but not the same register).

Note: ARn contains the 8 megaword segment address plus 800000h. ARp contains the address within the 8-megaword segment and is between 0 and 7FFFFh.

Figure 1. Solution Diagram

