

A TMS320C53-Based Enhanced Forward Error-Correction Scheme for U.S. Digital Cellular Radio

Application Report

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Abstract

This report presents an enhanced forward error-correction scheme that complies with the U.S. Digital Cellular (USDC) standard. The proposed scheme uses a generalized Viterbi algorithm (GVA) based on N. Seshadri and C-E. W. Sundberg's, "Generalized Viterbi Algorithm for Error Detection with Convolutional Codes" [1] that produces an ordered list of N globally best estimates of the transmitted sequence. The scheme uses the GVA to enhance performance of the USDC voice channel decoder and is implemented on the TMS320C53 fixed-point digital signal processor (DSP). This paper shows that the 'C53 implementation of the algorithm does not require significant increase in computational overhead when compared to a standard Viterbi algorithm.

Introduction

The second-generation U.S. cellular radio telephone system (IS-54 standard) is based on digital technology. To increase system capacity and improve speech quality, the voice channels use digital transmission for both forward and reverse radio links. Each radio channel is shared by at least three mobile units through a time-division multiple access (TDMA) scheme. Elaborate forward error-correction (FEC) techniques are employed to operate these radio links reliably under low carrier-to-interference (C/I) ratio and high data-transfer rate. The IS-54 standard combats channel noise by using systematic cyclic redundancy check (CRC) codes, convolutional encoding, and frame interleaving techniques on transmitted data. Although the standard does not recommend any particular decoding algorithm, the Viterbi algorithm (VA) is most commonly used by system designers.

Various generalizations of the original Viterbi algorithm have been presented in the literature [1, 2, 5, 6]. These schemes provide enhanced performance over the conventional Viterbi algorithms for a number of applications, including automatic repeat request (ARQ) schemes, concatenated codes, coded Viterbi equalization, etc. One scheme [2] modifies the VA to deliver a reliability value for each bit in the most likely path sequence. This algorithm is useful for Viterbi equalization on IS-54 radio channels, leading to an improved performance of the outer VA performing the FEC. Another scheme [1] generalizes the VA to find N globally best estimates of the transmitted sequence. It is shown here that this algorithm is particularly appropriate for the rate-1/2 framed convolutional encoder used by the IS-54 voice channel. This GVA is implemented on the TMS320C53 fixed-point DSP.

Algorithm Description

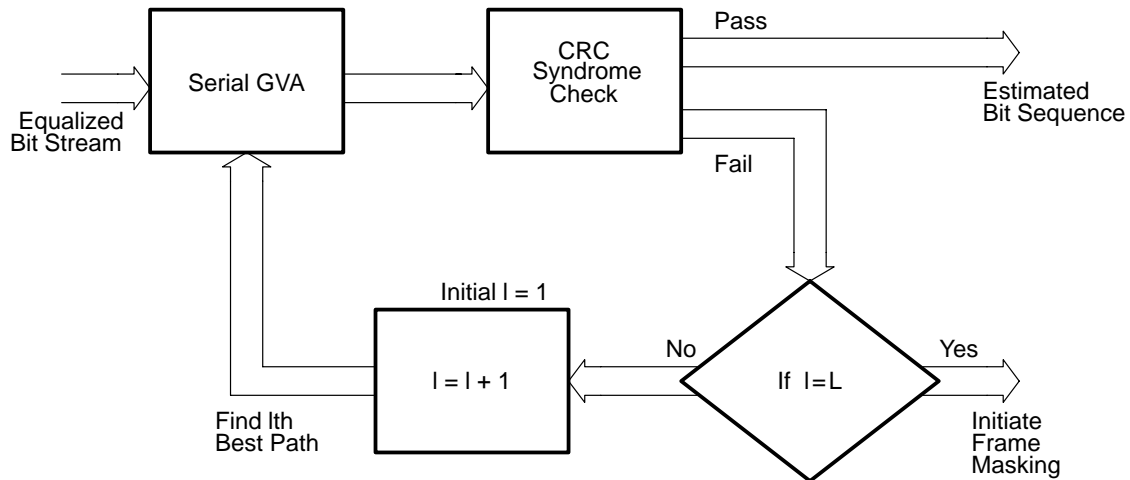
It is well known that bit errors usually occur in bursts in Viterbi decoders. If you know the globally second best path, the third, etc., you can use this information to reduce the burst error rate under noisy conditions. To select N best paths simultaneously, N best survivors (out of $2N$ for a rate-1/m code) at each state must be retained during the forward pass through the trellis. This is referred to as *parallel GVA* in [1]. However, for this application, only one path is estimated at a time. If requested, the *serial GVA* [1] produces the nth best path on the basis of the previous $n-1$ best paths.

The serial GVA algorithm, as shown in Figure 1, is selected for the voice channel FEC because it results in reduced memory requirement and less computational overhead, as discussed in the next section.

The IS-54 voice channel uses a concatenated coding scheme in which each message frame is divided into two bit classes: class I and II. For the twelve perceptually most important bits of class I, a 19-bit systematic CRC code is generated. These bits, along with the rest of the class I bits, form input to a rate-1/2 framed convolutional encoder with a constraint length of 5. The class II bits remain uncoded.

The frame size of the encoder is 89 bits, including five tail bits. The encoder always starts and ends in state 0. The serial GVA decoder maintains a state path history as it expands the trellis in the forward pass. It also sets up two accumulated metric tables, accum1 and accum2, for the two globally best paths. Since the trellis expands from initial state 0, the first element of the accum1 table is initialized to 0, and the rest of the table is set to a large positive number for a distance-type metric (or a large negative number for a correlation-type metric). Similarly, the second table, accum2, is also initialized to a large positive number, except for the first element, which, in this case, is initialized with a positive integer N.

Figure 1. IS-54 Voice-Channel GVA Algorithm



The first pass of the algorithm produces the globally best estimate of the transmitted sequence. The algorithm, in this case, is identical to a conventional VA, with one exception: it updates the state count array as it traces the best path back in time. This state count array is used for any subsequent invocations of the GVA. Each element h_{ij} of the state count array uniquely represents state i in time interval j and indicates how many of the previously identified $n-1$ best paths pass through state i in time j . When the GVA is invoked for the first time, the state count array is initialized to 0. During trace-back of the best path, corresponding elements of the array are incremented by 1.

To find the second best path, the trellis is expanded again; however, this time, the second best path (out of four possible survivors) that enters state i in time j whose $h_{ij} \neq 0$ is retained. For the states whose corresponding h_{ij} s are 0 (that is, states that are not included in the globally best path), the best survivor is retained. Note that, in this case, no processing is required because the state path table already contains the history of the best path. During the trace-back phase for the second best path, elements of the state count array that corresponds to the path are incremented by 1. This procedure is repeated for n best paths.

For the rate-1/2 voice channel coding, two survivors normally leave and enter state i at any given instant. The better of the two paths entering state i is retained for further expansion. However, for the second best path estimation, four links are considered. Two links each from state i and state $i+16$ in time $j-1$ enter state i in time j . Two links are retained for further expansion. The accumulated metric tables, accum1 and accum2, represent the two survivors for state i . The difference between the initial state 0 metrics of the two best paths (that is, $\text{accum2} - \text{accum1} = N$) serves to maintain an initial offset between the two most likely paths. This allows the two paths to possibly diverge later in time. The actual value of N is system-dependent and can be determined experimentally.

The knowledge of the second best path, the third, etc., is utilized by the voice channel decoder in this way: if the CRC syndrome is nonzero for the best path, the decoder output contains errors. In this case, the second best estimate of the transmitted data is considered. If the CRC check is successful on this estimated sequence, then it is selected as the decoder output. Otherwise, the next best path is considered. This procedure is repeated either until an estimated sequence with zero syndrome is found or until the L best candidates fail. In case of failure, the current speech frame is marked bad, and a frame-masking procedure is initiated as specified by the IS-54 standard.

Implementation Details

Programmable DSPs are widely used in digital cellular mobile unit and base station designs. The high-performance TMS320C5x is especially designed for digital cellular applications. The newest member of this generation, the TMS320C53, provides a low-cost, low-power DSP engine with more than 20K words of on-chip memory. Its 35-ns fast instruction cycle time, large on-chip memory, and programmable power-down modes make it especially suitable for hand-held telephone designs.

The GVA is implemented on a TMS320C53. The 'C53 min/max instructions facilitate a search algorithm for trellis expansion. Its dynamic bit testing and zero-overhead loops efficiently implement a trace-back routine.

The serial GVA algorithm is chosen for two primary reasons:

- The relatively insignificant increase in computational overhead when compared to a conventional VA
- Less memory usage compared to other types of GVAs

The first pass of the GVA algorithm (that is, search for the best path) is identical to a conventional VA. The only additional overhead is the update of the state count array during the trace-back stage. The second pass of the GVA (if required) is more complicated. In this case, two out of four possible survivors are selected. This normally requires a binary search of the accum1 and accum2 tables (for a total of five comparisons). However, when an ordered list of accumulated metric tables is maintained, only two comparisons are required. Moreover, comparison is required only for the trellis points for which h_{ij} is nonzero, as previously discussed. Table 1 summarizes the result of a TMS320C53 implementation of conventional VA and serial GVA algorithms. Although the serial GVA takes longer to find the second best path, it is required to do so only if the CRC syndrome fails on the best path. Therefore, the computational requirement of the serial GVA averages out over varying channel conditions.

Table 1. Algorithm Execution Time on a 35-ns TMS320C53

	Conventional VA	Serial GVA	
		Best Path	Second Best Path
Trellis Expansion	1.15 ms	1.15 ms	3.1 ms
Trace-back	31.15 μ s	46.7 μ s	46.7 μ s

The other advantage of this algorithm is its conservative memory requirement. The two main system design constraints of a portable dual-mode phone are small form factor and low power consumption. Both preclude a design from having a large amount of expensive static RAMs. Since the algorithm serially finds the globally best estimates, there is no need to save path histories of the previously found paths. Therefore,

one state path history buffer suffices for this application. Table 2 compares the memory requirement of a serial GVA that finds two best paths with the memory requirement of a conventional VA. Both algorithms are implemented on a TMS320C53 processor.

Table 2. Memory Requirement

	Conventional VA [†]	GVA [†]
State Path History	192	192
State Count	–	192
Accumulated Metric	32	64 [‡]

[†] Number of 16-bit words required

[‡] For best and second best paths

Results

The performance of the GVA in comparison with the conventional VA is shown in Figure 2. The modulation scheme used is phase-shift keying (PSK). The results are measured over a simulated additive white Gaussian noise (AWGN) channel. Figure 3 shows the path history of the voice channel encoder for a sample input sequence. It also shows the best estimated path and the second best path traces. Note how the second best path diverges from the best path briefly and remerges with it subsequently. If the best path diverges only once from the actual encoder path, it is likely that the second best path will match the encoder path.

Figure 2. Simulated Bit Error Rate of Serial GVA Versus VA

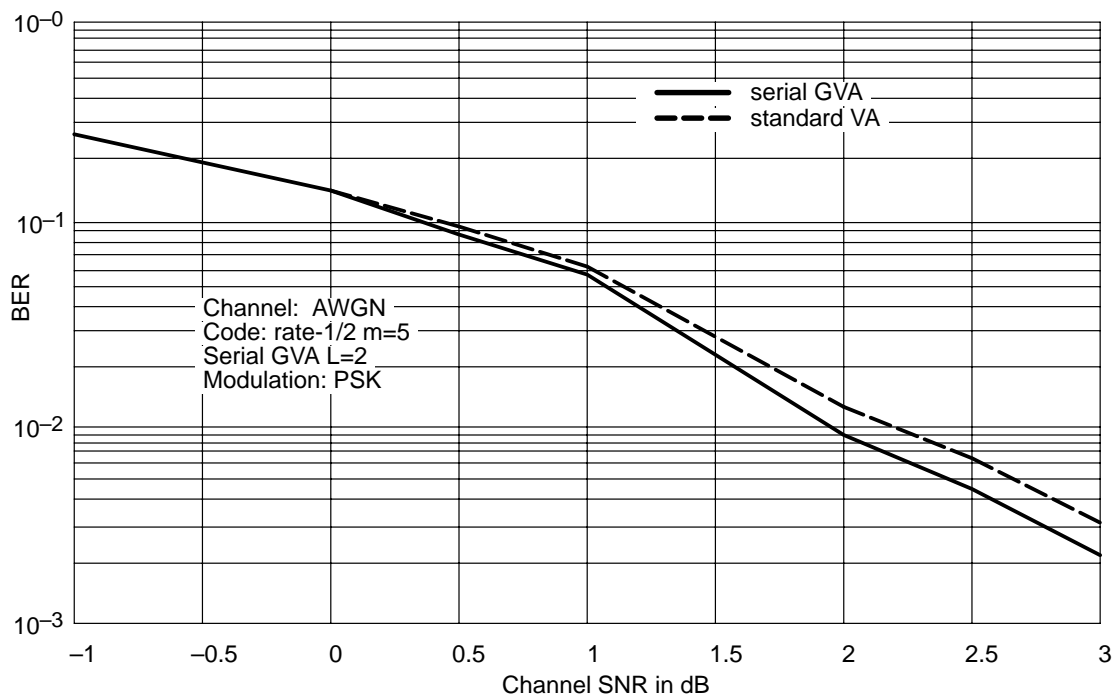
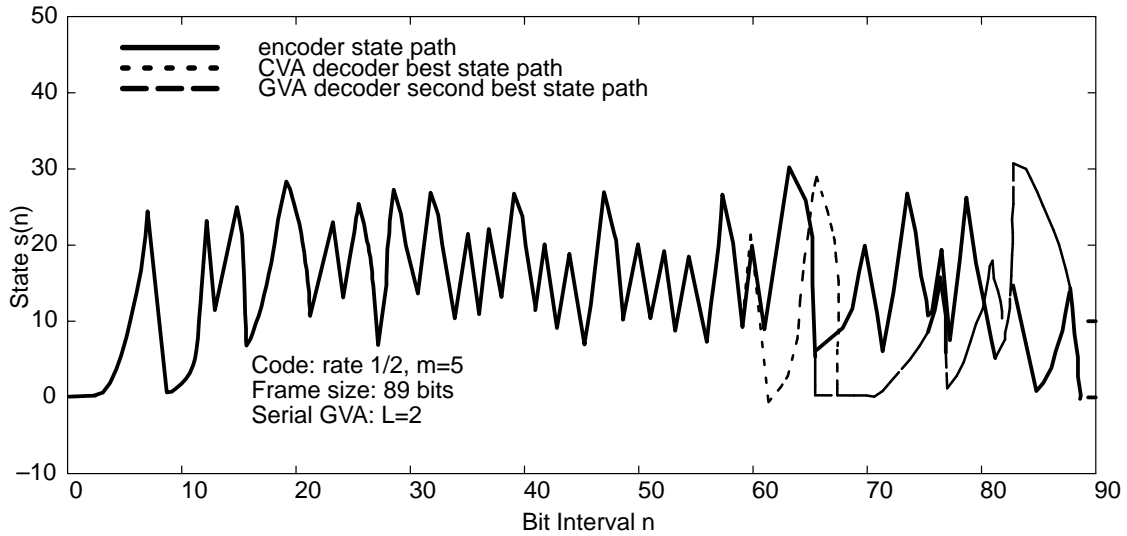


Figure 3. State Path History Trace



Conclusions

In general, modified Viterbi algorithms offer improved performance of a forward error-correction design at the expense of more computational overhead and added complexity. This paper presents an FEC subsystem for a USDC voice channel that uses a generalized Viterbi algorithm [1] to combat bit errors under noisy channel conditions. It shows that the proposed FEC design performs better than a standard Viterbi-based design. Furthermore, the FEC design does not require significant increase in memory space and processing power. The algorithm is implemented on a digital signal processor, the TMS320C53. The experimental results indicate that even when the proposed algorithm is restricted to two best estimates of the transmitted sequence (that is, $L = 2$), its bit error rate is less than that of a standard Viterbi algorithm operating under similar channel conditions. Further performance improvement is achievable if more than two estimated sequences are generated.

References

1. Seshadri, N., and Sundberg, C-E. W., "Generalized Viterbi Algorithm for Error Detection With Convolutional Codes", *GLOBECOMM '89 Conference Records*, pp. 43.3.1 – 43.3.4.
2. Hagenauer, J., and Hoher, P., "A Viterbi Algorithm With Soft-Decision Outputs and Its Applications", *GLOBECOMM '89 Conference Records*, pp. 47.1.1 – 47.1.7.
3. *Cellular System: Dual-Mode Mobile Station – Base Station Compatibility Standard*, IS-54 Project Number 2215, Electronic Industries Association, December 1989.
4. *TMS320C5x User's Guide*, Texas Instruments, 1993.
5. Hashimoto, T., "A List-Type Reduced-Constraint Generalization of the Viterbi Algorithm", *IEEE Transactions on Infinity Theory*, Volume IT-33, November 1987, pp. 866–876.
6. Schaub, T., and Modestino, J.W., "An Erasure Declaring Viterbi Decoder and its Applications to Concatenated Coding Systems", *ICC '86*, 1986, pp. 1612–1616.

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