Optical Quality Assurance With Parallel Processors

Application Report

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Introduction

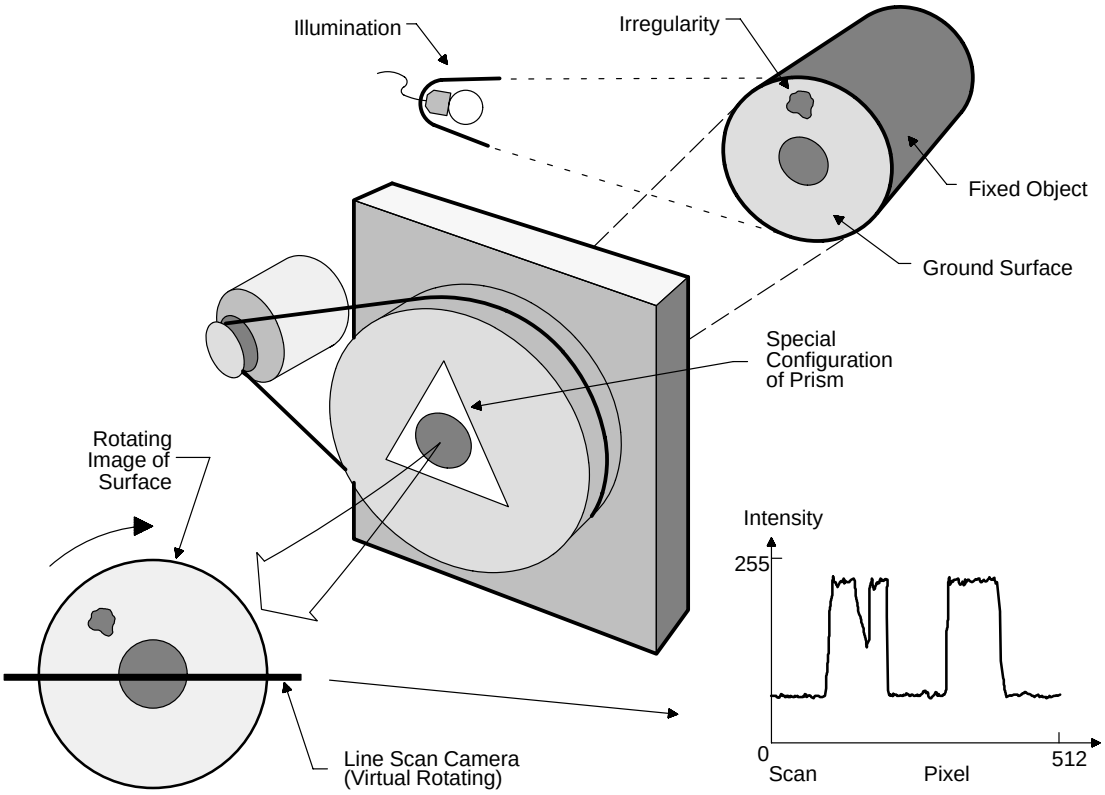
Within the field of industrial production, quality assurance is an important component, which must fulfill increasing requirements. The quality of production machines and the production speeds require that high-performance systems be able to control products in real time (e.g., 20 parts per second or several meters per second). This article describes a way to assure quality on the basis of digital imaging and signal processing with parallel signal processors for machine communication.

Due to its high computing rate and its capability to communicate via six parallel high-speed interfaces (20 Mbytes/second each), the first parallel digital signal processor, the Texas Instruments TMS320C40, is particularly suitable for image processing and forms the basis of the design. Transputers, on the other hand, are used mainly as flexible and high-performance machine controllers.

Overview

The application this paper describes is a system for securing the quality of surfaces — for example, those on front surfaces of roller bearings. The front surface is captured by means of a line scan camera with a maximum of 400 scans (512 pixels) per surface. The pixel data per line are analyzed and classified by algorithms. A rotating prism virtually rotates the surface to be examined. The line scan camera and the object to be tested are mechanically fixed during data acquisition. During the test procedure, the object is illuminated homogeneously. The line scan camera captures differences in light (256 gray steps) resulting from the surface. This application is illustrated in Figure 1.

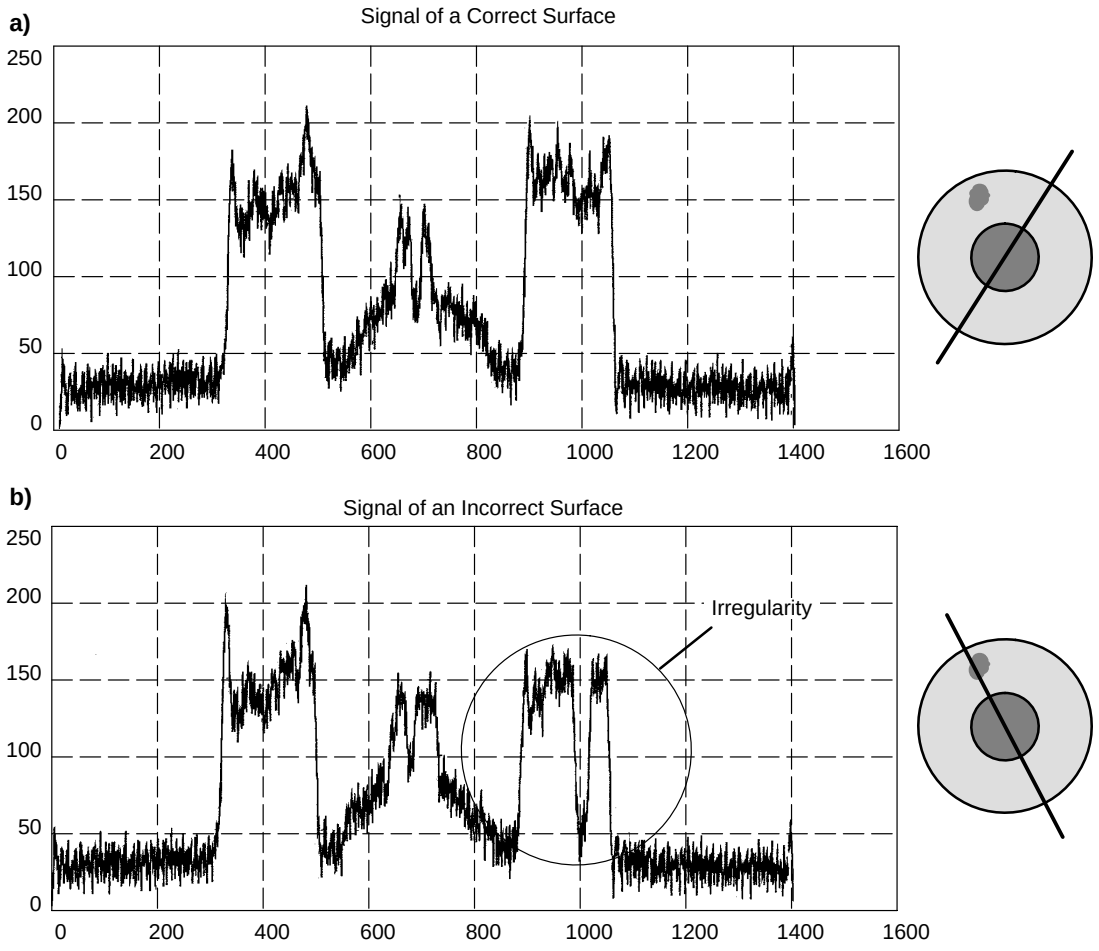
Figure 1. Surface Quality Scan Application



The signals of the line scan camera show characteristic shapes. Figure 2(a) shows a scan through a correct surface; Figure 2(b) shows a curve of an incorrect signal. This irregularity should be recognized and classified by the digital quality assurance system.

So far, this application has been built with analog hardware components (comparators, filters), revealing the common defects, such as aging of the components (parameter drift) and dependency on temperature. Nonrelevant zones of the signal (regardless of the object) cannot be extracted by the analog technology. Although the speed of common analog computer components is advantageous, digital processors are more flexible. Different mathematical algorithms can be implemented for classification. All results are reproducible. Nonrelevant zones can be extracted before the signal analysis. The computer performance will thus be concentrated on the essential test fields. The most important benefit is that you will be able to increase the system's performance later by improving the algorithms.

Figure 2. Measured Signal



The time requirements of a digital classification system are calculated with the following formula:

f(pixel clock of the line scan camera) = No. of pixels/s × No. of scans

- pixel clock of the line scan camera : 10 MHz (maximum)
- 5–20 objects/s
- 512 pixels (8 bits) × 400 scans (20 objects) = 4,096 Mbytes/s (average data rate)
- 10 Mbytes/s (peak data rate)
- TMS320C40 for image and signal processing
- Transputers for machine control

The number of scans per object, multiplied by the number of pixels per scan within one second is a function of the machine cycle. Within one machine cycle, the data of an object are recorded, analyzed, and classified. The required number of objects is a maximum of 20 per second. The pixel clock of the line scan camera is specified with 10 MHz. The required number of scans (400 scans) multiplied by the resolution of the line scan camera (512 pixels) for 20 objects, results in an average data rate of 4,096 Mbytes/s. On average, about 4 megasamples (4 Mbytes) per second must be transferred from the camera to the computer unit. The maximum data rate is calculated from the pixel clock of the line scan camera and amounts to 10 megasamples (10 Mbytes) per second. With conventional processors, this data rate cannot be transferred in real time from the line scan camera to the computing unit.

The Transputer T805 and the TMS320C40 DSP

The Texas Instruments TMS320C40 digital signal processor is not only able to manipulate big data quantities (275 MOPS and 50 MFLOPS), but also transfers up to 20 Mbytes/s per communication link. Inmos transputers control the recording, manipulation, and display of objects.

The ’C40 parallel DSP shows structures similar to those of a transputer. The performance, however, is 10 to 30 times better than that of a T805. The high-speed links are essential characteristics of parallel processors. The principle of the communicating sequential processes (CSP) model has been developed by HOARE and is the basis of parallel processing. Several software processes are running on one or more processors and communicate via the fast links for data exchange or via soft channels on one chip.

The parallel processors (the ’C40 and the transputer) are connected to each other via an Inmos-Link Adapter or dual-port RAM. The connection to the transputer world is most easily done via a transputer link adapter. This link adapter is implemented on the DSP1 (’C40 board) and converts two ’C40 links to the serial transputer link (one transputer link consists of link-in and link-out). Due to its serial data transmission, the transputer link represents a bottleneck. The data transfer between the DSP and the transputer is restricted to about 1 Mbyte/s by the serial link. But for parameters, configuration, and results, this data rate is adequate.

An increased data transfer rate is obtained by means of dual-port RAM, whereby the DSP 1 card is plugged into a 4-fold transputer card (TR3-N) as a piggyback board. The communication rate via DPRAM amounts to about 15 Mbytes/s. Figure 3 shows block diagrams of the T805 and the TMS320C40, and Figure 4 shows the interconnection.

Figure 3. Transputer T805 and the DSP TMS320C40

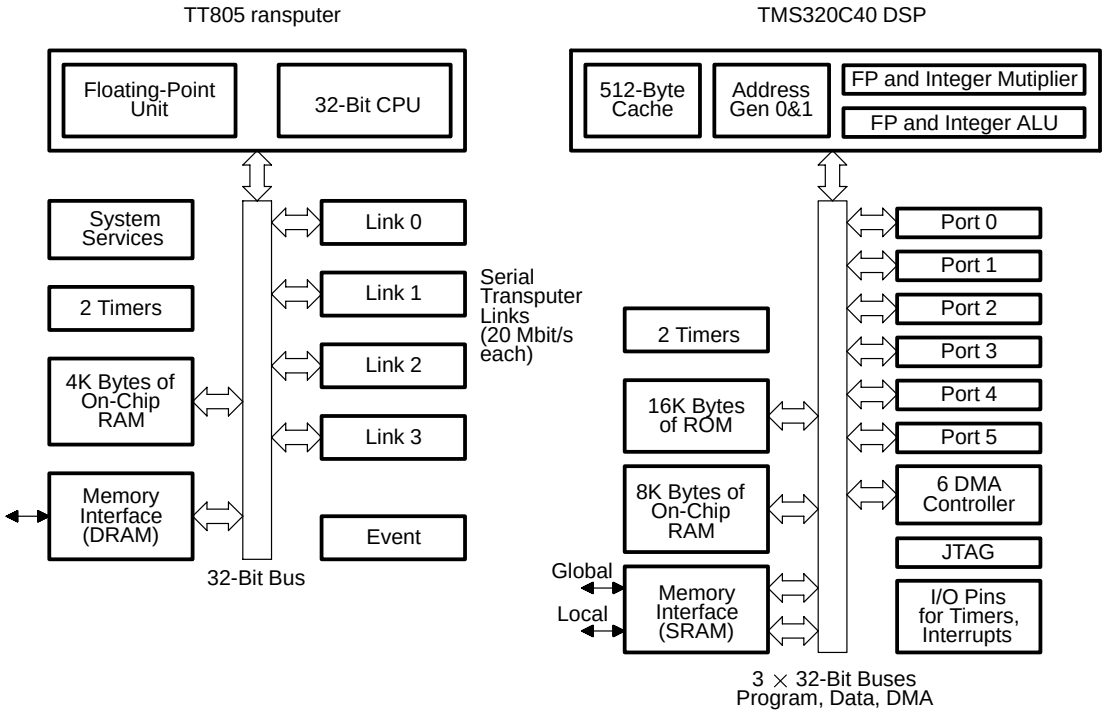
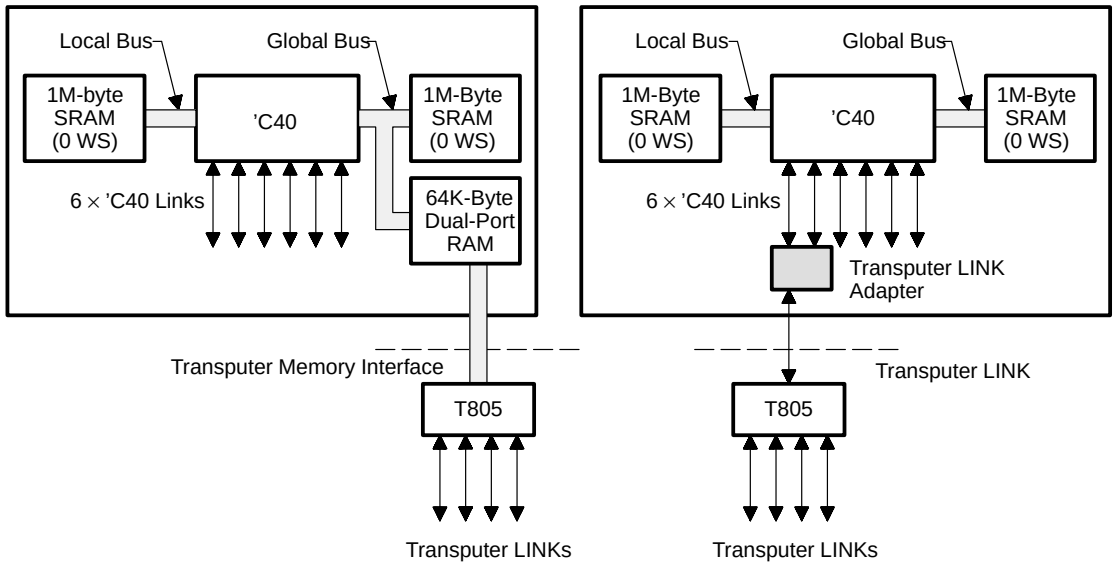


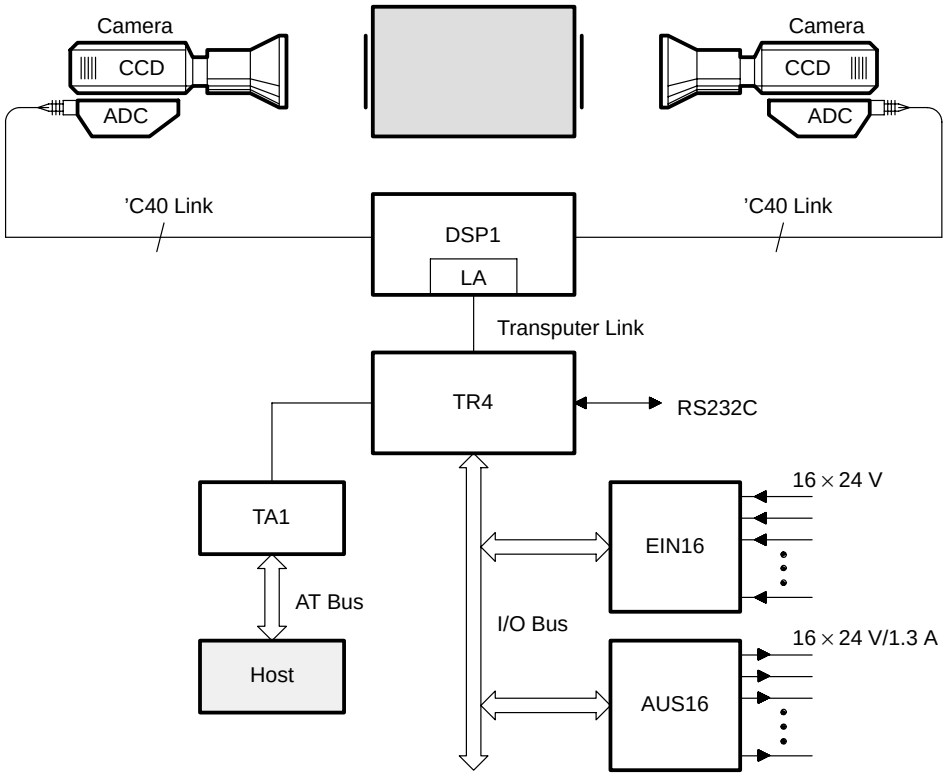
Figure 4. Interfacing the TMS320C40 and the Transputer



Hardware

The complete hardware concept of the quality assurance system is composed of the individual components for signal/image processing and control shown in Figure 5. The signal and image processing is designed for two test surfaces; that is, two cameras simultaneously examine two front surfaces, which are further analyzed and classified by a DSP. The cameras are each equipped with an 8-bit A/D converter, enabling the pixel data to be transferred directly to the ’C40 via the ’C40 link. The classification result is transferred in the form of command signals to the command section via the transputer link. The command section consists of a transputer card (TR4), on one side controlling digital inputs and outputs and on the other side managing the connection to the host computer. Via the digital inputs, signals from the machine are received (the object is ready for scanning); via the outputs, the machine is influenced (locked during scanning). The host computer (PC) represents the interface between user and application.

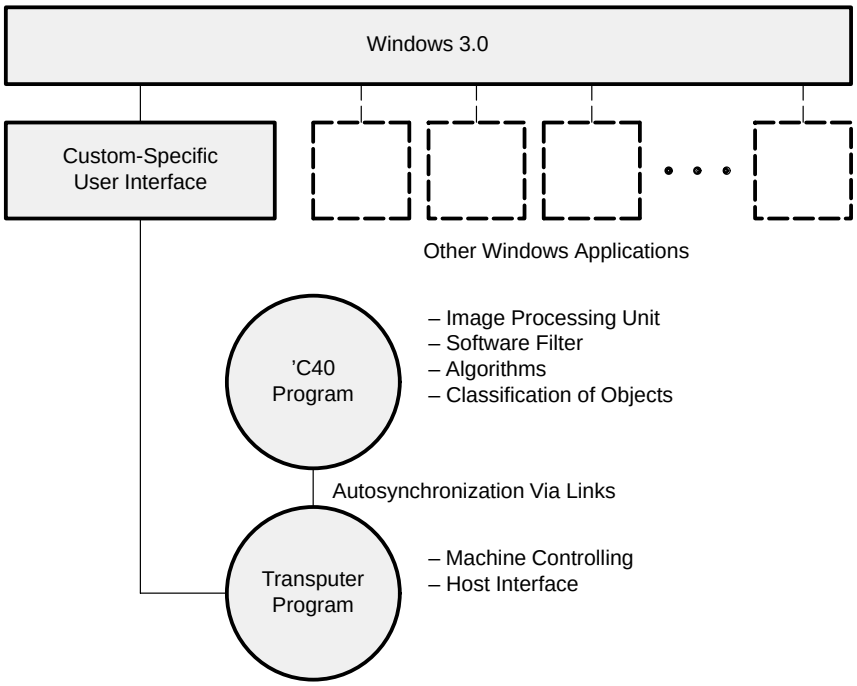
Figure 5. Overall Concept on Hardware



Software

The software is a Windows 3.0 application and is shown in Figure 6. This interface was chosen because it is user friendly. The customer-specific Windows 3.0 application initiates the transputer program. The transputer software carries out the machine command/control and produces the connection to the host. The software on the ’C40 is loaded from the transputer to the ’C40 and effects the classification by means of digital filters, different algorithms, and different types of image/signal processing. Both software modules (transputer and ’C40) synchronize and communicate via the ’C40/transputer link.

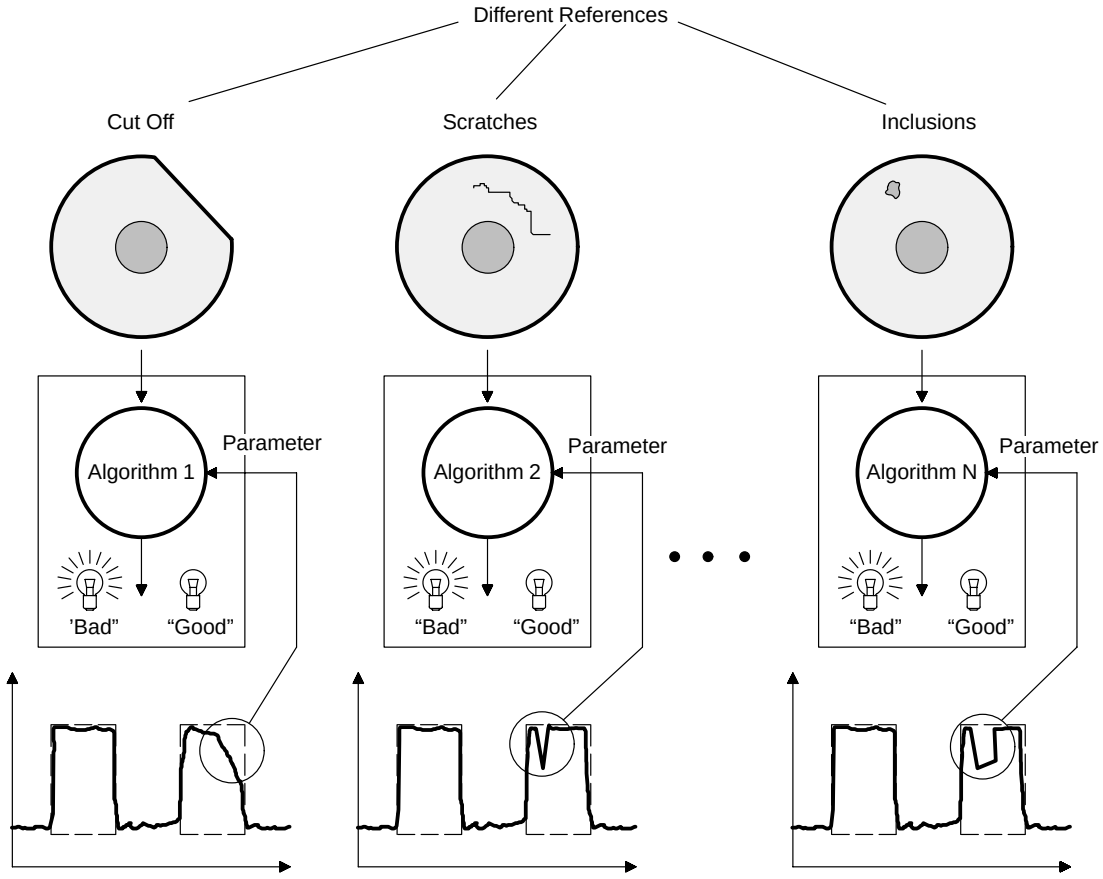
Figure 6. Overall Concept on Software



Algorithms

Before the classification of different objects can be carried out, the parameters of the implemented classification algorithms must be fixed. User parameters condition the algorithms to search for specific defects and return a “good” or “bad” result, as shown in Figure 7.

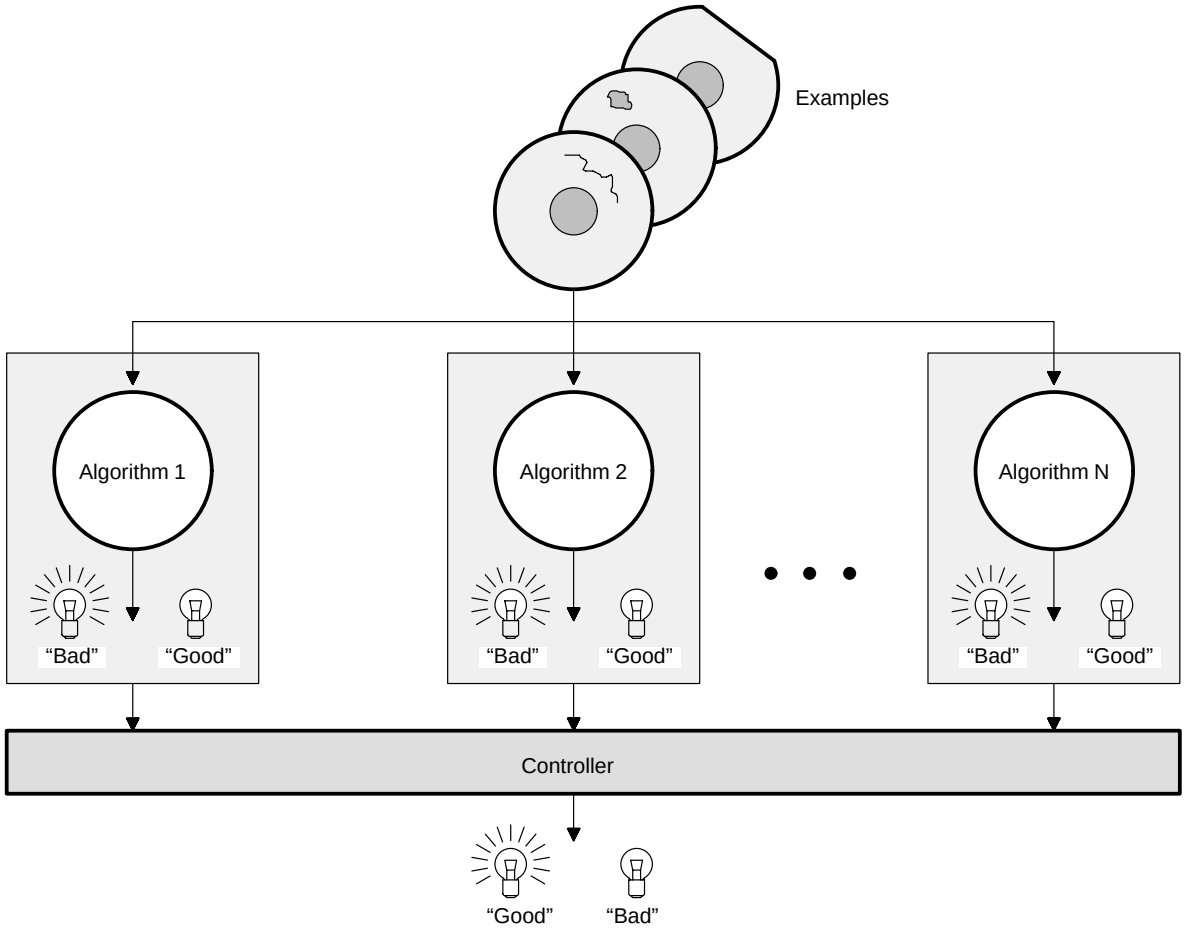
Figure 7. Setup of Algorithms



Object Recognition

In the classification phase, different objects are now transmitted in real time to the application. The results of the different algorithm modules are collected and evaluated by an overall controller. On the basis of these partial statements, the controller produces a general statement on the quality of the tested part. See Figure 8.

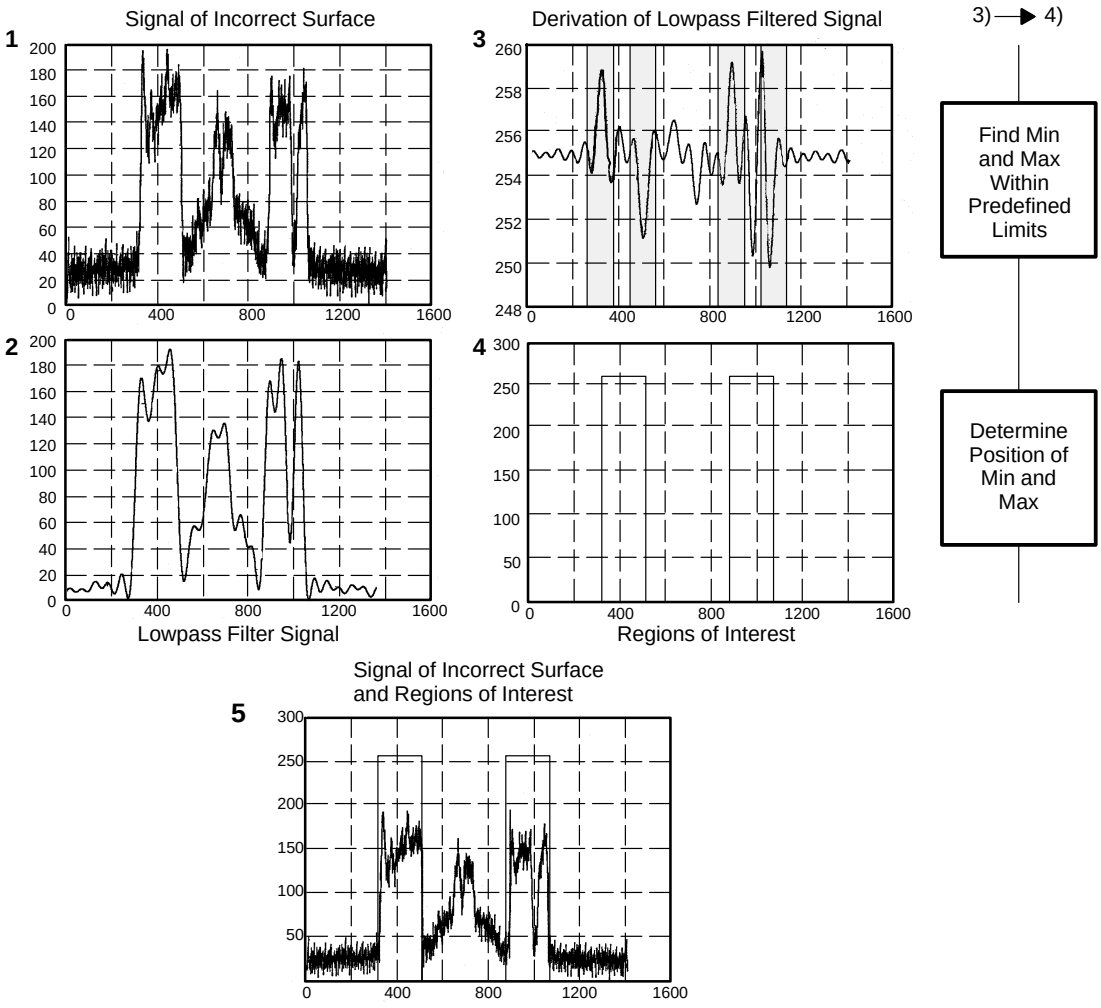
Figure 8. Recognition of Objects



The signal curves in Figure 9 show an example of separating relevant signal sections by means of digital signal processing. The two plateaus of an incorrect surface signal should be separated. Ideally, the signal is low-pass filtered to remove noise. The low-pass filtered signal will be differentiated to extract the edges. Within predefined limits, minimum and maximum are now determined; their positions will give information on the edge points of the plateaus.

Different signal processing algorithms (e.g., FFTs) can now be applied to these separated regions of interest.

Figure 9. Signal Filtering, Derivation and Max/Min Calculation



Conclusion

This example shows an application with parallel processors in industrial environments, where communication processors with DSP characteristics are required for signal and image processing. The main advantage of parallel processors is that the performance is made scalable by adding more processors. The interprocessor communication is guaranteed by high-speed interfaces, which transfer data independently of the CPU.

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