AMELIA — An A/D-D/A Interface to the TMS320C40 Global Bus

Application Report

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SPRA106
February 1994

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Introduction

AMELIA is Loughborough Sound Images' (LSI) Analog ModulE Link Interface Adapter. It is used on a number of LSI's development boards, including those that use the TMS320C40 DSP from Texas Instruments. It allows you to build a modular interface system that can be upgraded as technology progresses. In addition, AMELIA uses none of the 'C40's parallel communication links, so the processing system maintains its flexibility.

This application note describes the broad functionality of AMELIA, how it integrates analog and digital operations, and how it enhances the interface options open to the system builder.

Analog Conversion — A Brief Overview

The large number of 'C40 systems that connect to the outside world via an application-specific analog interface require a range of solutions. In these solutions, it is crucial that data be presented to the processor accurately to maintain its value.

A number of analog interface devices have been available for some time and the comparison has been made primarily in terms of conversion bandwidth, or how fast the converter can operate. The tradeoff has been in the conversion performance, or accuracy of the device. Generally, the wider the bandwidth, either the resolution of the converter (number of bits) or the signal-to-noise ratio is reduced. Thus, it is common to find converters with 8-bit resolutions that operate in the megahertz sampling range, but 16-bit devices are limited to hundreds of kilohertz.

Today, there is a much greater concern for accuracy of conversion. Ultimately, the application determines the exact performance requirements: from 8-bit servo control and 10- to 14-bit requirements of telecomms and radar, through the growing 16-bit arena, to the digital audio applications requiring 24 bits of resolution. Consequently, users are becoming more selective, and a single general-purpose device cannot fulfill all requirements.

Modular Interface Design Techniques

A modular approach to interface design makes possible a range of interface solutions to meet the requirements of all the varied applications. A modular design also protects earlier investments when you update your system.

Analog conversion techniques are progressing at a fast pace in the semiconductor industry; this means that traditional methods of design in which the converter is mounted on the same PCB as the DSP are somewhat limited. If your application would benefit from the improved performance that a new device can provide but your system has a traditional design, the whole system must be replaced, including DSP technology that may still be current. With the modular approach, the new module simply replaces the old, maintaining your investment in the 'C40 processing system.

LSI's modular technique attaches a separate PCB directly to LSI's 'C40 boards on both the PC and VME chassis; the PCB remains within the single height constraints of those systems. This approach realizes other benefits in the performance of the system. A single-board system has inherent flaws in the way that digital noise easily transmits into sensitive analog components and imposes an upper performance limit that is less than optimal. When the analog section is removed from the digital PCB, system performance figures approaching those of the converters are achieved. This is attributed to better isolation between the two sets of components.

Analog component layout also accounts for performance differences. With a single-board system, cost constraints on total system design prevent repeated changes on the circuit board. Consequently, a number of these systems rely on analog interfaces that exhibit suboptimal performance. Having a separate board for the analog interface affords two advantages: the layout problem is eased, and a new analog design can proceed independently of the digital system, allowing a more rapid time to market with a new design.

A modular interface design technique is now in place at LSI. To illustrate the performance benefits with the ’C40, typical measured figures are 90 dB signal to noise and distortion for a delta-sigma converter, and 84 dB for a 200-kHz successive approximation device. These figures were measured with the complete assembled system inserted into the host platform.

AMELIA

To develop a modular system, it was first necessary to find a common way in which to interface a wide range of conversion modules to an equally wide range of DSPs. The paramount consideration for LSI was flexibility so that all functionality of the DSP could be available; this precluded the use of serial ports on ’C3x and ’C5x devices. Additional design objectives were to avoid consuming a ’C40 communication link and to consider the differing connection methods and protocol requirements. The best solution was to memory map the analog interface.

Memory mapping solves the problems of interfacing to different TI DSP families and does not remove any device functionality. AMELIA serves as the link between the DSP and the interface device, absorbing any interconnection differences.

The basic functional blocks of AMELIA are shown in Figure 1. The device is produced in a 2000-gate FPGA and is packaged in a 68-pin PLCC. The pin assignment is shown in Table 1. AMELIA provides two synchronous serial ports for the ’C40. Sixteen-bit data words are transmitted and received under control of the sophisticated frame sync logic. The flexibility of that logic is ideally suited for connection to a wide range of A/D, D/A, and other serial communication devices. The ’C40 and serial sides of AMELIA operate asynchronously to each other. They can handle very slow peripherals without slowing the ’C40; the DSP is interrupted only when the data is ready for processing.

Figure 1. Block Diagram

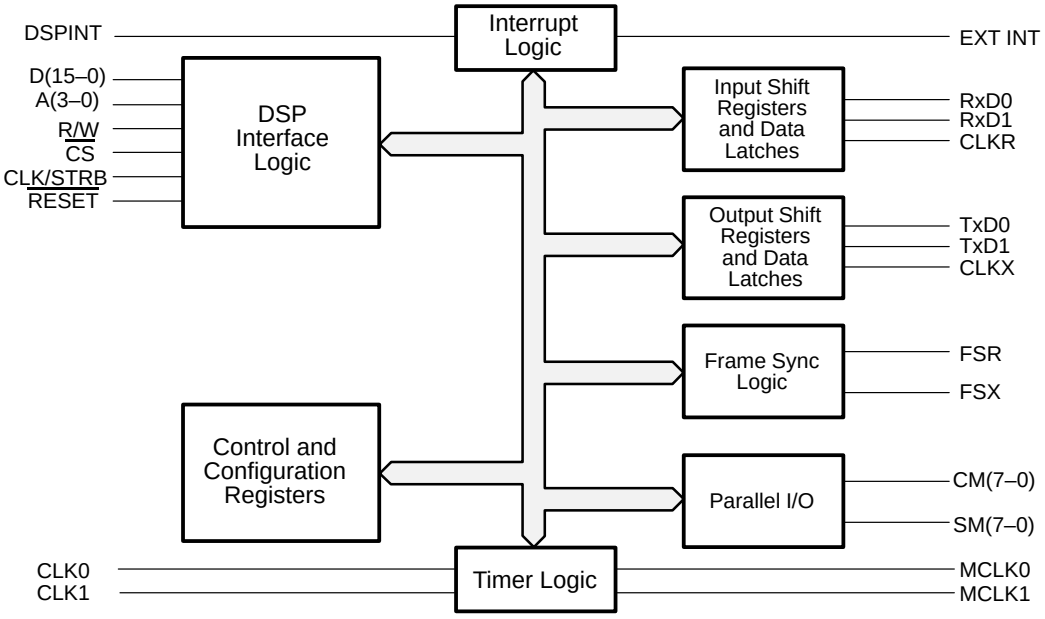


Table 1. Pin Assignments

Pin Name	Pin Number	State	Description
Analog Control/Status			
CM0 CM1 CM2 CM3 CM4 CM5 CM6 CM7	34 33 31 30 29 28 27 26	O	Control port to the analog daughter module.
SM0 SM1 SM2 SM3	39 37 36 35	I	Status port from the analog daughter module.
Analog Serial Bus Interface			
CLKR	52	I	Serial receive clock. This is the serial shift clock for both receive channels.
CLKX	47	I	Serial transmit clock. This is the serial shift clock for both transmit channels.
FSR	53	I	Frame synchronization pulse for the serial receive channels.
FSX	48	I/O	Frame synchronization pulse for the serial transmit channels.
RXD0 RXD1	50 51	I	Data receive for channel 0/1. Serial data for channel 0/1 is received on this pin.
TXD0 TXD1	45 46	O	Data transmit for channel 0/1. Serial data for channel 0/1 is transmitted on this pin.
DSP Parallel Bus Interface			
A0 A1 A2 A3	11 12 13 16	I	Four-bit address port.
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	61 62 63 64 65 67 68 1 2 3 5 6 7 8 9 10	I/O/Z	Sixteen-bit data port lines.
$\overline{CS}$	18	I	Chip select. When an access is performed, this signal must be low.
CLK/ STRB	19	I	Clock or strobe signal. This signal generates early write strobes for write cycles if the data hold time is insufficient for the device.

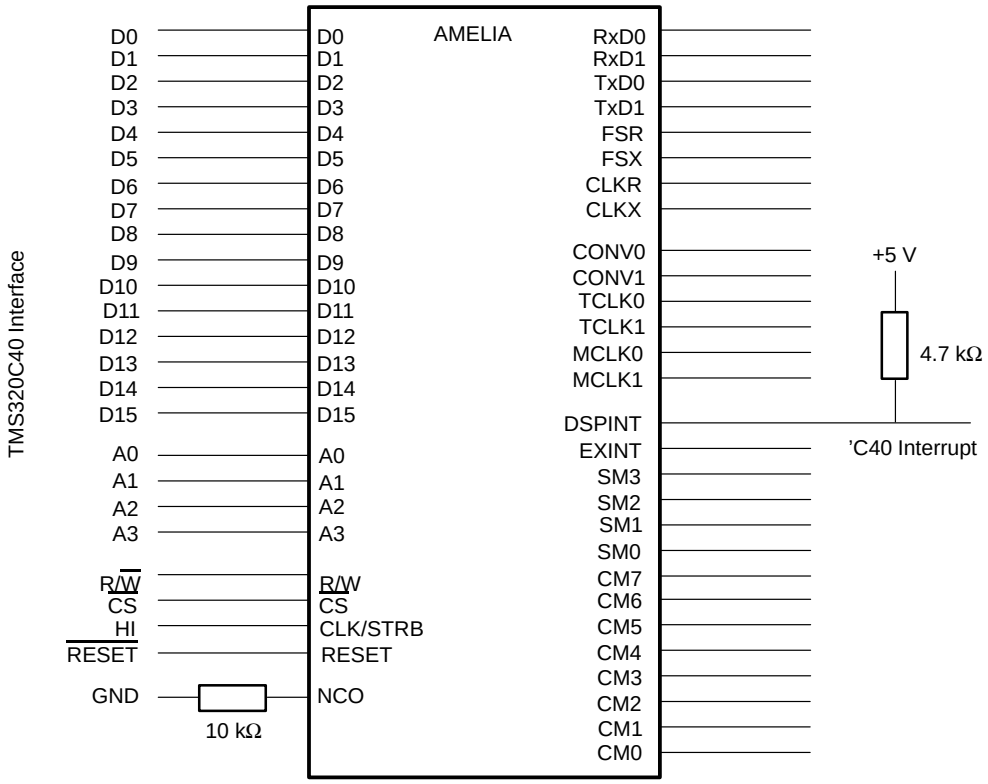
Table 1. Pin Assignments (Continued)

Pin Name	Pin Number	State	Description
$\overline{\text{RESET}}$	20	I	Reset. When this pin is low, the device is placed in the reset condition.
R/$\overline{\text{W}}$	17	I	Read/write signal When a read is performed, this signal must be held high. When a write is performed, this signal is low.
Interrupt			
DSPINT	22	O	Open-collector interrupt on the DSP. Interrupts generated by the serial interface or by an external interrupt source can be output to the DSP on this pin.
EXINT	44	I	External interrupt. Interrupts generated on this pin can be passed through to the DSP.
Miscellaneous			
NC0	54	Z	Unused pin. This pin must be terminated to ground via a 10-kΩ resistor.
NC1 NC2 NC3 NC4 NC5 NC6	59 56 57 58 60 40	Z	Unused pins. These pins must be left unconnected.
Power Supply			
GND1 GND2 GND3 GND4 GND5	14 15 32 49 66	GND	Ground pins.
V_{CC1} V_{CC2} V_{CC3} V_{CC4} V_{CC5}	4 21 25 38 55	V_{CC}	+5-Volt supply pins.
Timer			
CONV1	41	O/Z	Conversion pulse generator 1 output. This pin outputs pulses generated by timer 1 as programmed from the DSP interface.
MCLK0 MCLK1	42 43	I/O	Master clock. When configured as an input, this clock can drive either of the two internal timers. As an output, this pin is driven by the timer clock TCLK0/1.
TCLK0 TCLK1	23 24	I	Timer clock. The clock on this pin can drive either of the two internal timers; its source is on the motherboard.

AMELIA has three main components: a DSP parallel interface section, a synchronous serial interface, and a sample-rate generation section.

The parallel section is connected onto the ’C40 global (or local) bus with no signal modifications, as shown in Figure 2. AMELIA uses 16 bits of data and just four address lines; its signals include read/write, chip select, a clock input, and chip reset. The functional block includes data buffers and multiplexers, internal address decoders, and an interrupt generator. Interrupts can be generated from three different sources: receive register full, transmit register empty, and external interrupt signals received from the daughter module. This provides a flexible method of data transfer control.

Figure 2. AMELIA Circuit Connections



The timer section comprises a full 16-bit reloadable time-out counter and a divide-by-1,-2,-4 or -8 prescaler. The timer can be independently clocked from one of four sources, any of which can be used to provide the sample rate clock. The LSI 'C40-based board has a socketed oscillator that can be used for this purpose. The clock source is a user-selectable feature because sample rate sources are already provided on the analog interface modules.

The control and configuration block is a software programmable section that gives AMELIA its wide operating characteristic. These controls make it possible to accommodate a wide range of serial standards found on converter devices. Most converters use a form of synchronous serial interface (SSI), but this varies across manufacturers. The main differences are the phasing and the type of frame sync signals that control the transfer. AMELIA has sophisticated frame sync shaping circuitry to accommodate as wide a range of protocols as possible. As a result, AMELIA can input FSR and FSX signals in bit, word, or I2S formats with either normal or inverted polarity and can also generate FSX in any of these protocols.

The parallel I/O block provides eight digital outputs (CM7–0) and four digital inputs (SM3–0). These are general-purpose signals that can be used to provide autoconfiguration, control, or status information about the interface module being used. Analog interfaces use this feature to configure converter-specific signals on the modules.

The present version of AMELIA is a two-channel design incorporating two input and two output channels. As such, AMELIA integrates two parallel-to-serial and two serial-to-parallel converters. For analog data input, data is read from the analog module under control of the frame sync logic and transferred to the data

latches, which are then read by the ’C40. Data sampling is synchronous because both data channels are driven from the same clock source.

From performance measurements of AMELIA, the maximum clock rate that can be accommodated at the serial interface is 12 MHz. This gives adequate bandwidth for a wide range of devices to be interfaced to the ’C40.

Programming Interface

AMELIA can accommodate a wide range of fundamentally different conversion techniques. To implement this, the ASIC incorporates a high level of programmability. All control signals generated for the converters are configurable in terms of polarity. The duty cycle of the sample rate trigger is selectable as either a pulse train or as a square wave, allowing both delta-sigma and successive approximation parts to be accommodated. Because of the fundamental differences in the operation of these conversion standards, the delta-sigma converter requires a sample rate clock, whereas successive approximation devices need a stream of conversion pulses to operate.

This level of flexibility requires a block of 16 address locations from the ’C40. These locations include both channels’ input and output data registers, timer programming register, and the control and configuration registers. Also, a number of locations are reserved for future enhancements. The register map is shown in Table 2.

Table 2. Register Map

Location (Hex)	Read	Write
9000 0000	NU	NU
9000 0001	NU	NU
9000 0002	Ch0 Input Data	Ch0 Output Data
9000 0003	NU	NU
9000 0004	NU	NU
9000 0005	NU	Timer1
9000 0006	Ch1 Input Data	Ch1 Output Data
9000 0007	NU	NU
9000 0008	NU	User control
9000 0009	NU	NU
9000 000A	Analog Status	Analog Control
9000 000B	Interrupt Status	Interrupt Mask
9000 000C	NU	NU
9000 000D	NU	NU
9000 000E	NU	NU
9000 000F	NU	Configuration

NOTE: NU = Not Used.

Once the configuration for the analog module is complete, the details of the control registers may be ignored. The programming task is reduced to writing five prepared control words. Example 1 shows a two-channel echo program that simply reads data from the ADC and immediately writes that data back out to the DAC.

Example 1. Two-Channel Echo Program

```
*************************************************************************
*                                                                       *
*   ECHO example program.                                               *
*                                                                       *
*   ECHO initializes the AM/D16DS on the DPC/C40 and echoes the         *
*   input on each channel.                                              *
*                                                                       *
*************************************************************************

              .data

STACK         .word   002ffc00h       ;Define stack space
IACKLOC       .word   80000000h       ;Interrupt acknowledge location
IVECTAB       .word   002ff800h       ;Interrupt vector table
CHANA         .word   90000002h       ;Channel A address
CHANB         .word   90000006h       ;Channel B address
UCR           .word   90000008h       ;User control register address
ACR           .word   9000000ah       ;Analog control register address
IMR           .word   9000000bh       ;Analog interrupt mask register address
CONFIG        .word   9000000fh       ;Configuration register address

              .text

                                      ;Set up interrupt vector table
               BR     START
              .word   0h              ;Unused interrupts: NMI
              .word   0h              ;TINT0
              .word   0h              ;IIOF0
              .word   ISR             ;Amelia Interrupts on IIOF1

                                      ;Start of program...

START:          LDP     @STACK,DP     ;Initialize the stack
                LDI     @STACK,SP

                LDI     @IVECTAB,R0   ;Set up the interrupt vector table
                LDPE    R0,IVTP

;;;;            Write to the registers within AMELIA...


                LDI     @UCR,AR0      ;User control register
                LDI     0a000h,R5     ;
                STI     R5,*AR0       ;ADMCLK0 to be used
```

```
                LDI     @ACR,AR0            ;Analog control register
                LDI     0a0H,R5             ;
                STI     R5,*AR0             ;48 KHz sample rate
                                            ;AMELIA into reset

                LDI     @ACR,AR0            ;Analog control register
                LDI     0e0H,R5             ;
                STI     R5,*AR0             ;AMELIA released from reset,
                                            ;calibrating

                LDI     @CONFIG,AR0         ;Analog configuration register
                LDI     0b390H,R5           ;loaded with Key value
                STI     R5,*AR0             ;

                LDI     @IMR,AR0            ;Analog interrupt mask register
                LDI     01H,R5              ;Int when RX register full
                STI     R5,*AR0             ;

;;              AMELIA configuration complete. Initialize 'C40

                LDI     0,R3                ;channel a output
                LDI     0,R4                ;channel b output

                LDI     @IMR,AR0            ;AR0 = Interrupt mask register
                LDI     @CHANA,AR1          ;AR1 = channel a input
                LDI     @IACKLOC,AR2        ;AR2 = Interrupt ack. location
                LDI     @CHANB,AR3          ;AR3 = channel b input

                OR     90h, IIE             ;Enable IIOF1 interrupt
                OR     02000h, ST           ;CPU global interrupt

LOOP:           BR     LOOP                 ;IDLE until interrupted

ISR:
                LDI     *AR0,R5             ;read interrupt to clear

                LDI     *AR1,R3             ;Load channel a input –> R3
                STI     R3,*AR1             ;Save R3 –> channel a output

                LDI     *AR3,R4             ;Load channel b input –> R4
                STI     R4,*AR3             ;Save R4 –> channel b output

                RETI

               .end
```

The program begins by initializing the 'C40 stack and interrupt vector table location. AMELIA resides at addresses above 9000 0000h in the 'C40 memory map, placing it on the global expansion bus. The analog

module used in the example was a delta-sigma converter, the AM/D16DS daughter module from LSI. All the specific programming details for the module are included with that product.

To begin analog interface programming, you configure the user control register (UCR). This register defines the clock source to be used on the module and also any prescaler values that may be required. The on-module oscillator ADMCLK0 is selected. The analog control register then selects the sample rate of ADMCLK0 to be 48 kHz. The UCR also controls of the module calibration. The first figure written to the register resets the analog module, and the second write causes the register to enter an offset calibration cycle.

The configuration register defines the correct communication protocol between the ’C40 and the analog module, which has already been defined at LSI, so a simple write to the register is sufficient. In practice, the configuration register sets a number of controls to define clock polarities, a valid clock edge on which to read data, and the frame sync controls.

The interrupt mask register is the last initialization task; the rest of the program is application-specific. The final task to start the system is to enable the IIOF1 interrupt on the ’C40, the signal to which AMELIA is connected.

The data is read and written in the interrupt service routine, which also illustrates the simple software interface to AMELIA.

Conclusion

This article has outlined a significant advance in the techniques required to provide a modular analog interface to the ’C40. The single-chip interface adapter offers a number of advantages: all the functionality of the ’C40 is preserved, converters can easily be exchanged if the requirements change, and the interface modules have a higher performance specification. The combination adds up to a powerful interface solution that can be used to apply generic ’C40 signal processing technology to a range of specific applications.

ADC and DAC conversion is the basis of this paper, but other communication protocols could easily be transferred onto a common interface platform, including RS-232 and PSTN extension line connections. Digital interfaces can also be added, including digital audio, telecomm, and control applications. Adding functionality to the standard platform is a straightforward task.

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