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Interfacing the TLV1544 Analog-to-Digital Converter to the TMS320C203 DSP

Application Report

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Contents

List of Figures

List of Tables

Interfacing the TLV1544 Analog-to-Digital Converter to the TMS320C203 DSP

ABSTRACT

This application report provides a design solution for the interface between the TLV1544 10-bit serial-output analog-to-digital converter and the TMS320C203 digital signal processor. The report includes hardware requirements and three software application examples.

1 Introduction

The analog-to-digital (A/D) interface can present a significant design problem because hardware and software must work together across the interface to produce a usable, complete design. This application report provides a design solution for the interface between the TLV1544 10-bit serial-output analog-to-digital converter (ADC) and the TMS320C203 digital signal processor (DSP). It also provides reference information for further development of hardware and software, especially when using the TLV1548 companion device to the TLV1544.

The information presented describes the hardware and software needed to bridge between the system analog signals and the digital signal processing. The first six sections describe the basic operation of the TLV1544, the TLV1548, and the DSP interface. Sections 7 through 10 contain three example software applications. For additional information and for reference, see the following related documents:

- TMS320C5x User's Guide, literature number SPRU056
- TMS320C5x Data Sheet, literature number SPRS030
- TLV1544 Data Sheet, literature number SLAS139

Figure 1 is a schematic diagram of the hardware.

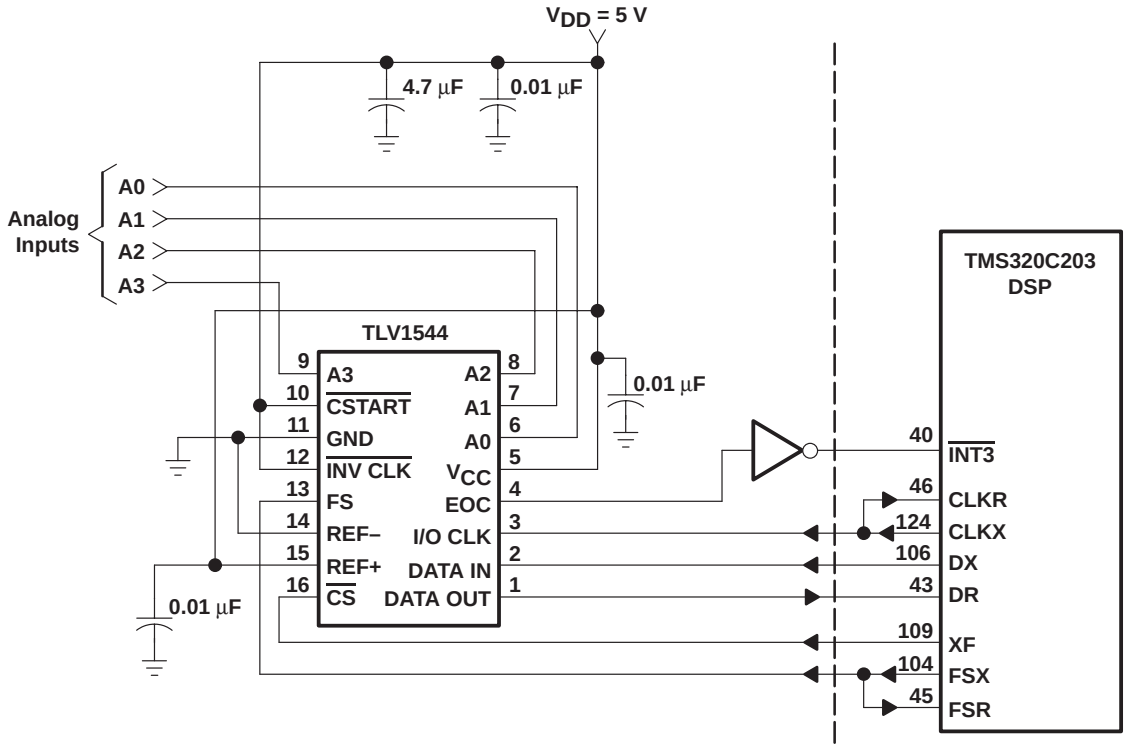


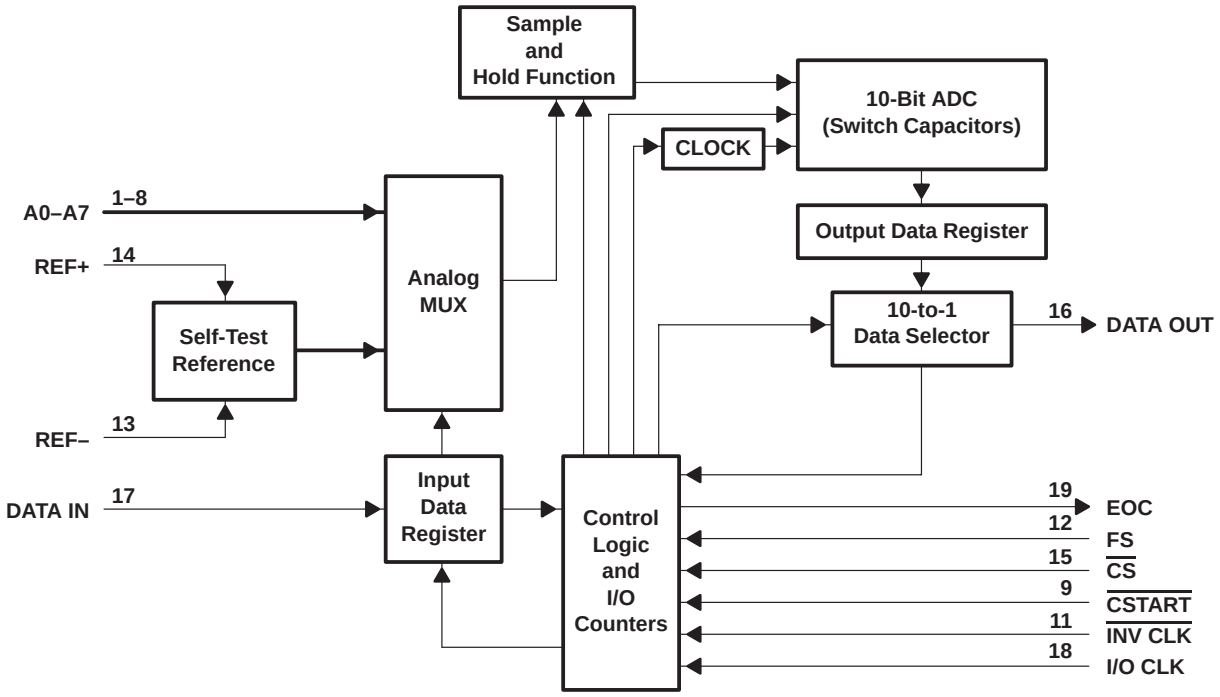
Figure 1. Schematic Diagram

2 TLV1544 and TLV1548 Overview

The TLV1544 and TLV1548 are CMOS 10-bit switched-capacitor successive approximation ADCs. Figure 2 shows the functional block diagram for the devices. The only functional difference is that the TLV1544 has four multiplexed analog inputs and the TLV1548 has 8 multiplexed analog inputs.

Each device has a chip-select ($\overline{CS}$), input-output clock (I/O CLK), data input (DATA IN), and serial data output (DATA OUT). An additional frame sync (FS) input initiates data transfer when using a DSP and connects to the DSP serial port FSX pin.

The $\overline{CSTART}$ input is not used in this application and is tied high. Since the DSP transmit clock, CLKX, already provides the proper phase for the ADC I/O CLK input, the INV CLK terminal is tied high.



Terminals shown are for the DB package.

Figure 2. Functional Block Diagram of the TLV1544 and TLV1548

3 Operational Overview

This application report discusses the software and hardware interface for the TLV1544. The software, however, remains basically the same for the TLV1548 except for the addressing of eight analog inputs instead of four.

This section describes the overall operational sequence of the A/D interface.

3.1 Signal Sequence

As shown in the timing sequence in Figure 3, a high level on the $\overline{CS}$ pin disables the DATA IN and takes DATA OUT to a high impedance state. When taken low, $\overline{CS}$ enables the device inputs, but no data is transferred until the falling edge of FSX is received from the DSP at the FS input of the TLV1544/TLV1548.

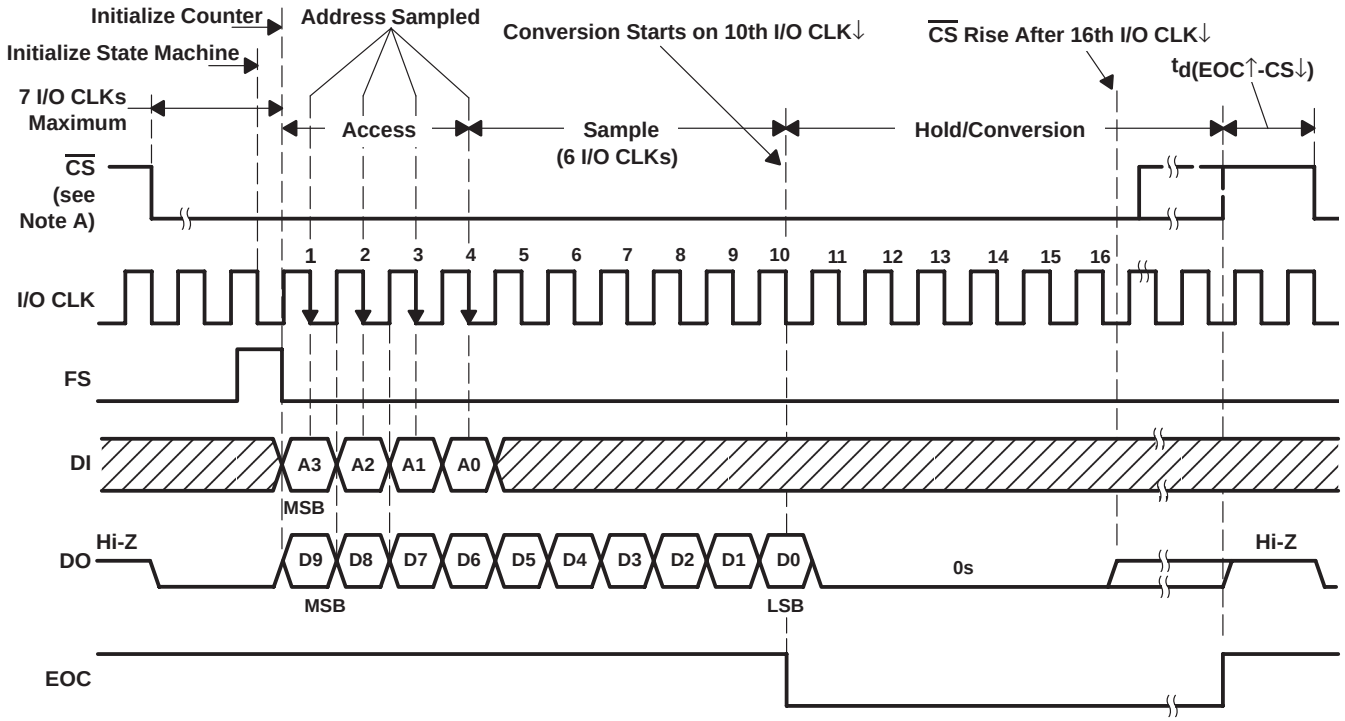
Due to internal counter timing, the maximum allowable time between the falling edge of $\overline{CS}$ and the falling edge of FSX is seven I/O CLK periods. In terms of the software, this means that the high-to-low transition of the DSP XF signal must be at or within 28 instruction cycles of the load DXR command (See the ADC/DSP section). This maximum time is shown as FSD_{max} in Figure 6.

After the falling edge of the DSP FSX, the TLV1544 recognizes the data clock, CLKX, as I/O CLK and receives the 4-bit analog channel address at DATA IN on the first four falling edges of the data clock. DATA IN ignores the remaining 12 clocks.

The channel address selects which analog input channel is converted.

The following six clock periods are the TLV1544 analog sampling time.

During the same 16-clock interval, DATA OUT provides the 10-bit conversion result, padded with 6 zeroes, on the 16 valid clock rising edges after FS goes low. The 10th falling edge of the I/O CLK holds the analog input signal, begins conversion, and takes EOC low indicating conversion start. When conversion is complete, the EOC output goes high indicating conversion is complete and the digital conversion result is in the output register. The DSP XF takes CS back to a high level and the sequence can be repeated.



NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{CS}$ setup time elapses.

Figure 3. DSP Interface Timing (16-Clock Transfer, Normal Sample Mode, $\overline{INVCLK}$=High)

3.2 Reference Voltage Inputs

The voltage difference between the REF+ and REF– terminals determines the analog input range, i.e., the upper and lower limits of the analog inputs that produce the full-scale (output data all 1s) and zero-scale (output data all 0s) readings, respectively. The absolute voltage values applied to REF+, REF–, and the analog input should not be higher than the positive supply or lower than ground. The digital output is full scale when the analog input is equal to or higher than the voltage on REF+ and is zero scale when the input signal is equal to or lower than REF–. In this application, the REF– terminal is connected to ground.

3.3 Input Data Bits

DATA IN is internally connected to a 4-bit serial input data register. The input data for the ADC are control data which select a different analog input channel or different mode of operation. The DSP provides the data word with the MSB first. Each data bit clocks in on the falling edge of the I/O CLK sequence. The software program modes are shown in Table 1.

Table 1. TLV1544/1548 Software Programmed Operation Modes

FUNCTION SELECT	INPUT DATA BYTE A3 – A0		COMMENT†
	BINARY	HEX	
Analog channel A0 for TLV1548 Selected	0000b	0h	Analog channel 0 for TLV1544 Selected
Analog channel A1 for TLV1548 Selected	0001b	1h	
Analog channel A2 for TLV1548 Selected	0010b	2h	Analog channel 1 for TLV1544 Selected
Analog channel A3 for TLV1548 Selected	0011b	3h	
Analog channel A4 for TLV1548 Selected	0100b	4h	Analog channel 2 for TLV1544 Selected
Analog channel A5 for TLV1548 Selected	0101b	5h	
Analog channel A6 for TLV1548 Selected	0110b	6h	Analog channel 3 for TLV1544 Selected
Analog channel A7 for TLV1548 Selected	0111b	7h	1001b
Software power down set	1000b	8h	No conversion result (cleared by any access)
Fast conversion rate (10 μs) set	1001b	9h	No conversion result (cleared by setting to fast)
Slow conversion rate (40 μs) set	1010b	Ah	No conversion result (cleared by setting to slow)
Self-test voltage ($V_{ref+} – V_{ref–}$)/2 selected	1011b	Bh	Output result = 200h
Self-test voltage $V_{ref–}$ selected	1100b	Ch	Output result = 000h
Self-test voltage V_{ref+} selected	1101b	Dh	Output result = 3FFh
Reserved	1110b	Eh	No conversion result
Reserved	1111b	Fh	No conversion result

†Except as noted in the Comments column, the Input Function Byte codes select the same function in the TLV1548 and the TLV1544 ADCs.

4 The ADC/DSP System

The software configures the DSP serial port to the 16-bit master mode so that the DSP generates the frame sync signal at FSX and the data clock at CLKX serial port terminals. From the hardware schematic, the connections between the DSP and the ADC are as follows.

Table 2. DSP/ADC Interconnection

FROM DSP	FROM ADC	TO DSP	TO ADC
FSX		FSR	FS
CLKX		CLKR	I/O CLK
DX			DATA IN
	DATA OUT	DR	
	EOC	$\overline{\text{INT3}}$	
XF			$\overline{\text{CS}}$

The following statements describe the generation and application of the configuration and control signals. (See Figure 1 and the TLV1544 functional block diagram).

1. The DSP CLKX output provides a 10-MHz data clock that is a divide-by-2 of the DSP master clock.
2. The DSP DX output supplies the 16-bit control to the TLV1544 at DATA IN.
3. The TLV1544 DATA OUT serial output provides the digital conversion results to the DSP DR terminal.
4. The falling edge of the frame sync signal (FSX) of the DSP serial port initiates the data transfer between the DSP and the ADC.

After the falling edge of FSX, the next 16 data clocks transfer data into the DSP DR terminal and out of the DX terminal. Since this DSP/ADC interface is synchronous, the FSX signal is sent to the FSR terminal and the CLKX is sent to the CLKR terminal.

5 The DSP Serial Port

The serial port provides direct communication with serial I/O devices and consists of six basic signals and four registers. The DSP internal serial port operation section discusses the registers.

The six signals are:

- CLKX – The serial transmit clock. This signal clocks the transmitted data from the DX terminal to the DATA IN terminal of the TLV1544.
- CLKR – The serial receive clock. This signal clocks data into the DSP DR terminal provided from the TLV1544 DATA OUT terminal.
- DX – Data transmit. From this terminal the DSP transmits 16-bit data to the DATA IN terminal of the TLV1544.
- DR – Data receive. The DSP receives 16-bit data from the DATA OUT terminal of the TLV544 into this terminal
- FSX – Frame sync transmit. This signal frames the transmit data. The DSP begins to transmit data from DX on the falling edge of FSX and continues to transmit data for the next 16 clock cycles from the CLKX terminal. The FSX signal is applied to the TLV1544 FS terminal.
- FSR – Frame sync receive, This signal frames the receive data. The DSP begins to receive data on the falling edge of FSR and continues to recognize valid data for the following 16 clocks from CLKR.

For information on the four registers, see the section, “DSP Serial Port Operation,” in Chapter 9 of the TI *TMS320C2xx User’s Guide.*

Table 3 lists the serial port pins and registers.

Table 3. DSP Serial Port Signals and Registers

PINS	DESCRIPTION	REGISTERS	DESCRIPTION
CLKX	Transmit clock signal	SSPCR	Synchronous serial port control register
CLKR	Receive clock signal	SDTR	Synchronous data transmit and receive register
DX	Transmitted serial data signal	XSR	Transmit shift register
DR	Received serial data signal	RSR	Receive shift register
FSX	Transmit frame synchronization signal		
FSR	Receive frame synchronization signal		

For this application the DSP serial port is programmed as the master, so the CLKX output is fed to the CLKR terminal and the FSX output is fed to the FSR terminal.

6 Other DSP/TLV1544 Signals

The DSP XF terminal generates the chip select signal applied to the $\overline{CS}$ terminal of the TLV1544. The TLV1544 inverted end-of-conversion (EOC) output signal drives the DSP $\overline{INT3}$ terminal. The rising edge of EOC determines the time that the current digital conversion result is available to be read by the DSP.

6.1 DSP Internal Serial Port Operation

Three signals are necessary to connect the transmit pins of the transmitting device with the receive pins of the receiving device for data transmission. The transmitted serial data signal (DX) sends the actual data. FSX initiates the transfer (at the beginning of the 16-bit packet), and CLKX clocks the bit transfer. The corresponding pins on the receive device are DR, FSR and CLKR, respectively.

Referring to Figure 4, the transmit data is written to the SDTR transmit, while received data is read from the SDTR receive. A transmit is executed by writing data to the SDTR transmit FIFO buffer, which copies the data to the XSR when the XSR is empty. The XSR manages the shifting of the data to the DX pin, thus allowing another write to SDTR transmit as soon as the SDTR-to-XSR copy is completed. On completion of the SDTR-to-XSR copy, a 0-to-1 transition occurs on the XRDY bit in the SSPCR and generates an XINT. The process is similar on the receiving end. Upon completion of the RSR-to-SDTR copy, a 0-to-1 transition occurs on the RRDY bit in the SSPCR and generates a RINT.

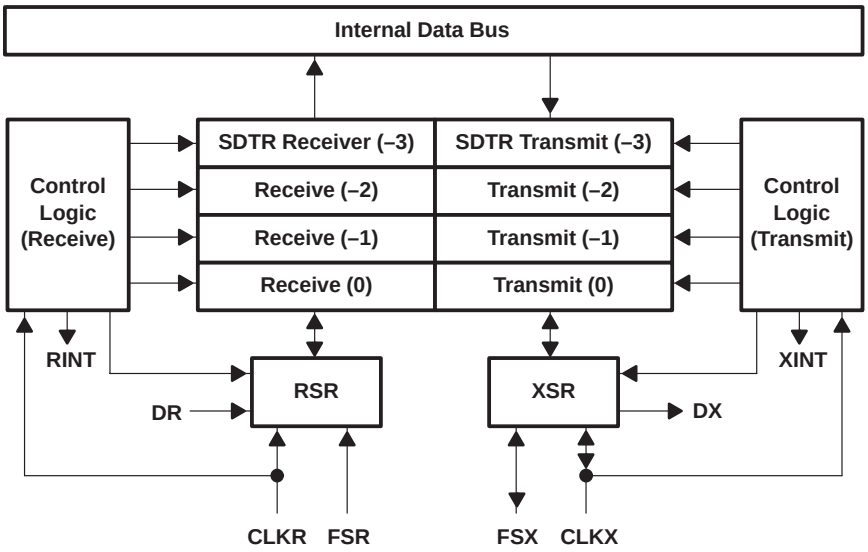


Figure 4. Internal DSP Serial Port Block Diagram

7 Software Overview

The interface program uses interrupt processing and stores 256 conversion result data-points for analog input channel A0. The CPU CLK for TMS320C203 DSP is 20 MHz (50 ns); the TLV1544 I/O CLK is driven by CLKX which is 10 MHz (100 ns).

The program starts with a common initialization procedure for the DSP followed by the initialization of the serial port.

The following steps initialize the DSP:

1. Disable the global interrupts.
2. Set the data page pointer to 0h.
3. Suppress the sign extension.

The next two steps initialize the serial port:

1. Set the synchronous serial port control register (SSPCR) to 0C00Eh.

The individual bits within the SSPCR now contain the following functions:

- The frame sync mode bit is set to 1 (FSM = 1) to allow burst mode operation.
- The clock mode bit is set to 1 (MCM = 1) to set the transmit clock CLKX to 1/2 of the DSP master clock of 20 MHz (CLKX frequency = 10 MHz)
- The transmit mode bit is set to 1 (TSM = 1) to generate the frame sync internally as required for the data transfer initiation. FSX is now programmed as an output.

2. Set the serial port control register to 0C03Eh.

- Writing 1s to the transmitter reset field (XRST) and to the receiver reset field (RRST) activates the serial port transmitter and receiver.

The following section describes the program.

8 Program Overview

This program uses two of the DSP interrupts (RINT and $\overline{\text{INT3}}$) to read and to store 256 data samples. Figure 5 shows its flowchart.

The CPU CLK for the ’C203 DSP is 20 MHz. The I/O CLK for the TLV1544 is driven by CLKX, which is 10 MHz.

The program executes the following steps:

1. Initializes the ’C203 DSP.
2. Initializes the serial port.
3. Sends the operation mode to the TLV1544 ADC for fast conversion rate.
4. Selects a specific analog input channel. This program selects input channel 0.
5. Upon the transfer of data from RSR to the receive FIFO, a RINT occurs which causes the DSP to load the content of the receive FIFO through the SDTR into ACC. The data is then shifted to the left ten times.
6. Following interrupt routine, the program initiates a low-to-high transition at the DSP XF terminal, which is connected to the ADC chip-select ($\overline{\text{CS}}$) pin, and deactivates the TLV1544. Then, it stores accumulator high word into the memory.
7. A low-to-high transition of the ADC EOC output causes, (through the inverter) a valid interrupt signal at INT3. The interupt routine then sends a high-to-low transition at the DSP XF to activate the TLV1544. The DSP then sends a frame sync and selects TLV1544 analog input channel 0.
8. Repeat steps 5 through 7 until 256 data samples are stored
9. After obtaining all data, the DSP powers the ADC down via a separate power-down routine.
10. The data is now available for use in user-defined functions (algorithms).

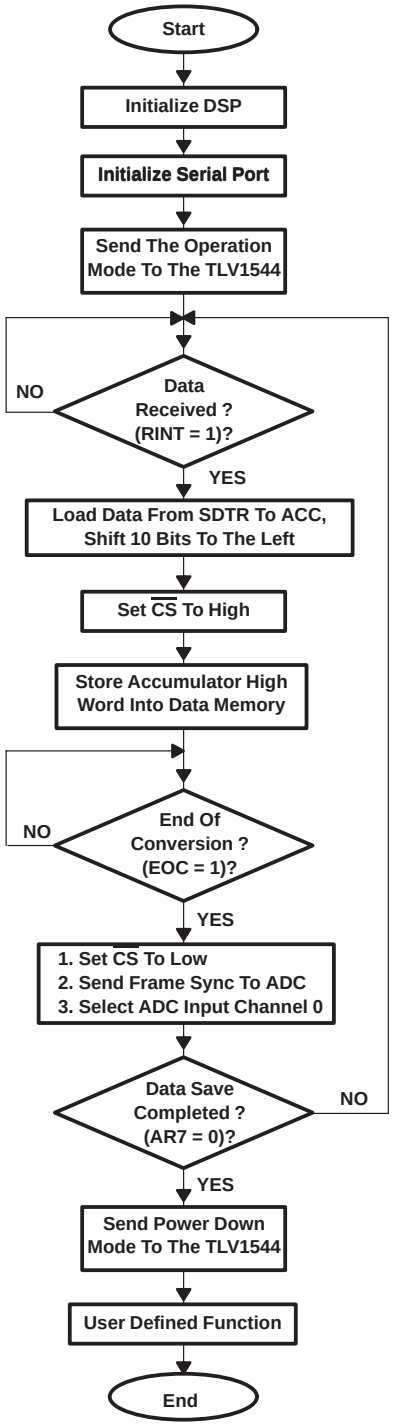


Figure 5. TLV1544 to TMS320C203 DSP Interface Program Flow Chart: Program 1

9 Program Listing

```
;*********************************************************************
;* (C) COPYRIGHT TEXAS INSTRUMENTS, INC. 1998                        *
;*********************************************************************
;*                                                                   *
;* File: 1544C203.ASM Main routine for the TLV1544-C203 Interface    *
;* Program                                                           *
;*                                                                   *
;*                                                                   *
;*********************************************************************
   .title    ”TLV1544C ADC to TMS320C203 Interface routine”
;*********************************************************************
; This routine allows the ’C203 DSP to interface with an ADC on the
;     Serial port of the DSP.
        .mmregs
ICR    .set      0ffech
SDTR   .set      0fff0h
SSPCR  .set      0fff1h
TEMP0  .set      060h          ;Transmit data
TEMP1  .set      061h          ;Receive data

       .ps       0
       B         start         ;0
       CLRC      INTM          ;2
       RET
       B         End_Conv      ;4 INT3 interrupt will jump to End_Conv
                               ;   subroutine
       CLRC      INTM          ;6
       RET
       B         Load_Data     ;8 RINT interrupt will jump to Load_Data
                               ;   subroutine

                 .data
channel_0        .set   0000h  ;TLV1544 channel 0
channel_1        .set   2000h  ;TLV1544 channel 1
channel_2        .set   4000h  ;TLV1544 channel 2
channel_3        .set   6000h  ;TLV1544 channel 3

power_down       .set   8000h  ;Software Power Down
fast_conv        .set   9000h  ;Fast Conversion Rate
slow_conv        .set   0A000h ;Slow Conversion Rate
test_200         .set   0B000h ;(Vreg+ – Vreg–)/2
test_000         .set   0C000h ;Vreg–
```

```
test_3FF        .set   0D000h ;Vreg+

num_data_0      .set   0FFh   ;Number of Data from channel 0
num_data_1      .set   0FFh   ;Number of Data from channel 1
num_data_2      .set   0FFh   ;Number of Data from channel 2
num_data_3      .set   0FFh   ;Number of Data from channel 3

data_loc_0      .set   1000h  ;Start data location for channel 0
data_loc_1      .set   1200h  ;Start data location for channel 1
data_loc_2      .set   1400h  ;Start data location for channel 2
data_loc_3      .set   1600h  ;Start data location for channel 3

                .ps    800h   ;Staring Program Address = 800h
                .text
start:
;** DSP C203 INTITIALIZATION
      SETC   INTM             ;DISABLE GLOBAL INTERRUPTS
      LDP    #0               ;SET DATA PAGE POINTER
      CLRC   SXM              ;Set sign extension mode to 0

;** SERIAL PORT INITIALIZATION
      SPLK   #0C00EH, TEMP0
      OUT    TEMP0, SSPCR     ;SET TXM=MCM=FSM=1
      SPLK   #0C03EH, TEMP0
      OUT    TEMP0, SSPCR     ;Taking Serial Port out of reset

      SPLK   #000Ah, IMR      ;Unmask RINT and INT3
      SPLK   #0002h, TEMP0    ;Select INT3
      OUT    TEMP0, ICR
      CLRC   INTM             ;Enable interrupts

;** SELECT CHANNEL, LOCATION, AND SAMPLES FOR ADC CHANNELS
      LAR    AR5,#channel_0   ;SELECT CHANNEL 0
      LAR    AR6,#data_loc_0  ;DATA LOCATION 0
      LAR    AR7,#num_data_0  ;NUMBER OF DATA 0

;** SEND OPERATION MODE TO TLV1544
      SETC   XF               ;Set CS High
      CLRC   XF               ;Send first CS Low
      SPLK   #fast_conv,TEMP0 ;Select fast conversion mode
      OUT    TEMP0, SDTR      ;Send operation mode
      IDLE                    ;wait for RINT
      SETC   XF               ;Set CS High
```

```
      SAR   AR5, TEMP0       ;TEMP0=AR5
      IDLE                   ;wait for INT3

;** REPEAT ROUTINE FOR NUM_DATA TIMES

loop:
      IDLE                   ;wait for RINT
      SETC  XF               ;Set CS High
      MAR   *,AR6            ;Select AR6
      SACH  *+,0,AR7         ;(AR6)=ACCH,*AR6+=1,select AR7
      IDLE                   ;wait for EOC
      BANZ  loop             ;IF AR7 <>0, FO TO LOOP

;** TLV1544 POWER DOWN AFTER TRANSITIONS
      SETC  XF               ;Set CS High
      CLRC  XF               ;Set CS Low
      SPLK  #power_down,TEMP0 ;Send power down mode to TLV1544
      OUT   TEMP0, SDTR

;** User Defined Function(S)
;Function:
;
;

End_Loop:
      NOP
      NOP
      NOP
      B     End_Loop

;** EOC from Low to High, INT3 active
End_Conv:
      CLRC  XF               ;Set CS Lo
      OUT   TEMP0, SDTR      ;Send operation mode (AR5) to TLV1544
      CLRC  INTM             ;Enable interrupts
      RET

;** RSR to Receive FIFO complete, RINT active
Load_Data:
      ;Load receive data from ADC
      IN    TEMP1, SDTR      ;Load data from SDTR
      LACC  TEMP1, 10        ;Store in ACC and shift ten bits to the
                             ;left
```

```
        CLRC   INTM             ;Enable interrupts
        RET

        .end
```

10 Summary

This application report demonstrates a method for bridging the analog-to-digital interface using the TLV1544 ADC and the TMS320C203 DSP.

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