- **Processed to MIL-PRF-38535**
- **Fast Instruction Cycle Time of 30 ns, 40 ns, and 50 ns**
- **Source-Code Compatible With all ’C1x and ’C2x Devices**
- **RAM-Based Operation**
  - **9K-Words × 16-Bit Dual-Access On-Chip Program/Data RAM**
  - **1056-Word × 16-Bit Dual-Access On-Chip Data RAM**
- **2K-Words × 16-Bit On-Chip Boot ROM**
- **224K-Words × 16-Bit Maximum Addressable External Memory Space (64K-Words Program, 64K-Words Data, 64K-Words I/O, and 32K-Words Global)**
- **32-Bit Arithmetic Logic Unit (ALU)**
  - **32-Bit Accumulator (ACC)**
  - **32-Bit Accumulator Buffer (ACCB)**
- **16-Bit Parallel Logic Unit (PLU)**
- **16 × 16-Bit Multiplier, 32-Bit Product**
- **Eleven Context Switch Registers**
- **Two Buffers for Circular Addressing**
- **Full-Duplex Synchronous Serial Port**
- **Time-Division Multiplexed (TDM) Serial Port**
- **Timer With Control and Counter Registers**
- **16 Software-Programmable Wait-State Generators**
- **Divide-By-1 Clock Option**
- **IEEE Standard 1149.1† (JTAG) Test-Access Port**
- **Operations are Fully Static**
- **Fabricated Using the Texas Instruments (TI™) Enhanced Performance Implanted CMOS (EPIC™) 0.72-μm Technology**
- **Military Operating Temperature Range −55°C to 125°C**

description

The SMJ320C50KGD digital signal processor (DSP) is a high-performance, 16-bit, fixed-point processor manufactured in 0.72-μm double-level metal CMOS technology.

TI’s military products currently employ three primary processes for the development of known good dies (KGDs), one of which is applied to the SMJ320C50 device. This process is called the DieMate™ system, and was developed by MicroModule Systems (MMS) and TI’s Materials and Controls Group. This system uses a membrane probe technique to make electrical contact to the individual die within special carriers. Contact is made without any disturbances to the bond pads other than typical probe markings. Following burn-in and test, the dies are simply removed from the carrier, inspected, and packed for shipment.

Future implementation of the SMJ320C50 KGD may employ the hot-chuck-probe process. This process uses standard probed product that is tested again, this time at full data sheet specifications, in wafer form at speed and elevated temperature (125°C). Each individual die is then sawed, inspected, and packaged for shipment.

A number of enhancements to the basic ’C2x architecture give the ’C50 a minimum 2x performance over the previous generation. A four-deep instruction pipeline, which incorporates delayed branching, delayed call to a subroutine, and delayed return from a subroutine, allows the ’C50 to perform instructions in fewer cycles. The addition of a PLU gives the ’C50 a method of manipulating bits in data memory without using the ACC and the ALU. The ’C50 has additional shifting and scaling capabilities for proper alignment of multiplicands or for storage of values to data memory.

† IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port and Boundary-Scan Architecture
EPIC, TI, and DieMate are trademarks of Texas Instruments Incorporated.

description (continued)

With the addition of the IDLE2 instruction, the ’C50 achieves low-power consumption. IDLE2 removes the functional clock from the internal hardware of the ’C50 that puts it into a total-sleep mode using only 5 μA. A low-logic level on an external interrupt with a chip duration of at least five clock cycles ends the IDLE2 mode.

SMJ Mil-Temp Product Flow

Multiprobe	25°C or hot chuck probe @ 125°C
Visual	100x
Test conditions	Per military data sheet
DC test	Tested to data sheet @ –55°C and 125°C
AC test	Tested to data sheet @ –55°C and 125°C @ Speed
Warranty	Data sheet upon shipment, 1 year
Certificate of Compliance	Yes
Change of notification	Yes

For electrical and timing specifications, see the *SMJ320C50x Digital Signal Processor* data sheet, (literature number SGUS020).

SPECIFIC DIE-RELATED INFORMATION

Die Size (approx.)	391 mils × 421 mils
Die Thickness	15.5 mils ± 1 mil
Backside Surface Finish	SIO2
Die Backside Potential	Floating
Max Allowable Die Junction Operating Temperature	175°C
Glassivation Material and Thickness	3KAOX / 9KACN
Recommended Packing	GEL PACK
Die Attach Information	SILVER GLASS
Suggested Bond Wire Size	1.25 AL
Suggested Bonding Method	WEDGE
ESD Sensitivity	Class II
Max Allowable Process Temperature for Die Attach	450°C

SMJ320C50 Pad Information

	PAD	XCENTER	YCENTER	PAD NAME
TOP	1	5347.4	9670.8	$\overline{IAQ}$
	2	5161.8	9670.8	$\overline{TRST}$
	3	4908.6	9670.8	V_{SS1}
	4	4773.6	9670.8	V_{SS2}
	5	4573.4	9670.8	MP/$\overline{MC}$
	6	4139.3	9670.8	D15
	7	3851.3	9670.8	D14
	8	3515.3	9670.8	D13
	9	3272.3	9670.8	D12
	10	3024.8	9670.8	D11
	11	2777.3	9670.8	D10
	12	2421.0	9670.8	D9
	13	2121.1	9670.8	D8
	14	1702.6	9670.8	V_{DD1}
	15	1567.6	9670.8	V_{DD2}
LEFT	16	106.3	8552.8	V_{SS3}
	17	106.3	8417.8	V_{SS4}
	18	106.3	7859.8	D7
	19	106.3	7616.8	D6
	20	106.3	7321.3	D5
	21	106.3	7096.3	D4
	22	106.3	6871.3	D3
	23	106.3	6646.3	D2
	24	106.3	6323.9	D1
	25	106.3	6098.9	D0
	26	106.3	5818.7	TMS
	27	106.3	5498.0	V_{DD3}
	28	106.3	5363.0	V_{DD4}
	29	106.3	4942.2	TCK
	30	106.3	4764.3	NC
	31	106.3	4601.2	V_{SS5}
	32	106.3	4466.2	V_{SS6}
	33	106.3	4041.0	$\overline{INT1}$
	34	106.3	3789.2	$\overline{INT2}$
	35	106.3	3537.4	$\overline{INT3}$
	36	106.3	3201.4	$\overline{INT4}$
	37	106.3	2949.6	$\overline{NMI}$
	38	106.3	2697.8	DR
	39	106.3	2445.9	TDR
	40	106.3	2035.1	FSR

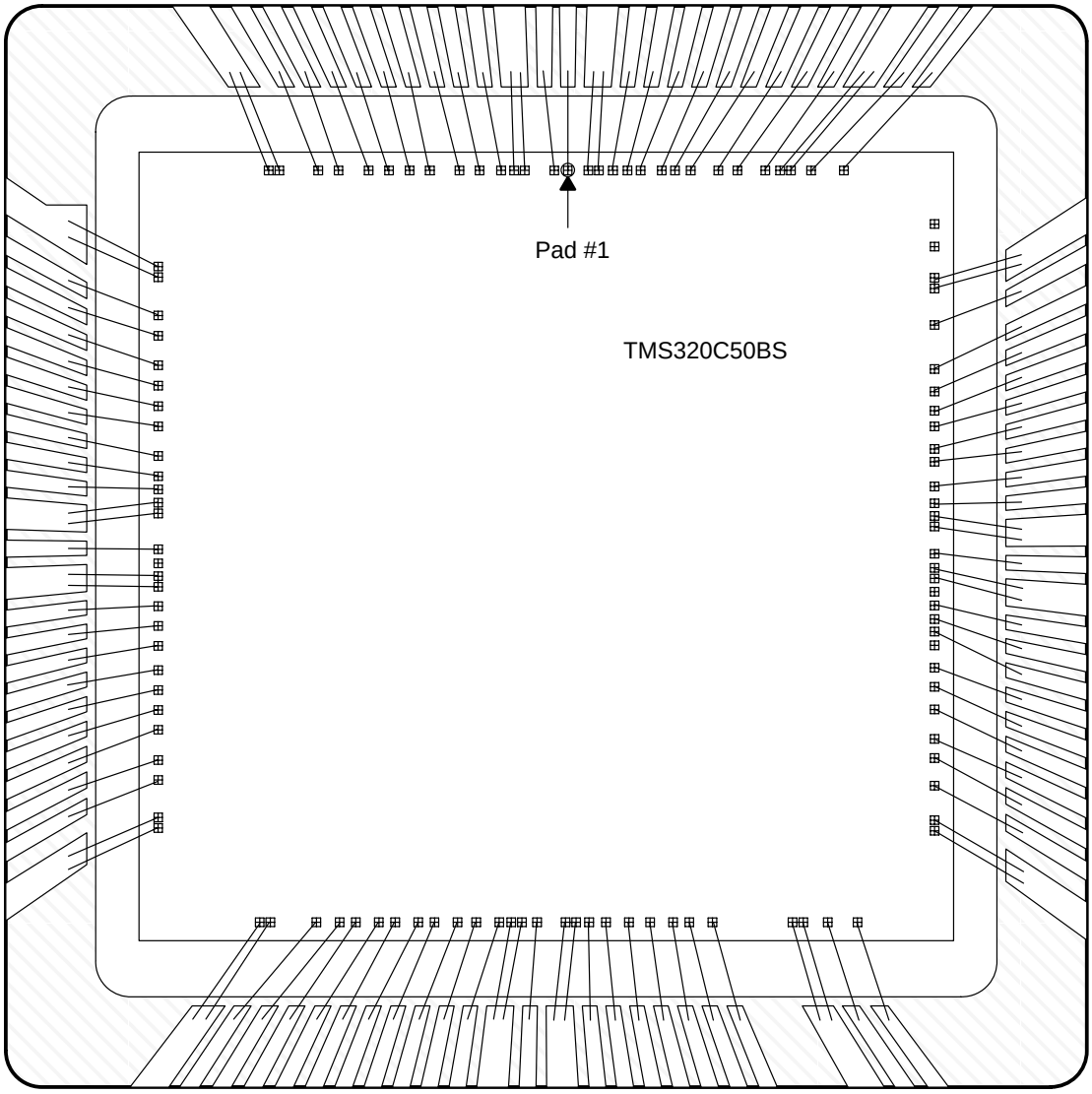
	PAD	XCENTER	YCENTER	PAD NAME
	41	106.3	1783.3	CLK
	42	106.3	1353.6	V_{DD5}
	43	106.3	1218.6	V_{DD6}
BOTTOM	44	1513.4	106.3	V_{SS7}
	45	1648.4	106.3	V_{SS8}
	46	2128.3	106.3	A0
	47	2403.3	106.3	A1
	48	2637.3	106.3	A2
	49	2912.2	106.3	A3
	50	3132.7	106.3	A4
	51	3407.7	106.3	A5
	52	3628.2	106.3	A6
	53	3903.1	106.3	A7
	54	4123.6	106.3	A8
	55	4398.6	106.3	A9
	56	4569.6	106.3	V_{DD7}
	57	4704.6	106.3	V_{DD8}
	58	4896.7	106.3	TDI
	59	5319.6	106.3	V_{SS9}
	60	5454.8	106.3	V_{SS10}
	61	5646.0	106.3	CLKMD1
	62	5886.6	106.3	A10
	63	6161.6	106.3	A11
	64	6527.3	106.3	A12
	65	6802.3	106.3	A13
	66	7036.3	106.3	A14
	67	7311.2	106.3	A15
	68	8202.2	106.3	V_{DD9}
	69	8337.2	106.3	V_{DD10}
	70	8649.0	106.3	$\overline{RD}$
	71	9195.5	106.3	$\overline{WE}$
RIGHT	72	10274.3	1253.8	V_{SS11}
	73	10274.3	1388.8	V_{SS12}
	74	10274.3	1902.0	$\overline{DS}$
	75	10274.3	2236.6	$\overline{IS}$
	76	10274.3	2524.8	$\overline{PS}$
	77	10274.3	2882.6	R/$\overline{W}$
	78	10274.3	3168.8	$\overline{STRB}$
	79	10274.3	3365.0	$\overline{BR}$
	80	10274.3	3625.7	NC

SMJ320C50 Pad Information (Continued)

	PAD	XCENTER	YCENTER	PAD NAME
	81	10274.3	3795.5	CLKIN2
	82	10274.3	3950.6	X2/CLKIN
	83	10274.3	4126.6	X1
	84	10274.3	4296.2	NC
	85	10274.3	4459.4	V_{DD11}
	86	10274.3	4594.4	V_{DD12}
	87	10274.3	4766.7	TDO
	88	10274.3	5085.1	V_{SS13}
	89	10274.3	5220.1	V_{SS14}
	90	10274.3	5375.3	CLKMD2
	91	10274.3	5579.4	FSX
	92	10274.3	5866.1	TFSX/TFRM
	93	10274.3	6086.8	DX
	94	10274.3	6379.1	TDX
	95	10274.3	6599.8	$\overline{\text{HOLDA}}$
	96	10274.3	6820.5	XF
	97	10274.3	7180.3	CLKOUT1
	98	10274.3	7558.5	$\overline{\text{IACK}}$
	99	10274.3	8089.5	V_{DD13}
	100	10274.3	8224.5	V_{DD14}
	101	10274.3	8724.3	NC
	102	10274.3	8859.3	NC
TOP-R	103	9201.4	9670.8	EMU0
	104	8796.6	9670.8	EMU1/$\overline{\text{OFF}}$
	105	8540.1	9670.8	V_{SS15}
	106	8405.1	9670.8	V_{SS16}
	107	7927.9	9670.8	TOUT
	108	7690.0	9670.8	TCLKX
	109	7456.5	9670.8	CLKX
	110	7133.8	9670.8	TFSR/TADD
	111	6956.1	9670.8	TCLKR
	112	6771.8	9670.8	$\overline{\text{RS}}$
	113	6587.5	9670.8	READY
	114	6403.1	9670.8	$\overline{\text{HOLD}}$
	115	6016.9	9670.8	$\overline{\text{BIO}}$
	116	5780.7	9670.8	V_{DD15}
	117	5645.7	9670.8	V_{DD16}

MECHANICAL DATA

MOUNT AND BOND



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