- **Single-Chip Digital NTSC/PAL Encoder**
- **Master Clock 27 MHz, 28.6 MHz**
- **YCbCr or RGB Selectable Input**
- **Y, C, Composite or RGB Selectable Output**
- **16-Color Overlay With Color Lookup Table**
- **Line 21 Closed Caption Data Encoding**
- **Video Attribute Insertion Capability**
- **Macrovision® Anticopy Protection for Digital Video Disk (DVD) Applications ('AV410 Only)**
- **Supports PAL B, D, G/H and I Formats**
- **Support for Interlace/Non-Interlace Scan**
- **9-Bit Over-Sampling D/A Converter**
- **100-Pin Plastic Quad Flatpack (PQFP) Package**

description

The TMS320AV410/411 digital NTSC/PAL encoder converts digital RGB and YCbCr signals to conform to the NTSC/PAL standard. Signals may be output in Y, C, composite, and RGB formats. The integrated synchronization signal generator and three-channel D/A converter minimize the requirement for additional external logic. An internal matrix circuit performs YCbCr to RGB conversion. The 'AV410/411 is designed for MPEG video applications such as DVD, video CD, CATV set-top box, and PC applications. Host control of the 'AV410/411 is achieved via an I^2C compatible interface or a general purpose four-line host interface. A simplified stand-alone mode allows the 'AV410/411 to operate without a host controller. The device uses a dual supply configuration for reduced power dissipation. The core circuitry operates at 3.3-V while the device input/output operates at 5-V to provide a TTL-compatible interface.

The TMS320AV410 complies with the Macrovision (version 7.01) requirements for DVD applications. The Macrovision anti-taping process is applied to Y, C, and composite outputs. The 'AV410 does not support Macrovision on RGB outputs. In order to obtain this device and the associated Macrovision programming information, the customer must provide proof of Macrovision licensing. Please contact your nearest Texas Instruments (TI™) sales representative for more information.†

The TMS320AV411 is identical in functionality to the TMS320AV410 without the Macrovision function.

The TMS320AV410 and the TMS320AV411 are characterized for operation from –10°C to 70°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† This device is protected by U.S. patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. Use of the Macrovision anticopy process in the device is licensed by Macrovision for non-commercial home use only. Reverse engineering or disassembly is prohibited.

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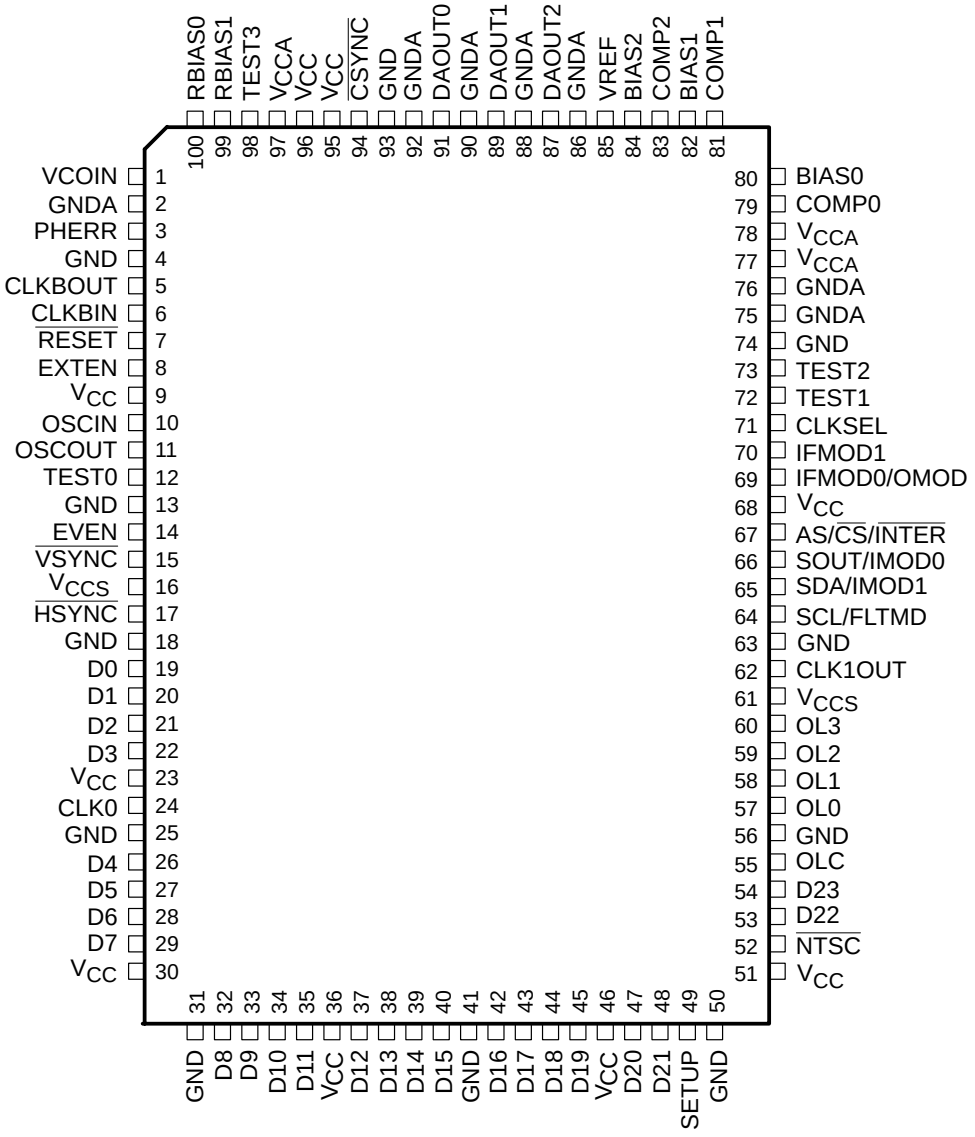
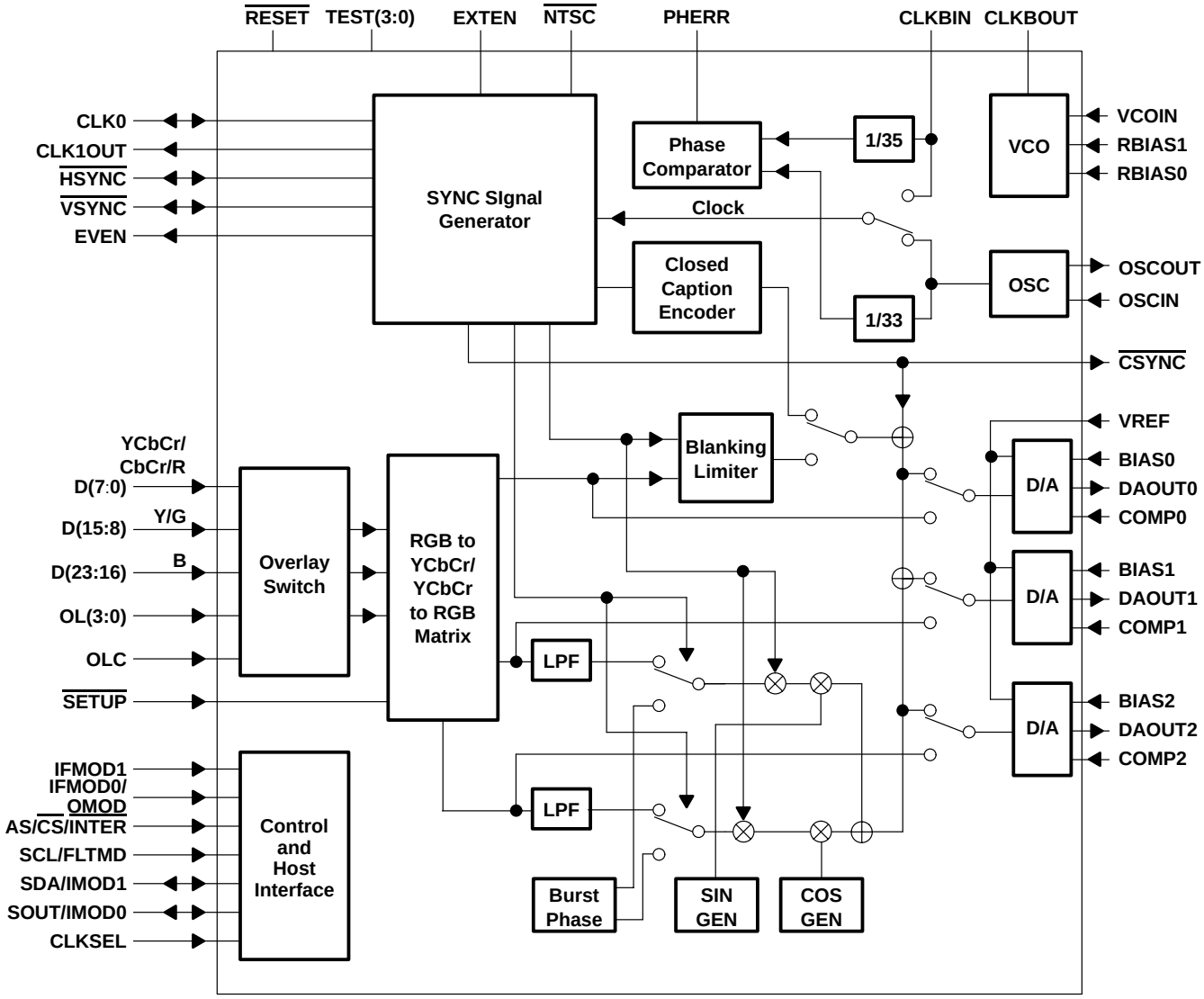
TI is a trademark of Texas Instruments Incorporated.

PJM PACKAGE
(TOP VIEW)



block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AS	67	I	When IFMOD1 is low and IFMOD0 is low (I^2C host interface mode), AS operates as the I^2C slave address select input. When AS is low, the 'AV410/411 I^2C slave address is 88h. When AS is high, the slave address is 8Ch.
BIAS0	80	I	DAC0 bias terminal
BIAS1	82		DAC1 bias terminal
BIAS2	84		DAC2 bias terminal
CLK0	24	I/O	When EXTEN is low, CLK0 is the clock output used to clock pixel data out from the system video decoder device. Typically, CLK0 outputs at 27 MHz or 28.6 MHz, as determined by the settings of the OSCIN and CLKBIN pins and the setting of the CLKSEL pin or the CLKSEL 1:0 register bit values. When EXTEN is high, CLK0 is the external clock input.
CLKBIN	6	I	Secondary system clock input for a dual clock system. In a dual clock system, CLKBIN has a 28.6-MHz clock source as its input. This clock source may originate external to the 'AV410/411 or may be obtained from the 'AV410/411 internal phase-locked loop (PLL). When using the internal PLL, CLKBIN should be tied to the CLKBOUT terminal. For a single-clock system, CLKBIN should be tied low.
CLKBOUT	5	O	Internal PLL clock output terminal. CLKBOUT should be tied to CLKBIN when using the internal PLL to generate the 28.6-MHz system clock. This function is not available in stand-alone mode.
CLK1OUT	62	O	Alternate pixel clock output which clocks at one-half the system clock frequency. CLK1OUT clock frequency is either 13.5 MHz or 14.3 MHz.
CLKSEL	71	I	When IFMOD1 is high (stand-alone mode), CLKSEL selects the expected system clock frequency for the 'AV410/411. If CLKSEL is low, system clock frequency is 27 MHz; if CLKSEL is high, frequency is 28.6 MHz. When IFMOD1 is low, CLKSEL should be tied low.
COMP0	79	I	DAC0 compensation capacitor
COMP1	81		DAC1 compensation capacitor
COMP2	83		DAC2 compensation capacitor
$\overline{CS}$	67	I	Chip select for the simple serial host interface mode (IFMOD1 low and IFMOD0 high).
$\overline{CSYNC}$	94	O	Composite sync output, active low

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23	19 20 21 22 26 27 28 29 32 33 34 35 37 38 39 40 42 43 44 45 47 48 53 54	I	Video data input IMODE1,0 = 0,0 : D[7:0] – YCbCr input IMODE1,0 = 0,1 : D[7:0] – CbCr input D[15:8] – Y input IMODE1,0 = 1,0 : RGB input mode 0 D[7:0] – R input, input range 1† D[15:8] – G input, input range 1† D[23:16] – B input, input range 1† IMODE1,0 = 1,1 : RGB input mode 1 D[7:0] – R input, input range 2‡ D[15:8] – G input, input range 2‡ D[23:16] – B input, input range 2‡ Unused inputs should be tied low. † Input range 1 = Black level = 16, white 100% level = 235 ‡ Input range 2 = Black level = 0, white 100% level = 240
DAOUT0	91	O	Y or R video output signal
DAOUT1	89	O	Composite or G video output signal
DAOUT2	87	O	C or B video output signal
EVEN	14	O	Field ID output for interlaced scan mode. A low indicates odd field. High indicates even field.
EXTEN	8	I	External/internal sync mode select. A low indicates internal sync mode where the ’AV410/411 accepts the system clock from the OSCIN or CLKBIN inputs and has CLK0, $\overline{\text{HYSNC}}$, and $\overline{\text{VSYNC}}$ as outputs. A high on EXTEN activates external sync mode where CLK0, $\overline{\text{HSYNC}}$, and $\overline{\text{VSYNC}}$ are expected inputs to the ’AV410/411.
FLTMD	64	I	When IFMOD1 is high (stand-alone mode), FLTMD is the color signal cutoff frequency select. If FLTMD is low, cutoff frequency is 1.5 MHz. If FLTMD is high, cutoff is 3 MHz.
GND	4, 13, 18, 25, 31, 41, 50, 56, 63, 74, 93	I	Digital ground
GNDA	2, 75, 76, 86, 88, 90, 92	I	Analog ground
$\overline{\text{HSYNC}}$	17	I/O	Horizontal sync pulse. When EXTEN is low, $\overline{\text{HSYNC}}$ is an output. When EXTEN is high, $\overline{\text{HSYNC}}$ is expected as an input to the device.
IFMOD0	69	I	When IFMOD1 is low, IFMOD0 selects between the I^2C and the simple serial host interface mode. A low on IFMOD0 selects I^2C mode. A high selects the simple serial host interface mode.
IFMOD1	70	I	Selects between ’AV410/411 serial host interface modes (I^2C and simple serial) and the stand-alone (non-host) control mode. A low selects serial host interface mode. A high selects stand-alone mode.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
IMOD0 IMOD1	66, 65	I	When IFMOD1 is high (stand-alone mode), IMOD1:0 selects the desired format for video input to the 'AV410. Refer to the description for D23:0 pins.
$\overline{\text{INTER}}$	67		When IFMOD1 is high (stand-alone mode), $\overline{\text{INTER}}$ selects between interlaced and non-interlaced display. Low selects interlaced mode. High selects non-interlaced mode.
$\overline{\text{NTSC}}$	52	I	PAL/NTSC mode select L : NTSC H : PAL
OL0 OL1 OL2 OL3	57 58 59 60	I	Overlay color select input. When the 'AV410/411 operates in stand-alone mode, OL3:0 selects the overlay color from the preset color choices listed in Table 1. In I^2C or simple serial host interface mode, OL3:0 selects the overlay color from the color choices that have been programmed by the user in the overlay color registers.
OLC	55	I	Overlay switching select L : Output video signal H : Output overlay signal
OMOD	69		When IFMOD1 is high (stand-alone mode), OMOD selects the output mode. A low on OMOD selects, Y, C, composite output. A high selects RGB output.
OSCIN	10	I	External oscillator input or crystal connection
OSCOUT	11	O	Crystal connection (crystal low side)
PHERR	3	O	Phase comparator output. PHERR is input to VCOIN when using the internal PLL to generate the system clock.
RBIAS0	100		VCO bias resistor 1
RBIAS1	99		VCO bias resistor 2
$\overline{\text{RESET}}$	7	I	Reset input, active low. A reset action sets all registers to default values. $\overline{\text{RESET}}$ should be toggled once following device powerup.
SCL	64	I	When IFMOD1 is low (serial host interface modes), SCL is the serial clock input.
SDA	65	I/O	In I^2C interface mode, SDA is the serial data input/output (open drain). In simple serial interface mode, SDA is the serial data input.
$\overline{\text{SETUP}}$	49	I	In NTSC mode, setup level select: L : 0% setup H : 7.5% setup
SOUT	66	I/O	In simple serial host interface mode, device status is output on SOUT. SOUT is unused in I^2C mode and should be tied low.
TEST0 TEST1 TEST2	12 72 73	I	Device test terminals. Connect to GND for normal operation.
TEST3	98	O	PLL test terminal. Should remain floating.
V_{CC}	9, 23, 30, 36, 46, 51, 68, 95, 96	I	3.3-V supply voltage
V_{CCA}	77, 78, 97	I	5-V analog supply voltage
V_{CCS}	16, 61	I	5-V supply voltage
VCOIN	1	I	VCO control voltage input. VCOIN is input from the PHERR terminal when using the internal PLL to generate the system clock.
VREF	85	I	DAC reference voltage input
$\overline{\text{VSYNC}}$	15	I/O	Vertical sync pulse. When EXTEN is low, $\overline{\text{VSYNC}}$ is an output. When EXTEN is high, $\overline{\text{VSYNC}}$ is expected as an input to the device.

input format

The ‘AV410/411 accepts digital input signals in RGB or YCbCr formats. For YCbCr format, the user may select between two different modes. A multiplexed 8-bit YCbCr mode is available (similar to CCIR 656), as well as a multiplexed 16-bit YCbCr mode. Video and overlay signals are input subject to the timing conditions illustrated in Figure 15 and Figure 16.

IMOD0 determines the manner in which input signal levels are processed. When IMOD0 is 0, a value of 16 is processed as black level, and a value of 235 is processed as 100% white level. When IMOD0 is 1, a value of 0 is processed as black level, and a value of 240 is processed as 100% white level. Both cases are shown in Figure 1.

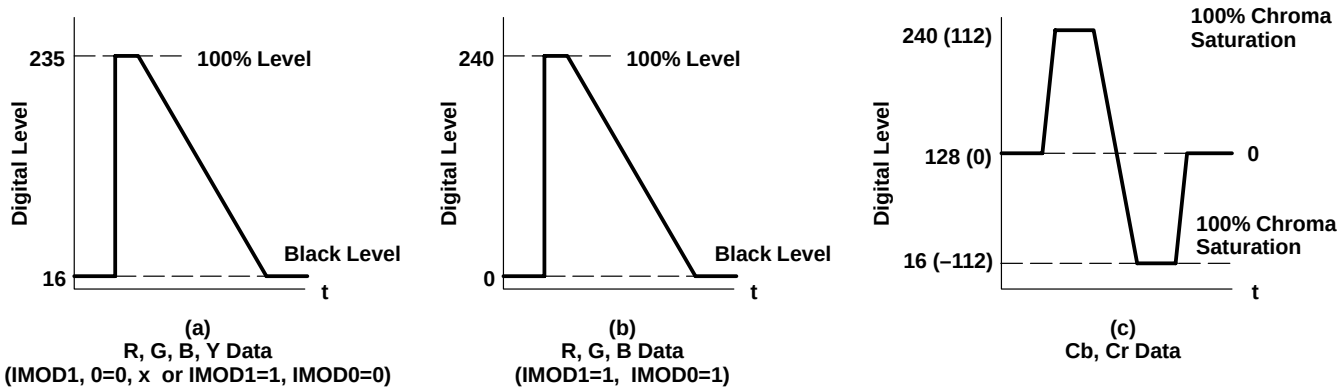


Figure 1. Input Video Data

color signal cutoff frequency select

When output is YC composite, the chroma signal is restricted to the frequency band by the low-pass filter. On the ’AV410/411, cutoff frequency is selected using the FLTMD pin or the FLTMD bit in the VID0 register. When FLTMD is set to L, cutoff frequency is 1.5 MHz; when FLTMD is set to H, cutoff frequency is 3 MHz.

internal/external synchronization

When the EXTEN pin is low, the ’AV410/411 operates in internal synchronization mode. The system clock must be input to OSCIN or CLKBIN. The $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ terminals are outputs. CLK0 will output a 27-MHz or 28.6-MHz clock. When EXTEN is high, the ’AV410/411 operates in external synchronization mode. In this mode $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and CLK0 are inputs. In external synchronization mode, $\overline{\text{HSYNC}}$ is active for the falling edge of the input signal, and $\overline{\text{VSYNC}}$ is active for the rising edge. The EVEN and $\overline{\text{CSYNC}}$ signals are output for internal and external synchronization modes. EVEN is the field signal where a low level indicates odd-field and a high level indicates even-field. Figure 21 shows the relationship between EVEN and the video output signals for NTSC and PAL.

’AV410/411 clock arrangements

The ’AV410/411 has various clock modes available. Choice of the particular mode depends upon the clocking schemes and host interface available in the system.

single-clock system

Figure 2 shows the configuration for the single-clock (27 or 28.6 MHz) system. The internal synchronization mode is also active for the ’AV410/411. Selection of clock frequency must be identified using the CLKSEL pin (stand-alone mode) or the CLKSEL0 bit in the VID1 register (simple serial or I^2C host interface modes).

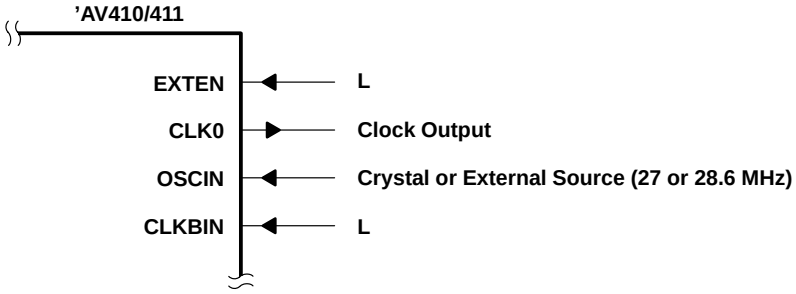


Figure 2. Single-Clock System

dual clock system without internal PLL

Figure 3 shows the configuration for the dual clock (27 and 28.6 MHz) system. The internal synchronization mode is also active for the ’AV410/411, but the internal PLL is not active. Selection between the two clocks is made by entering 00 or 11 to the CLKSEL1:0 bits in the VID1 register. This configuration is not available when using the stand-alone mode.

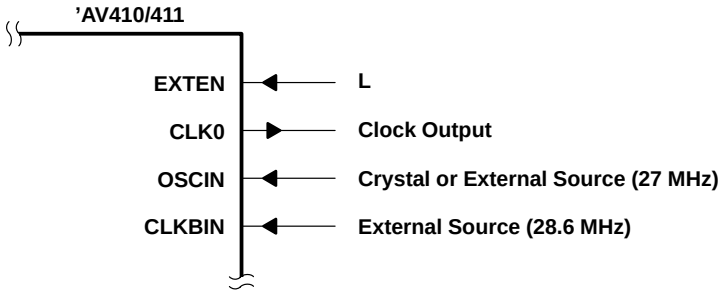


Figure 3. Dual Clock System Without PLL

dual clock system using internal PLL

Figure 4 shows the configuration for the dual clock system using the internal PLL. The internal synchronization mode of the ’AV410/411 is active. To enable the ’AV410/411 for a 28.6-MHz clock, first enable the PLL via the PLLEN control bit, then enter the proper selection to the CLKSEL1:0 bits. To select the 27-MHz clock, enter the proper value for the CLKSEL1:0 bits, then disable the PLL via the PLLEN control bit. This configuration is not available in stand-alone mode.

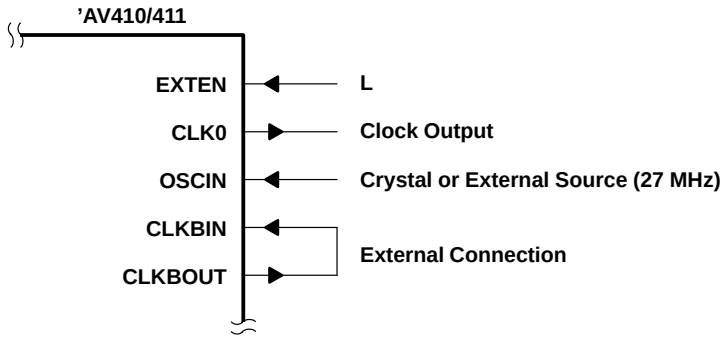


Figure 4. Dual Clock System Using Internal PLL

external synchronization mode

Figure 5 shows the configuration for the ’AV410/411 operating in external synchronization mode. CLK0 is an input to the device in this arrangement. Note that $\overline{\text{VSYNC}}$ and $\overline{\text{HSYNC}}$ are also required inputs in this mode.

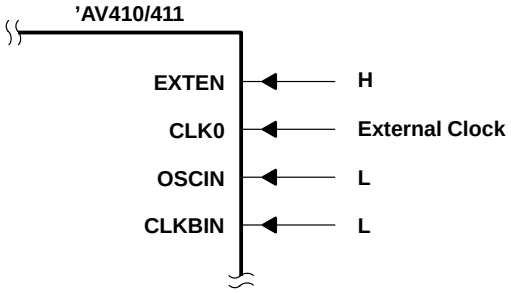


Figure 5. External Synchronization Mode

video bus interface

Figure 6 and Figure 7 show video bus connections. Figure 6 shows connections to the TMS320AV220. Figure 7 shows connections to a general MPEG-2 video decoder. Because the connections shown in Figure 7 use two ’AV410 devices, composite, YC, and RGB signals can be obtained simultaneously.

video attribute insertion

The ’AV410/411 has capability to insert video information into the vertical blanking period. For example, the ’AV410/411 can insert a video attribute which indicates the proper aspect ratio to the video receiver. For NTSC mode, the ’AV410/411 can insert 14-bit video information on line 20 of every field to conform to the EIAJ CPX-1024 Video Aspect Ratio ID specification. Attribute information should be set using the ATR1 and ATR0 registers. The ATR2 register (bits 5:0) should be set with the 6-bit CRC data that is calculated by the following equation:

$$G(X) = X^6 + X + 1$$

where

X^6, X are preset to 1

Bit 7 of the ATR2 register enables attribute insertion.

For PAL mode, the ’AV410/411 can insert 14-bit video information on line 20 of every frame to conform to the ETS 300-294 Wide Screen Signaling specification. Attribute information should be set in the ATR1 register and bits 5:0 of the ATR2 register. Bit 7 of the ATR2 register enables attribute insertion.

In NTSC and PAL encoding modes, data in the ATR1 and ATR0 registers are transferred to internal circuitry when the ATR2 register is set. For this reason, the ATR2 register should be set last.

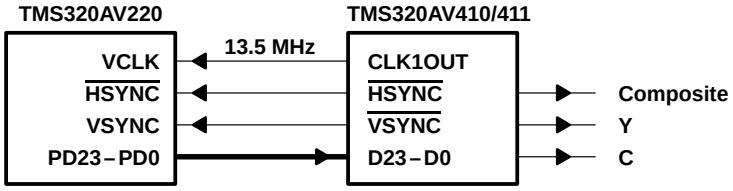


Figure 6. Interface to TMS320AV220

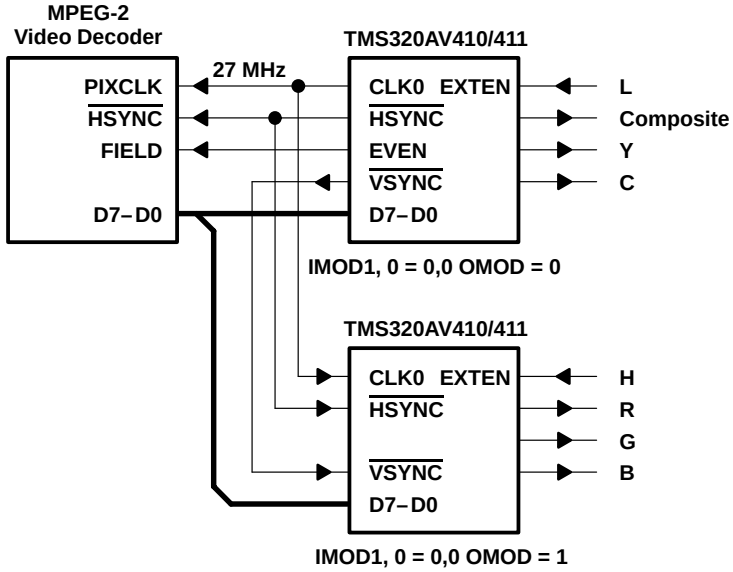


Figure 7. Interface to MPEG-2 Video Decoder

control modes

The ’AV410/411 has three control modes: stand-alone mode, simple serial host interface mode, and the I^2C serial host interface mode (slave mode only). Figure 8 illustrates the three control modes.

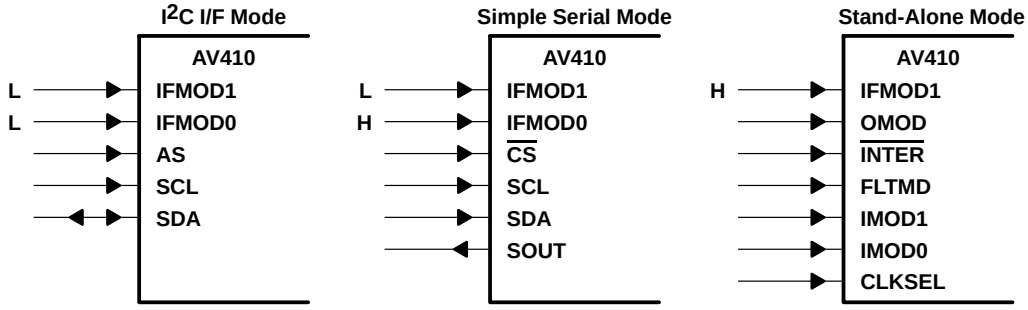


Figure 8. Control Modes

stand-alone mode

When the IFMOD1 pin is high, the ’AV410/411 operates in stand-alone mode. The input mode, output mode, scan mode select, and color filter mode select functions are controlled by pin settings rather than internal registers. In this mode, the closed caption encode, color bar generation, overlay lookup table, and attribute data insertion functions are disabled. In stand-alone mode, overlay displays the preset colors shown in Table 1.

Table 1. Overlay Colors in Stand-Alone Mode

OL[3:0]	OVERLAY COLOR
0000	black
0001	dark blue
0010	dark red
0011	dark magenta
0100	dark green
0101	dark cyan
0110	dark yellow
0111	gray

OL[3:0]	OVERLAY COLOR
1000	black
1001	blue
1010	red
1011	magenta
1100	green
1101	cyan
1110	yellow
1111	white

simple serial host interface mode

When IFMOD1 is low and IFMOD0 is high, the ’AV410/411 operates in simple serial host interface mode. In this mode, data transfer is executed via a four-line interface. A chip select ($\overline{CS}$), serial data input (SDA), serial data output (SOUT), and serial clock (SCL) are used to write data and read status from the device registers. Data transfers are always most significant bit first. Figure 9 illustrates the read/write operation in simple serial host interface mode.

A write is executed by first pulling $\overline{CS}$ low. After the falling edge of $\overline{CS}$, the first eight bits entered on SDA should be the address of the first register to write. Next the data is entered on SDA. The ’AV410/411 address pointer is automatically incremented to allow successive data register writes as long as $\overline{CS}$ remains low. The status data byte is read out on the SOUT pin simultaneous with each byte written to the ’AV410/411. To obtain status data without performing a write, the host should perform a dummy write cycle to address 0xFF after pulling $\overline{CS}$ low. Note that the first four bits of the status byte are always zero. See Table 2 for a description of status output.

When operating in the simple serial host interface mode, the ’AV410/411 overlay function uses the colors set in the lookup table. When using the overlay function, the user must set these colors (via the YG, B, and R registers) at least once after powerup.

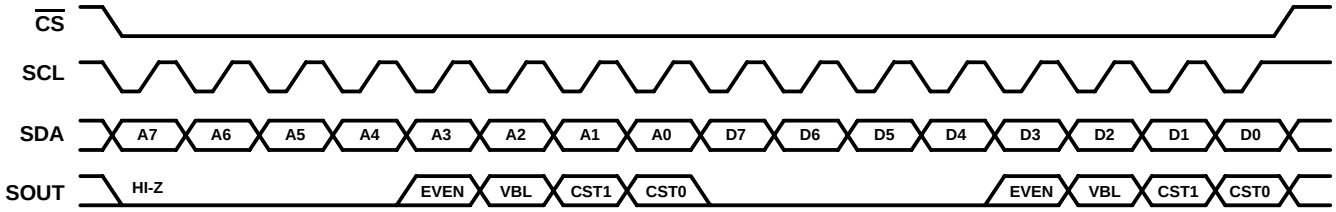


Figure 9. Simple Serial Mode Read/Write

Table 2. Status Data Bit Descriptions

BIT LOCATION	DESCRIPTION	FUNCTION
7:4	Unused	Always 0
3	Non-interlace scan field status	1 = Even field 0 = Odd field
2	Vertical blanking indicator	1 = Blanking line 0 = Active video line
1	Caption data status 1	1 = Second caption data field not available for write 0 = Second caption data field available for write
0	Caption data status 0	1 = First caption data field not available for write 0 = First caption data field available for write

I²C host interface mode

When the IFMOD1 and IFMOD0 pins are both low, the ’AV410/411 operates in the I²C compatible host interface mode. The ’AV410/411 performs read and write operations according to the I²C specification and functions as a slave-mode only device. The slave address may be selected from among two values, depending upon the level of the AS pin. When AS is set low, the ‘AV410/411 I²C address is 0x88h. When AS is set high, the address is 0x8Ch. When operating in the I²C host interface mode, the ’AV410/411 overlay function uses the colors set in the lookup table. These colors must be set (via the YG, B, and R registers) at least once after powerup when the overlay function is used.

I²C write

The I²C write is executed by sending (on SDA) the 7-bit slave address and write bit in the first byte following the I²C start condition. After the acknowledge, the second byte entered specifies the beginning address for the write. The data to write follows on successive bytes. The auto-increment function of the ’AV410/411 address pointer allows consecutive data bytes to be entered until the I²C stop condition is received. Figure 10 illustrates the I²C write operation.

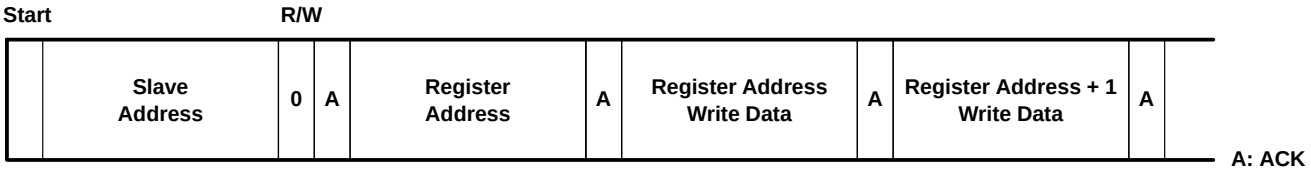


Figure 10. I²C Data Write

I²C read

To read the status byte from the ’AV410/411, enter (on SDA) the 7-bit slave address followed by the read bit. After the acknowledge, the next eight bits clocked out on SDA are the status byte. The first four bits of status are always zero. See Table 2 for a description of status output. Figure 11 illustrates the I²C read operation.

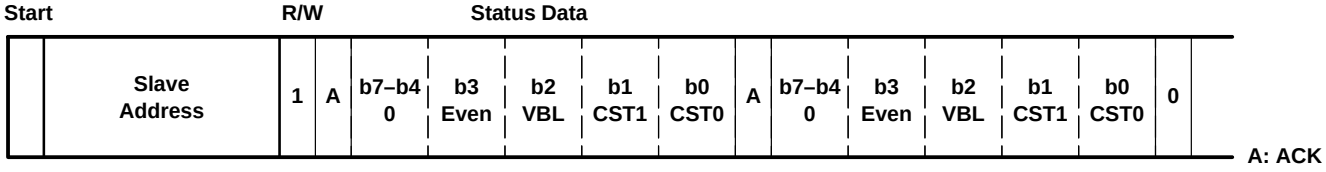


Figure 11. I²C Status Data Read

control register

register address

ADDRESS [HEX]	REGISTERS
00	VID0
01	VID1
02	CCE
03	CAPT0
04	CAPT1
05	CAPT2
06	CAPT3
07	VID2
08	YG0
09	B0
0A	R0
0C	YG1
0D	B1
0E	R1
10	YG2
11	B2
12	R2
14	YG3
15	B3
16	R3
18	YG4
19	B4
1A	R4
1B	YG5
1C	B5
1E	R5
20	YG6
22	B6
22	R6
24	YG7
25	B7
26	R7

ADDRESS [HEX]	REGISTER
28	YG8
29	B8
2A	R8
2C	YG9
2D	B9
2E	R9
30	YG10
31	B10
32	R10
34	YG11
35	B11
36	R11
38	YG12
39	B12
3A	R12
3C	YG13
3D	B13
3E	R13
40	YG14
41	B14
42	R14
44	YG15
45	B15
46	R15
48	ATR0
49	ATR1
4A	ATR2

00H VID0: video mode register0

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BLNK	OMOD	$\overline{\text{INTER}}$	FLTMD	CBAR1	CBAR0	IMOD1	IMOD0

BLNK: Blanking enable
0 : Normal operation (default)
1 : Forced blanking
When writing a one to this bit, video outputs will be blanked without regard to input video signals or input overlay signals. Synchronization signal and color burst are output in this mode.

OMOD: Output mode
0 : Y, C, composite output (default)
1 : RGB output

$\overline{\text{INTER}}$: Scan mode select
0 : Interlace (default)
1 : Non-interlace

FLTMOD: Chroma low-pass filter mode select
0 : Cutoff frequency 1.5 MHz (default)
1 : Cutoff frequency 3 MHz

CBAR1: Color bars enable
Selects enable/disable of color bars generator
0 : Outputs video signals input (default)
1 : Outputs built-in color bars signal

CBAR0: Color bars type select
Selects color bars type
0 : 75% color bars
1 : 100% color bars

IMOD1, IMOD0: Input mode select

IMOD1, 0 = 0, 0 : YCbCr 8-bit input mode (default)
D[7:0] – YCbCr input

IMOD1, 0 = 0, 1: YCbCr 16-bit input mode
D[7:0] – CbCr input
D[15:8] – Y input

IMOD1, 0 = 1, 0: RGB input mode 0
D[7:0] – R input (Black level = 16, 100% level = 235)
D[15:8] – G input (Black level = 16, 100% level = 235)
D[23:16] – B input (Black level = 16, 100% level = 235)

IMOD1, 0 = 1, 1: RGB input mode 1
D[7:0] – R input (Black level = 0, 100% level = 240)
D[15:8] – G input (Black level = 0, 100% level = 240)
D[23:16] – B input (Black level = 0, 100% level = 240)

01H VID1: video mode register1

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
IPMD	0	0	VBLDIS	HBLDIS	PLLEN	CLKSEL1	CLKSEL0

NOTE: Bit6 – bit5 must be set to 0.

IPMD: Interpolation mode
0 : Interpolation disable (default)
1 : Interpolate Y and RGB signals by 27 or 28.6 MHz up-sampling

VBLDIS: Disable internal vertical blanking
0 : Enable internal vertical blanking (default)
1 : Disable internal vertical blanking after the equalization pulse

HBLDIS: Disable internal horizontal blanking
0 : Enable internal horizontal blanking (default)
1 : Disable internal horizontal blanking except for sync period

PLLEN: Selects enable/disable of PLL circuit
0 : PLL disable (default)
1 : PLL enable

CLKSEL0: Selects system clock when in NTSC mode
0 : 27 MHz (default)
1 : 28.6 MHz
Don’t care when in PAL mode

CLKSEL1: Clock select input. Selects system clock as input from OSCIN or CLKBIN. To execute the selection, clock must be active to OSCIN and/or CLKBIN prior to selection.
0 : Use clock of OSCIN (default).
1 : Use clock of CLKBIN.

If the internal PLL is disabled and the user wishes to switch from OSCIN to the clock generated by the internal PLL, PLLEN (bit 2) must first be enabled. Once frequency is locked, CLKSEL1 and CLKSEL0 may be modified to switch the clock selection.

07H VID2: video mode register2

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	0	ADJ1	ADJ0

ADJ1: Input phase adjust1
0 : No phase adjust (default)
1 : Invert Cr, Cb capture phase

ADJ0: Input phase adjust0
0 : No phase adjust (default)
1 : Invert Y and Cr, Cb capture phase

02H CCE: closed caption encode enable register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
—	—	—	—	—	—	CCEN1	CCEN0

CCEN1: Second field caption encode enable
0 : disable (default)
1 : enable

CCEN0: First field caption encode enable
0 : disable (default)
1 : enable

03H CAPT0: caption data register0

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
—	First caption data in first field						

04H CAPT1: caption data register1

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
—	Second caption data in first field						

05H CAPT2: caption data register2

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
—	First caption data in second field						

06H CAPT3: caption data register3

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
—	Second caption data in second field						

08–46H: overlay color registers

Set colors which overlay displays.

When input mode is YCbCr, overlay colors are set in YCbCr format.

YG0–YG15 register: Sets luminance level as 8-bit unsigned integer
Black level is 0; setting value must be under 240.
B0–B15 register: Sets Cb signal at 8-bit 2s complement signed integer
R0–R15 register: Sets Cr signal at 8-bit 2s complement signed integer

When input mode is RGB, overlay colors are set in RGB format. In this case, black level is 0. When IMOD0 is 0, the setting value must be less than 240. When IMOD0 is 1, there is no limitation on value setting.

YG0–YG15 register: Sets G signal level at 8-bit unsigned integer
B0–B15 register: Sets B signal level at 8-bit unsigned integer
R0–R15 register: Sets R signal level at 8-bit unsigned integer

48H ATR0: video attribute data register0

NTSC

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
—	—	WORD0-B			WORD0-A		

PAL

Not used

49H ATR1: video attribute data register1

NTSC

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WORD2				WORD1			

PAL

Set GROUP1 and GROUP2 data.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GROUP2				GROUP1			

4AH ATR2: video attribute data register2

NTSC

Set CRC data and enable attribute data insertion.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ATR_EN	—	CRC					

ATR_EN: Attribute insertion enable
Selects enable/disable insertion of attribute information
0 : No insertion of attribute information (default)
1 : Inserts attribute information

PAL

Set GROUP3 and GROUP4 data and enable attribute data insertion.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ATR_EN	—	GROUP4			GROUP3		

ATR_EN: Attribute insertion enable
Selects enable/disable insertion of attribute information
0 : No insertion of attribute information (default)
1 : Inserts attribute information

applications circuits

To use the ’AV410/411 built-in oscillator, connect a third overtone crystal (equivalent series resistance under 40 Ω) to OSCIN and OSCOUT terminals. The recommended oscillator circuit is shown in Figure 12. The accuracy of the subcarrier frequency depends on the accuracy of the system clock. TI recommends using a crystal oscillator with deviation of frequency under ±50 ppm. Other circuits are shown in Figure 13 and Figure 14.

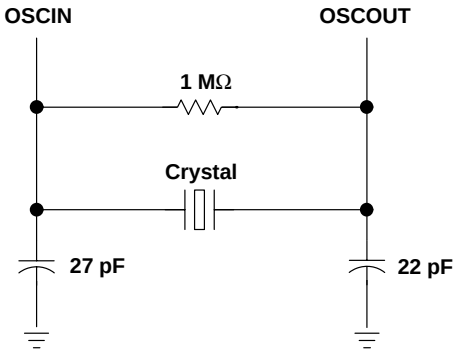
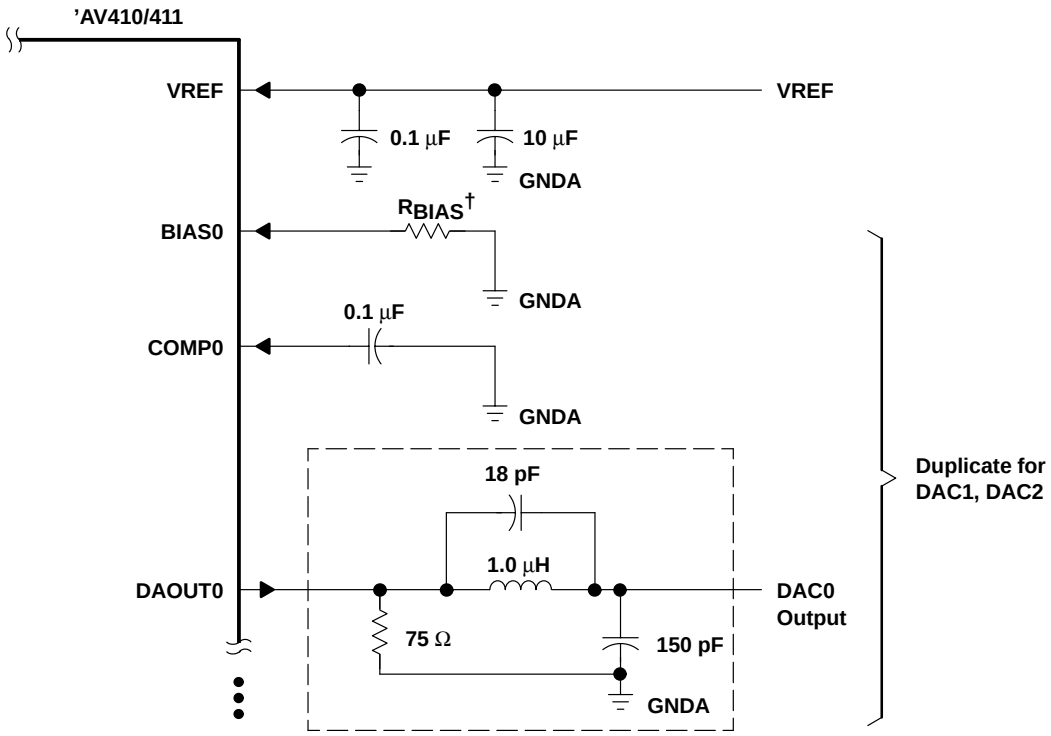


Figure 12. Recommended Oscillator Circuit



† For Y, C, composite output, R_{BIAS} = 280 Ω
For RGB output, R_{BIAS} = 530 Ω

Figure 13. 'AV410/411 Output D/A Biasing

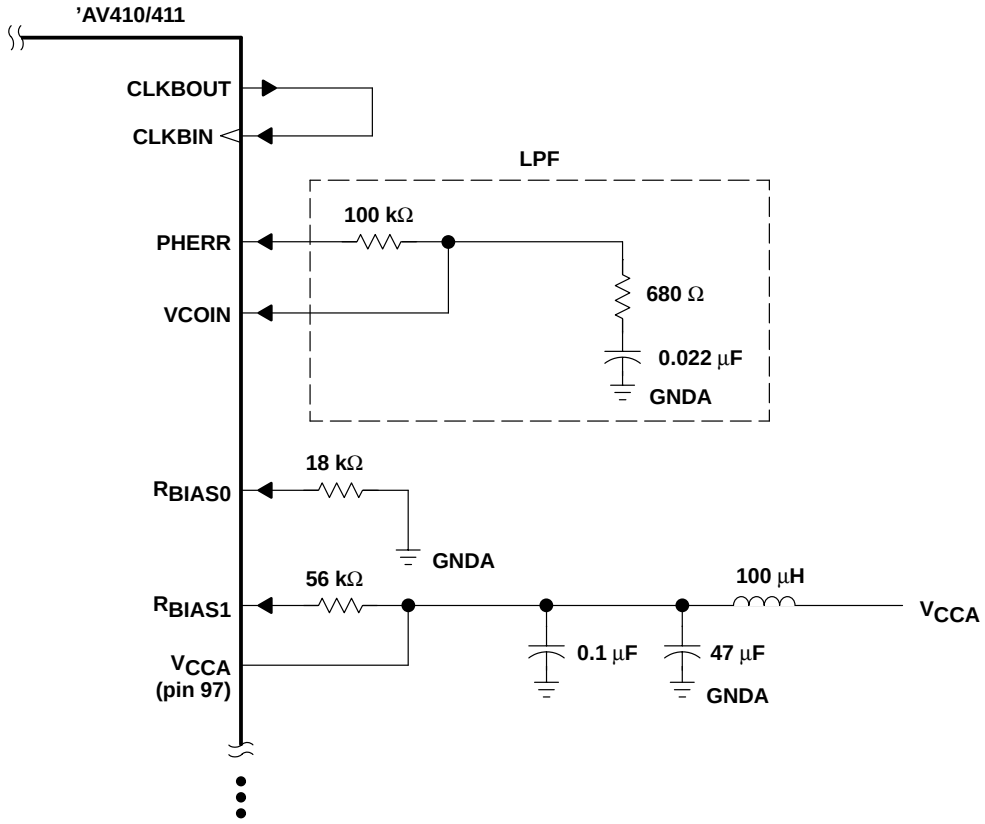


Figure 14. Pin Configuration for Optional PLL Circuit

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4 V
Supply voltage range, V_{CCA} . . . . . –0.5 V to 6 V
Supply voltage range, V_{CCS} . . . . . –0.5 V to 6 V
Input voltage range, V_I . . . . . –0.5 V to V_{CCS} + 0.5 V
Output voltage range, V_O . . . . . –0.5 V to V_{CCS} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CCS}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CCS}) . . . . . ±20 mA
Operating free-air temperature range . . . . . –10°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{CCA}	Analog supply voltage		4.75	5	5.25	V
V_{CCS}	Input/output supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	All except SCL, SDA	2			V
		SCL, SDA	$0.7V_{CCS}$			
V_{IL}	Low-level input voltage	All except SCL, SDA			0.8	V
		SCL, SDA			0.8	
I_{OH}	High-level output current	All except $\overline{\text{CSYNC}}$	–400			µA
		$\overline{\text{CSYNC}}$	–10.8			mA
I_{OL}	Low-level output current	All except $\overline{\text{CSYNC}}$			3.2	mA
		$\overline{\text{CSYNC}}$			38	
f_{clk}	Clock frequency	NTSC/PAL		27		MHz
		NTSC only		28.6363		
V_{ref}	D/A reference voltage	VREF input	1.21	1.235	1.26	V
T_A	Operating temperature range		–10	25	70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All except $\overline{\text{CSYNC}}$, OSCOUT	V_{CCS} = 4.75 V,	I_{OH} = –400 µA	V_{CCS}–0.8			V
		$\overline{\text{CSYNC}}$	V_{CCS} = 4.75 V,	I_{OH} = –10.8 mA	V_{CC}–0.55			
		OSCOUT	V_{CC} = 3 V,	I_{OH} = –400 µA	2			
V_{OL}	Low-level output voltage	All except $\overline{\text{CSYNC}}$, OSCOUT	V_{CCS} = 4.75 V,	I_{OL} = 3.2 mA			0.5	V
		$\overline{\text{CSYNC}}$	V_{CCS} = 4.75 V,	I_{OL} = 38 mA				
		OSCOUT	V_{CC} = 3 V,	I_{OL} = 800 µA				
I_I	Input current	All except OSCIN	V_{CCS} = 5.25 V,	V_I = 0 to V_{CCS}			±1	µA
I_{IL}	Input current	OSCIN	V_{CC} = 3.6 V,	V_I = 0			–50	µA
I_{IH}	Input current	OSCIN	V_{CC} = 3.6 V,	V_I = 3.6 V			10	µA
I_{CC}	Digital supply current		V_{CC} = 3.6 V			85	95	mA
I_{CCA}	Analog supply current		V_{CCA} = 5.25 V			130	150	mA
INL	DAC integral lineality error		V_{ref} = 1.235 V		–1.5		1.5	LSB
DNL	DAC differential lineality error		R_{bias} = 280 Ω		–1		1	LSB
	DAC monotonicity		Load = 39 Ω		Guaranteed			
	DAC output voltage (code = 511)		T_A = 25°C		1.20		1.33	V

video data input timing requirements over recommended operating voltage and temperature ranges (see Figure 15)

PARAMETER			MIN	MAX	UNIT
t_{su}	D, OLC, OL before CLK0↑	Internal sync mode	20		ns
		External sync mode	5		
t_h	D, OLC, OL after CLK0↑	Internal sync mode	0		ns
		External sync mode	3		

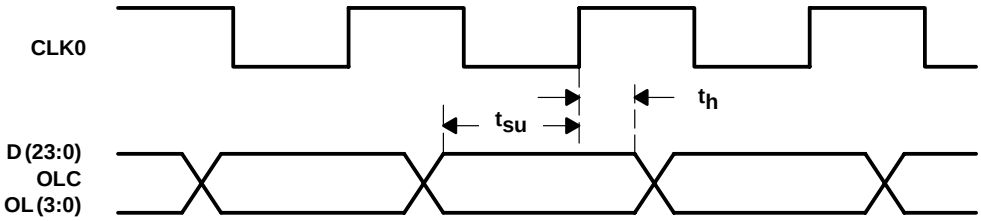


Figure 15. Video Data Input Timing

video data input timing requirements over recommended operating voltage and temperature ranges (see Figure 16)

		ALTERNATE SYMBOL			MIN	TYP	MAX	UNIT
t_{d1}†	Data input start timing	t_{st1}	NTSC	f_{clk} = 27 MHz	$\frac{240}{27 \cdot 10^6}$			s
			NTSC	f_{clk} = 28.6 MHz	$\frac{256}{28.6 \cdot 10^6}$			
			PAL	f_{clk} = 27 MHz	$\frac{260}{27 \cdot 10^6}$			
t_{d2}†	Data input start timing	t_{st2}	NTSC	f_{clk} = 13.5 MHz	$\frac{120}{13.5 \cdot 10^6}$			s
			NTSC	f_{clk} = 14.3 MHz	$\frac{128}{14.3 \cdot 10^6}$			
			PAL	f_{clk} = 13.5 MHz	$\frac{130}{13.5 \cdot 10^6}$			

† Guaranteed by design.

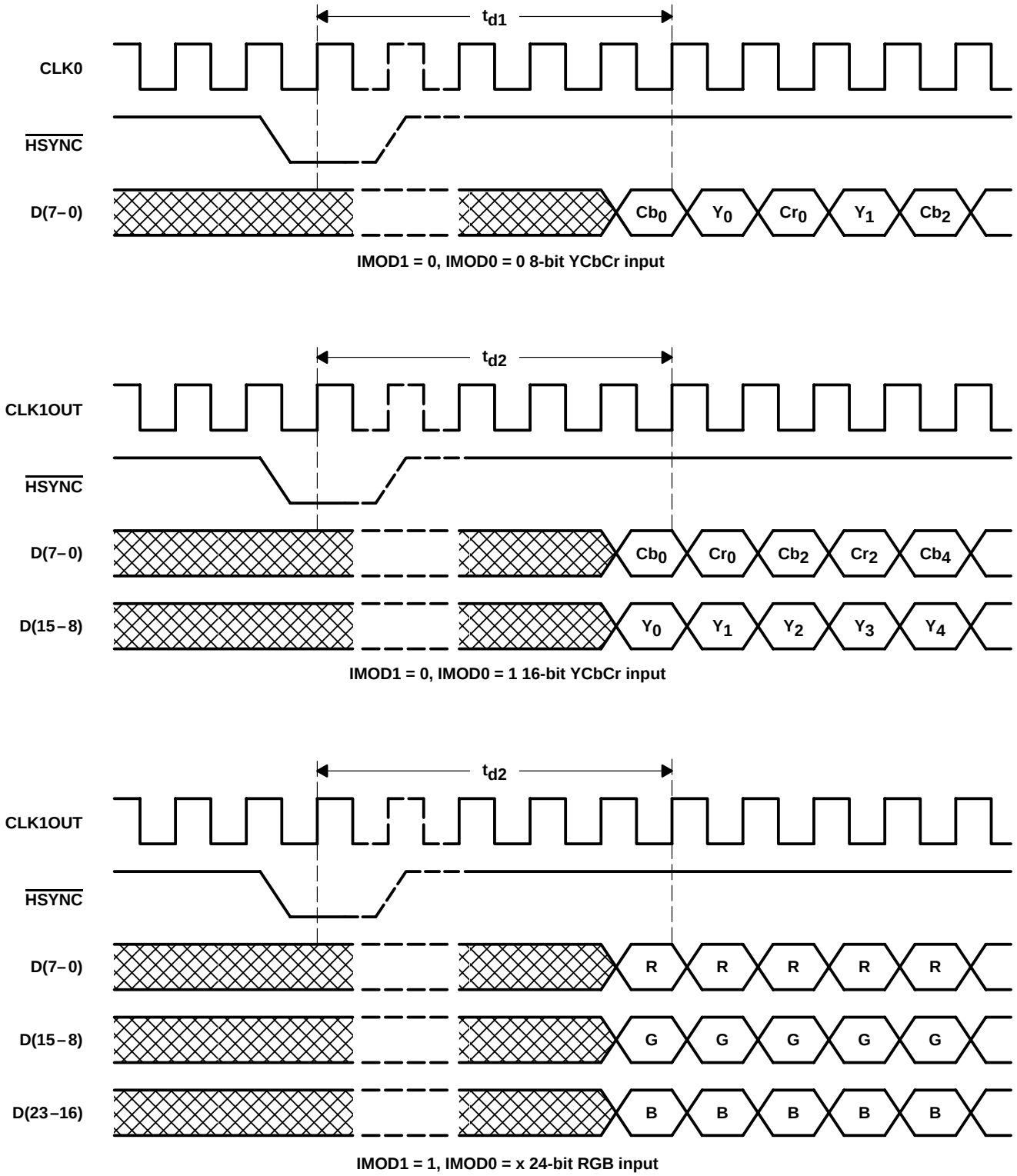


Figure 16. Video Data Input Timing

internal synchronization mode output timing requirements over recommended operating voltage and temperature ranges (see Figure 17)

	PARAMETER	MIN	MAX	UNIT
t_d	Delay time, CLK0 to $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, EVEN		10	ns

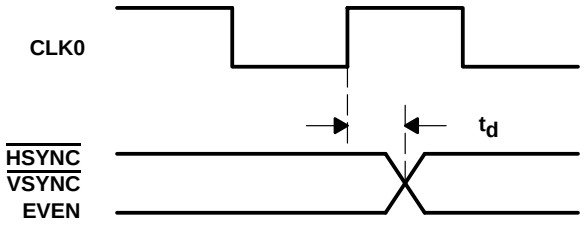


Figure 17. Internal Synchronization Mode Output Timing

external synchronization mode input timing requirements over recommended operating voltage and temperature ranges (see Figure 18)

	PARAMETER	MIN	MAX	UNIT
t_{su}	Setup time, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ before CLK0 ↑	5		ns
t_h	Hold time, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ after CLK0 ↑	3		ns

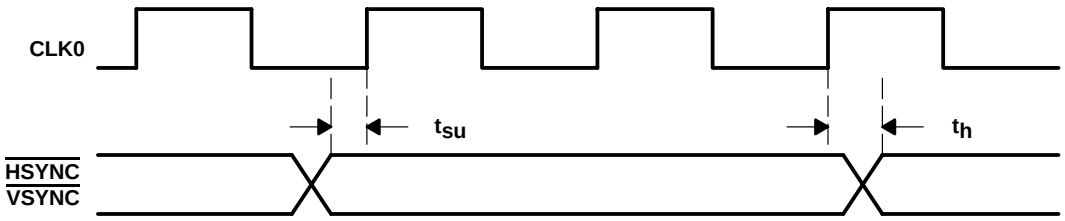


Figure 18. External Synchronization Mode Input Timing: $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$

external pulse duration timing requirements over recommended operating voltage and temperature ranges (see Figure 19)

	PARAMETER	MIN	MAX	UNIT
t_w	Pulse duration, $\overline{\text{RESET}}$	100		ns
t_w	Pulse duration, $\overline{\text{HSYNC}}$	100		ns

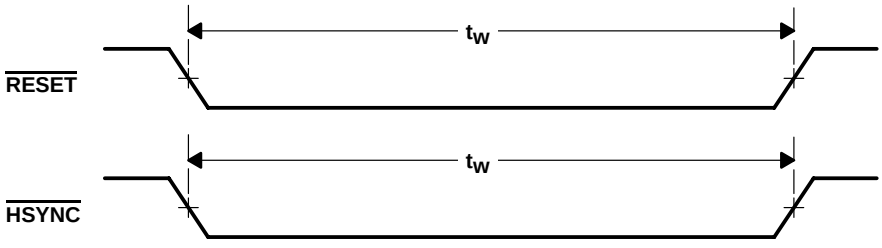


Figure 19. External Pulse Duration: $\overline{\text{HSYNC}}$ and $\overline{\text{RESET}}$

internal synchronization mode output timing requirements over recommended operating voltage and temperature ranges (see Figure 20)

PARAMETER			MIN	TYP	MAX	UNIT
t_W‡	Pulse duration, VSYNC	NTSC		3		H†
		PAL		2		H

† H is the RS170A line period.
‡ Guaranteed by design.

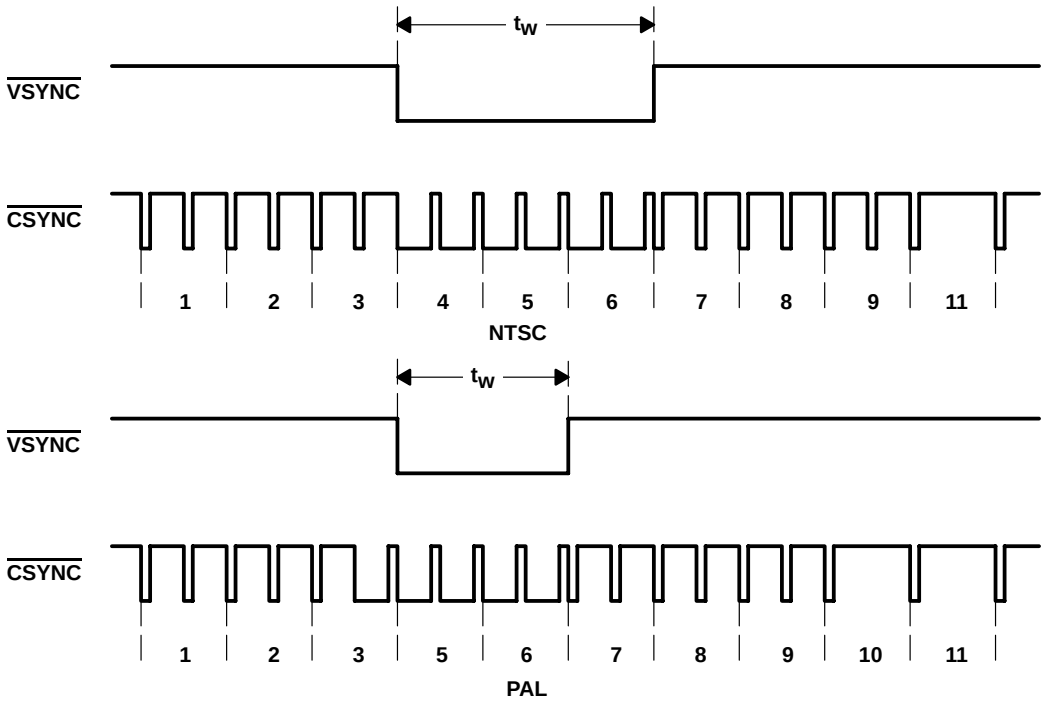


Figure 20. Internal Synchronization Mode: $\overline{\text{VSYNC}}$ Output Timing

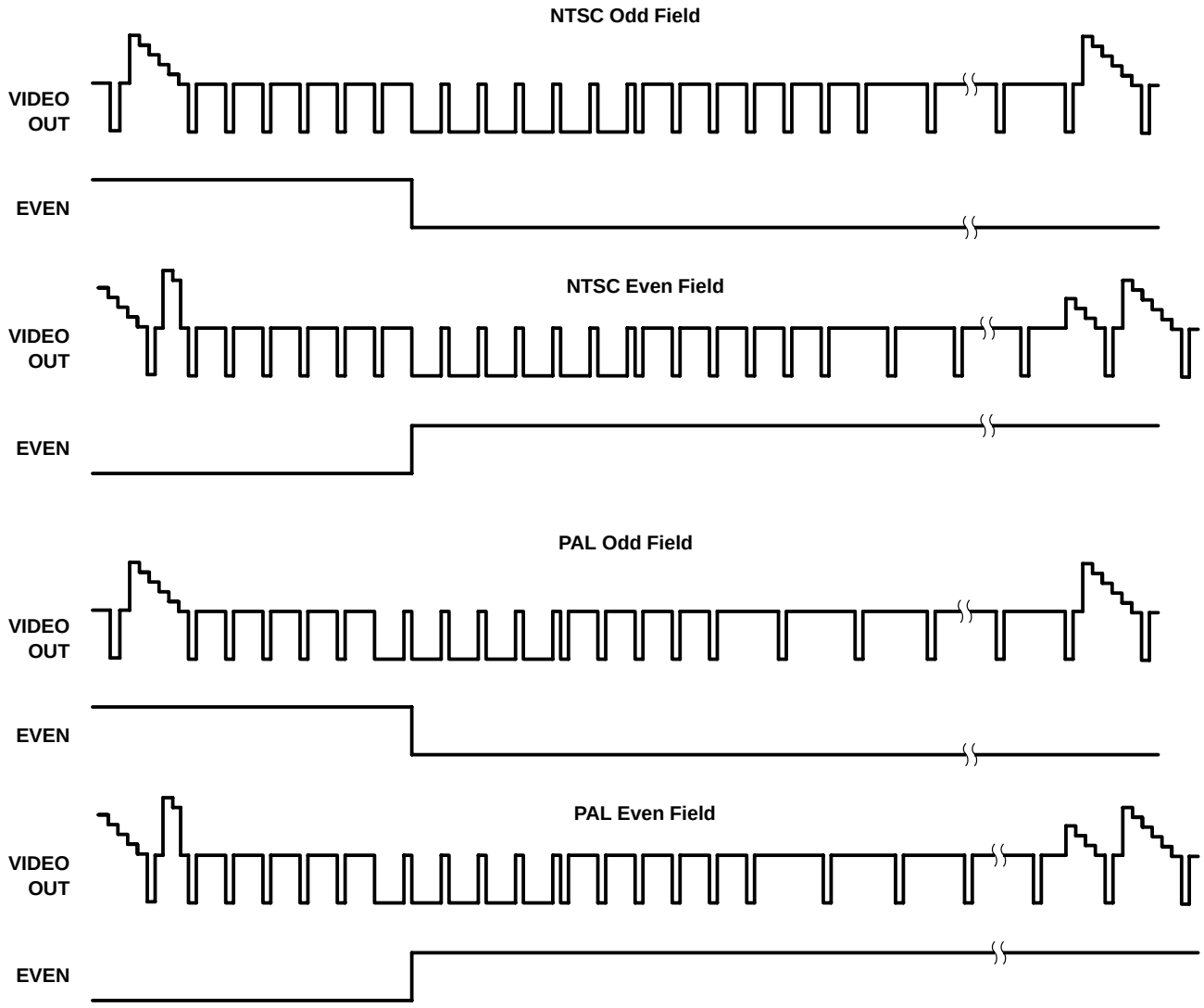


Figure 21. EVEN Signal Output Timing

I²C interface timing requirements over recommended operating voltage and temperature ranges (see Note 1 and Figure 22)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
f_{clock}	Clock frequency, SCL		f_{scl}	0	400	kHz
t_w	Pulse duration, SCL	Low	t_{low}	1.3		µs
		High	t_{high}	0.6		
t_d	Delay time, SDA free time on bus prior to transmission		t_{buf}	1.3		µs
t_{su1}	Setup time, start condition	SCL before SDA	$t_{su,\ sta}$	0.6		µs
t_{su2}	Setup time, stop condition	SCL before SDA	$t_{su,\ sto}$	4.7		µs
t_{su3}	Setup time, master write	SDA before SCL	$t_{su,\ dat}$	100		µs
t_{h1}	Hold time, start to first SCL pulse		$t_{hd,\ sta}$	0.6		µs
t_{h2}	Hold time, data master write	SDA after SCL	$t_{hd,\ dat}$	0		µs
t_{h3}	Hold time, data master read	SDA after SCL	$t_{hd,\ dat}$	150		µs
t_r	Rise time, SDA, SCL				300	ns
t_f	Fall time, SDA, SCL				300	ns

NOTE 1: Guaranteed, not tested.

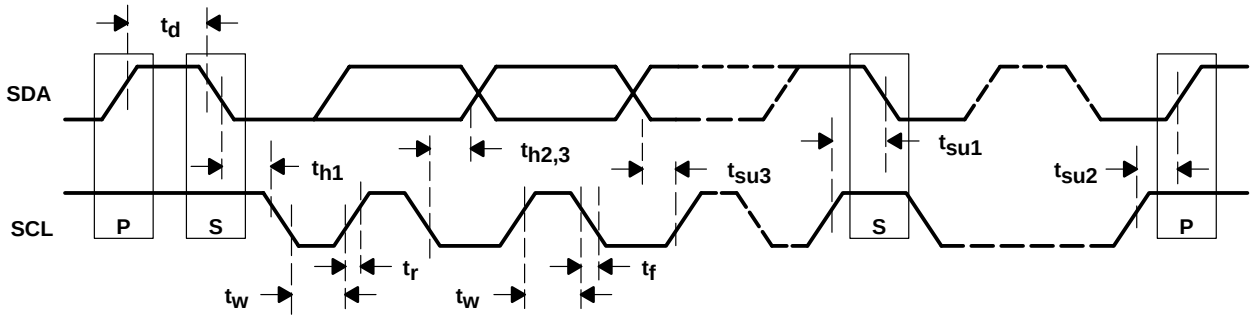


Figure 22. I²C Interface Timing

serial mode timing requirements over recommended operating voltage and temperature ranges (see Figure 23)

PARAMETER			MIN	MAX	UNIT
t_w	Pulse duration	SCL low	150		ns
		SCL high	150		
t_{su}	Setup time, $\overline{CS}$, $\overline{SDA}$ before SCL ↑		50		ns
t_h	Hold time, $\overline{CS}$, $\overline{SDA}$ after SCL ↑		10		ns

serial mode switching requirements over recommended operating voltage and temperature ranges (see Figure 23)

PARAMETER		MIN	MAX	UNIT
t_{en}	Enable time, $\overline{CS}$ to SOUT		10†	ns
t_{dis}	Disable time, $\overline{CS}$ to SOUT		15†	ns
t_d	Delay time, SCL to SOUT		150	ns

† Design value

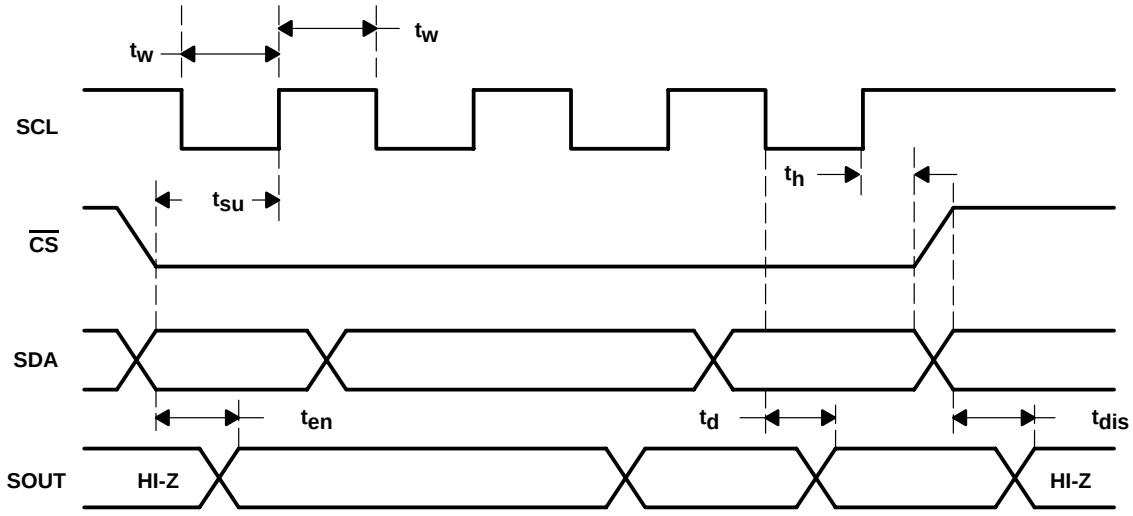
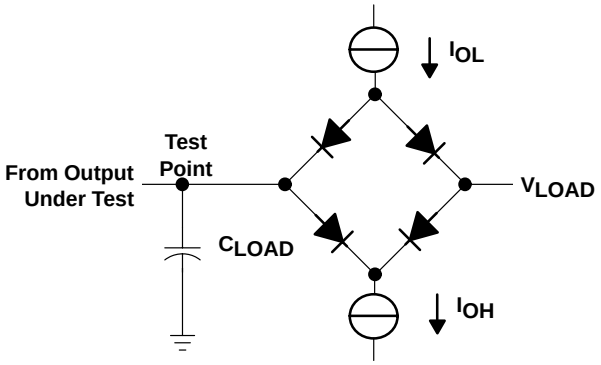
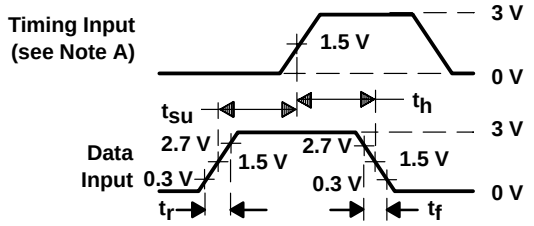


Figure 23. Simple Serial Mode Timing

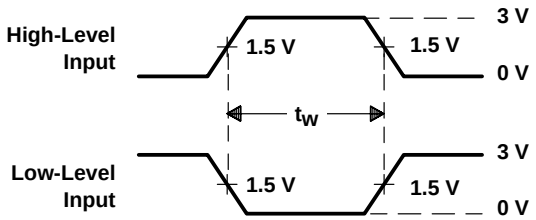
PARAMETER MEASUREMENT INFORMATION



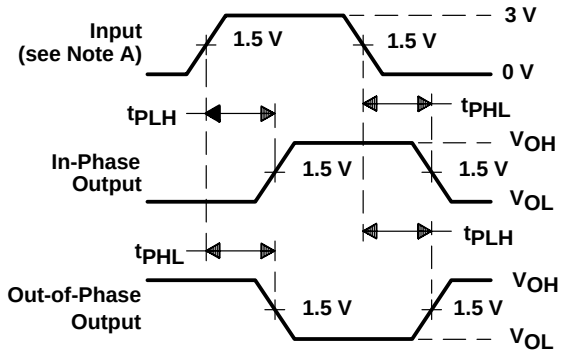
LOAD CIRCUIT



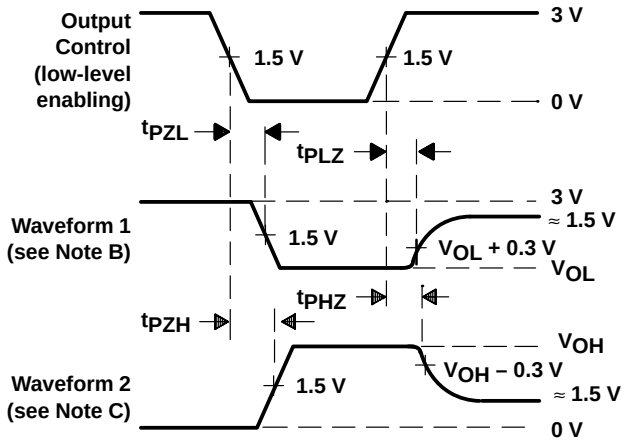
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



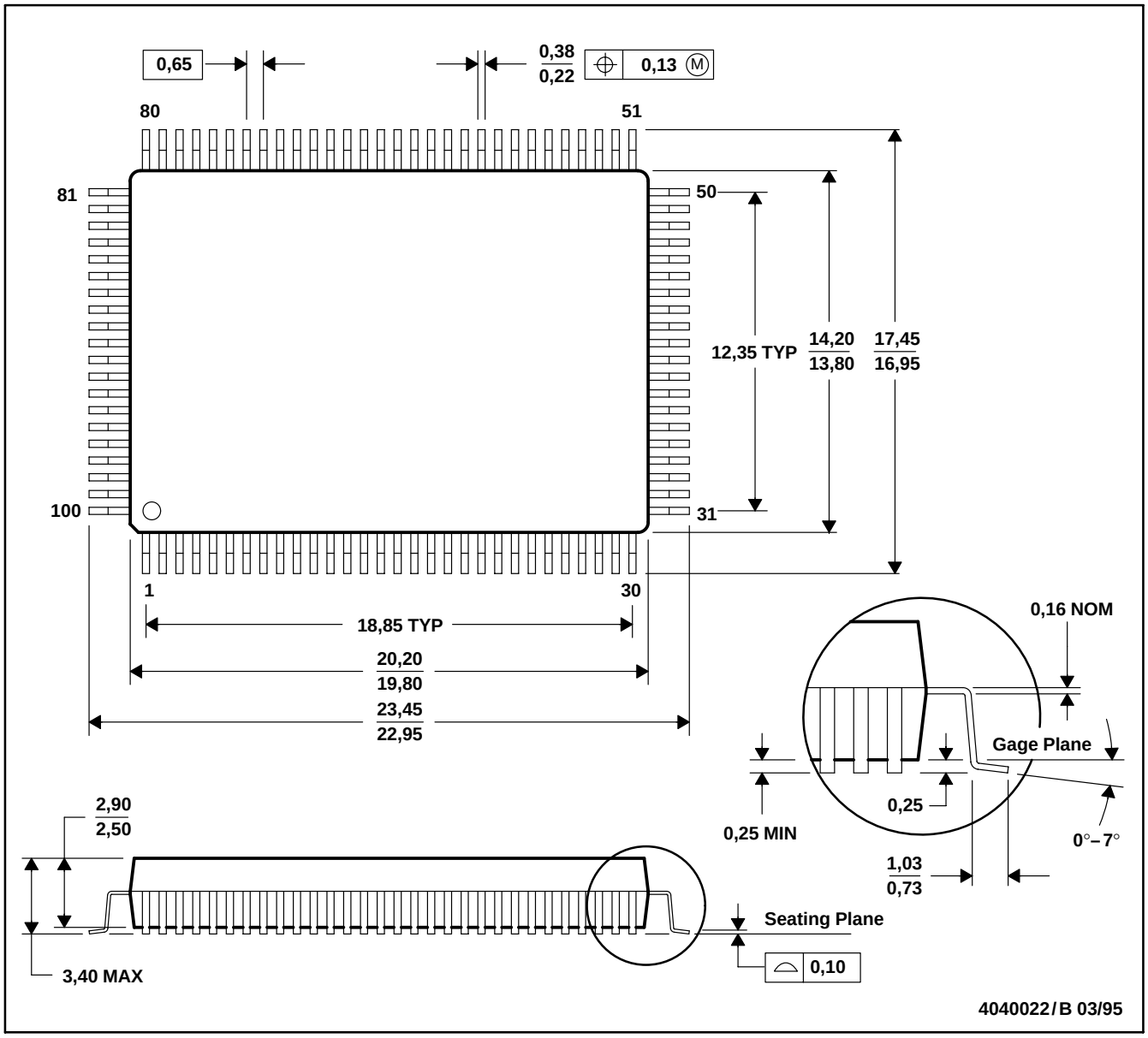
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by pulse generators having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, $t_r \le 6$ ns, $t_f \le 6$ ns.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
C. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. For t_{PLZ} and t_{PHZ}, V_{OL} and V_{OH} are measured values.

Figure 24. Load Circuit and Voltage Waveforms

MECHANICAL DATA

PJM (R-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-022

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