- **Direct Interface to the TMS320AV120 MPEG Audio Decoder and the TMS320AV420 NTSC Encoder**
- **Based on the C-Cube™ CL450™ Core**
- **Microcode Is Stored in an On-Chip ROM**
- **Audio Input Buffer Is On Chip**
- **Audio/Video Synchronization Logic Is Included**
- **Simple Microprocessor Host Interface**
- **Direct Interface to Either the Sony or Sanyo CD-ROM Decoders**
- **Video-CD Specific Functions:**
  - **Fast Forward and Reverse**
  - **Still Picture**
  - **Direct DRAM (Stream In) Access**
- **Fully Complies With All Requirements of the MPEG Standard (ISO CD 11172)**
- **Performs Real-Time Decoding of CIF-Resolution Bitstreams (352×240 Pixels at 30 Hz or 352×288 Pixels at 25 Hz)**
- **Performs Real-Time Horizontal Pixel Interpolation and Frame Duplication to Produce Output Formats of 704 × 240 Pixels at 60 Hz or 704 × 288 Pixels at 50 Hz**
- **Automatically Converts Decompressed Video to RGB Color-Space, Optional YCbCr Output**
- **Supports NTSC and PAL Video Output Timing Formats**
- **Interfaces to Z-80, H-8, or Similar Processors and DRAM With No External Logic**
- **Requires Only 4 Mbits of 80-ns DRAM to Decode CIF-Resolution MPEG Bit Streams**
- **Decodes Huffman Variable-Length Codes at a Peak Rate of 4 Bits Per Clock (160 Mbit/s at 40 MHz)**
- **Is Fabricated in EPIC™ CMOS Process**

description

The TMS320AV220 is a video CD MPEG-1 decoder designed to operate with the TMS320AV120 MPEG audio decoder to implement a complete audio and video decoder solution. It also interfaces directly with the TMS320AV420 NTSC encoder.

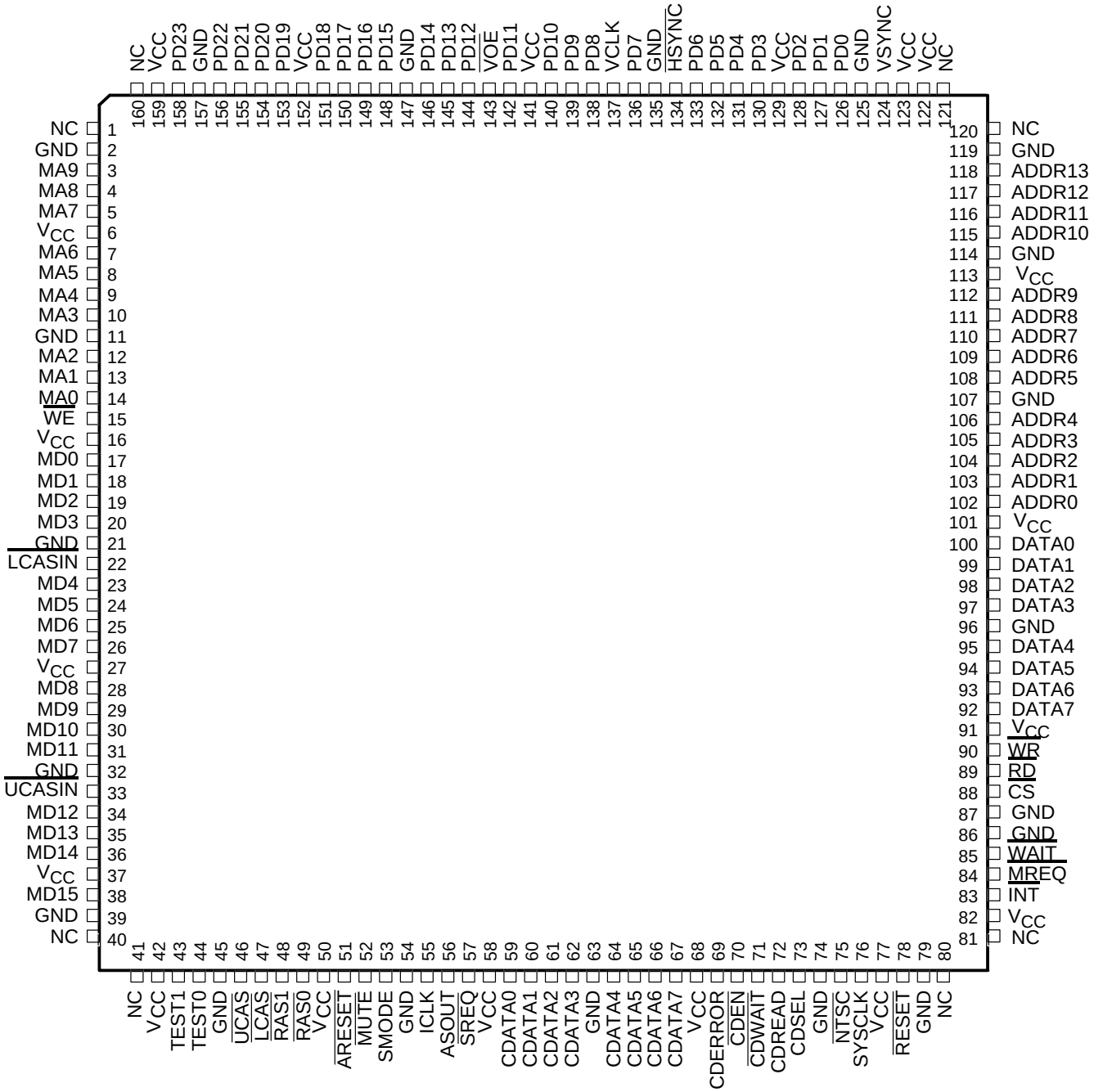
The TMS320AV220 is designed to be fully compatible with the video-CD and Karaoke standards and is targeted for low-cost, consumer-oriented applications. All components required to accept and decode the multiplexed MPEG-1 system stream are included on the chip, including the logic necessary for audio/video synchronization. The ’AV220 also accepts MPEG-1 packet streams. With the addition of appropriate headers, video picture streams are accepted and audio PCM data can be passed through the ’AV220 to the ’AV120 for playback in bypass mode.

The TMS320AV220/120 chip set is designed to interface to a host system through a generic 8-bit microprocessor interface. Glueless interface is possible to a Z-80, H-8, or similar processor.

The compressed MPEG-1 data-stream interface is through an 8-bit port that can directly connect to either of the popular Sanyo (LC8950 or LC8951) or Sony (CXD1186BQ) CD-ROM decoders.

C-Cube and CL450 are trademarks of C-Cube Microsystems.
EPIC is a trademark of Texas Instruments Incorporated.

PCM PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADDR13 ADDR12 ADDR11 ADDR10 ADDR9 ADDR8 ADDR7 ADDR6 ADDR5 ADDR4 ADDR3 ADDR2 ADDR1 ADDR0	118 117 116 115 112 111 110 109 108 106 105 104 103 102	I	Host address bus. ADDR13–ADDR0 are used by the host to address the 'AV220 registers and external DRAM.
$\overline{\text{ARESET}}$	51	O	Audio reset, active low. $\overline{\text{ARESET}}$ can be tied directly to $\overline{\text{RESET}}$ of the TMS320AV120 audio decoder.
ASOUT	56	O	Audio data serial output. MPEG audio frames are output at ASOUT. ASOUT can be tied directly to the SIN input of the TMS320AV120.
CDATA7 CDATA6 CDATA5 CDATA4 CDATA3 CDATA2 CDATA1 CDATA0	67 66 65 64 62 61 60 59	I	Compressed-data bus. MPEG-1 system streams are input at this bus.
$\overline{\text{CDEN}}$	70	I	Compressed-data enable, active low. When CDSEL is low, $\overline{\text{CDEN}}$ acts as the write strobe from the CD controller. When CDSEL is high, $\overline{\text{CDEN}}$ acts as the transfer enable from the CD controller.
CDERROR	69	I	Compressed-data error. When CDERROR is high, the data on CDATA contains errors.
CDREAD	72	O	Compressed-data read strobe. When CDSEL is low, the rising edge of CDREAD is the read request to the CD controller. When CDSEL is high, the falling edge of CDREAD is the read request and data is latched on the rising edge of CDREAD.
CDSEL	73	I	Compressed-data interface select. CDSEL changes the operation of $\overline{\text{CDEN}}$ and CDREAD to select between different CD controllers. CDSEL low selects the Sony interface and CDSEL high selects the Sanyo interface.
$\overline{\text{CDWAIT}}$	71	I	Compressed-data wait. $\overline{\text{CDWAIT}}$ is active low when CDSEL is high and should be tied high when CDSEL is low.
$\overline{\text{CS}}$	88	I	Chip select, active low. $\overline{\text{CS}}$ enables register or DRAM read/writes by the host processor.
DATA7 DATA6 DATA5 DATA4 DATA3 DATA2 DATA1 DATA0	92 93 94 95 97 98 99 100	I/O	Host data bus. DATA7–DATA0 is used by the host processor when accessing 'AV220 registers and during direct memory DRAM accesses. MPEG data can not be input on DATA7–DATA0.
GND	2, 11 21, 32, 39, 45, 54, 63, 74, 79, 86, 87, 96, 107, 114, 119, 125, 135, 147, 157		Ground

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{HSYNC}}$	134	I	Horizontal synchronization, active low. $\overline{\text{HYSNC}}$ controls the 'AV220 pixel-data output horizontal-line timing. $\overline{\text{HYSNC}}$ ties directly to the TMS320AV420 $\overline{\text{HYSNC}}$ output.
ICLK	55	O	Audio data clock. Each rising edge of ICLK indicates that compressed audio data is valid at ASOUT. ICLK can be tied directly to ICLK of the TMS320AV120 audio decoder.
$\overline{\text{INT}}$	83	O	Interrupt request, active low. $\overline{\text{INT}}$ goes low when an interrupt occurs and stays low until the INTERRUPT register is read. $\overline{\text{INT}}$ is an open-drain output.
$\overline{\text{LCAS}}$	47	O	Low-byte column-address strobe, active low. $\overline{\text{LCAS}}$ latches the DRAM column address for the lower memory data byte, MD7 – MD0.
$\overline{\text{LCASIN}}$	22	I	Lower data-latch enable. The 'AV220 latches data coming from the low data byte of the DRAM (MD7 – MD0) on the rising edge of $\overline{\text{LCASIN}}$. Typically, $\overline{\text{LCASIN}}$ is connected to the DRAM $\overline{\text{CAS}}$ terminal mechanically farthest from the 'AV220.
MA9 MA8 MA7 MA6 MA5 MA4 MA3 MA2 MA1 MA0	3 4 5 7 8 9 10 12 13 14	O	DRAM memory address. The 'AV220 multiplexes the row and column addresses on MA9 – MA0 to address 4 Mbits of DRAM (see the section on DRAM interface for more information about how the address signals are used with different DRAM components and DRAM array sizes).
MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8 MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0	38 36 35 34 31 30 29 28 26 25 24 23 20 19 18 17	I/O	DRAM memory data bus. Data is transferred between the 'AV220 and the local DRAM memory via MD15 – MD0. The direction of the data transfer is determined by the state of $\overline{\text{WE}}$.
$\overline{\text{MREQ}}$	84	I	Memory-access request, active low. $\overline{\text{MREQ}}$ requests a memory or register read/write by the host processor.
$\overline{\text{MUTE}}$	52	O	Audio mute, active low. The 'AV220 asserts $\overline{\text{MUTE}}$ during fast mode and when the audio buffer is empty and EOS is detected. $\overline{\text{MUTE}}$ is also asserted if a bit error occurs in the packet length causing the packet to be discarded. $\overline{\text{MUTE}}$ ties directly to the $\overline{\text{MUTE}}$ input of the TMS320AV120 audio decoder.
NC	1, 40, 41, 80, 81, 120, 121, 160		No connect. These terminals must be left floating.
$\overline{\text{NTSC}}$	75	I	NTSC/PAL video output select. When $\overline{\text{NTSC}}$ is low, the video output is in the NTSC format. When $\overline{\text{NTSC}}$ is high, the video output is in the PAL format.

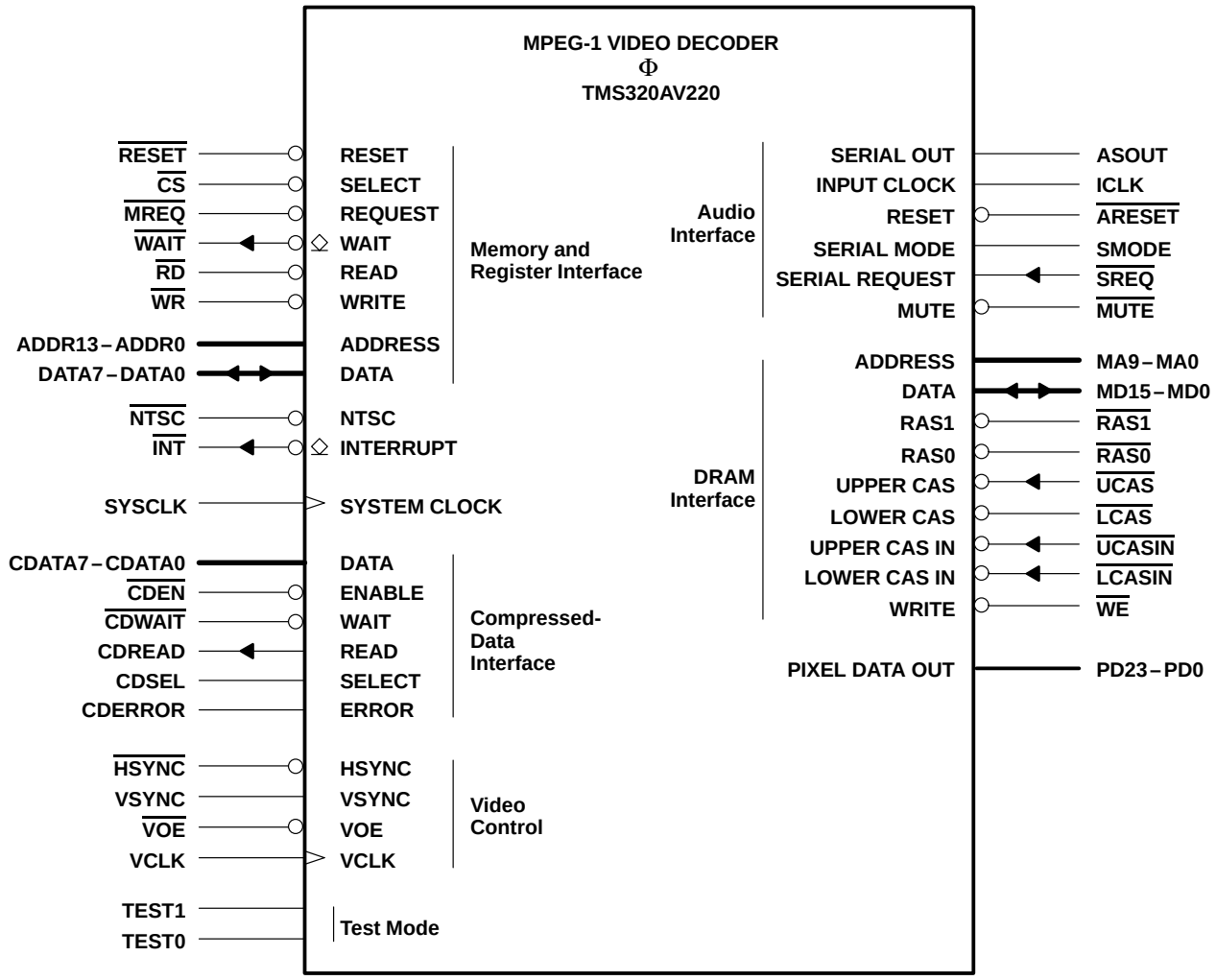
Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PD23 PD22 PD21 PD20 PD19 PD18 PD17 PD16 PD15 PD14 PD13 PD12 PD11 PD10 PD9 PD8 PD7 PD6 PD5 PD4 PD3 PD2 PD1 PD0	158 156 155 154 153 151 150 149 148 146 145 144 142 140 139 138 136 133 132 131 130 128 127 126	O	Pixel data bus. The ’AV220 transmits pixel data to the video display subsystem using PD23–PD0. Each 24-bit word on PD23–PD0 contains eight bits each of blue (PD23–PD16), green (PD15–PD8), and red (PD7–PD0). The highest bit of each component is most significant; (i.e., blue7 corresponds to PD23). The ’AV220 can be configured to output the pixel data in the YCbCr color space. When the YCbCr format is selected, the luminance (Y) values are output on PD15–PD8. The Cb and Cr coefficients alternate on successive VCLK periods and are output on PD7–PD0. PD23–PD16 are not used when YCbCr is selected. PD23–PD0 tie directly to the D23–D0 inputs of the TMS320AV420 NTSC encoder.
$\overline{\text{RAS1}}$ $\overline{\text{RAS0}}$	48 49	O	DRAM row-address strobe. The ’AV220 asserts these signals to latch the row address into the local DRAM array. $\overline{\text{RAS0}}$ (active low) latches the row address. $\overline{\text{RAS1}}$ is reserved and should not be connected.
$\overline{\text{RD}}$	89	I	Read strobe, active low. $\overline{\text{RD}}$ is used by the host when reading ’AV220 registers.
$\overline{\text{RESET}}$	78	I	Reset, active low. $\overline{\text{RESET}}$ is required to first initialize the device on power up. $\overline{\text{RESET}}$ low clears all buffers, resets the video decoder core, downloads microcode, and initializes registers. The host can not read or write registers or memory (DRAM) until the reset sequence is completed, in not more then 25 ms. If a register access is attempted during the reset period, the chip activates the $\overline{\text{WAIT}}$ line until the reset is completed. The CD interface does not accept data during this time. The ’AV220 does not activate CDREAD until the reset sequence is completed. $\overline{\text{RESET}}$ low causes $\overline{\text{ARESET}}$ to pulse low resetting the audio decoder.
SMODE	53	O	Audio data/timing information select. SMODE is low when output data on ASOUT is compressed audio. SMODE is high when output data on ASOUT is either a (PTS) (bit 33 low) or a SCR (bit 33 high). SMODE ties directly to the SMODE input of the TMS320AV120.
$\overline{\text{SREQ}}$	57	I	Audio serial-data request input, active low. $\overline{\text{SREQ}}$ is the handshake signal provided by the audio decoder that requests the ’AV220 to output more audio data. $\overline{\text{SREQ}}$ ties directly to the TMS320AV120 $\overline{\text{SREQ}}$ output.
SYSCLK	76	I	System clock, 40 MHz. The ’AV220 uses SYSCLK to clock the internal processor and the DRAM controller. For proper operation of the ’AV220, SYSCLK must have a nominal frequency of 40 MHz. All local DRAM accesses are synchronized to this clock. VCLK is limited to half the frequency of SYSCLK. The use of a precision 40-MHz oscillator for SYSCLK is strongly recommended. Other information in this data sheet regarding the performance and speed of the ’AV220 is based on a 40-MHz SYSCLK frequency.
TEST1 TEST0	43 44	I	Test-mode select. Tie TEST1 and TEST0 low for normal operation.
$\overline{\text{UCAS}}$	46	O	Upper-byte column-address strobe, active low. $\overline{\text{UCAS}}$ latches the column address in DRAM for the upper memory data byte, MD15–MD8.
$\overline{\text{UCASIN}}$	33	I	Upper data-latch enable. The ’AV220 latches data coming from the high data byte of the DRAM (MD15–MD8) on the rising edge of $\overline{\text{UCASIN}}$. Typically, $\overline{\text{UCASIN}}$ is connected to the DRAM $\overline{\text{CAS}}$ terminal mechanically farthest from the ’AV220.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
V_{CC}	6, 16, 27, 37, 42, 50, 58, 68, 77, 82, 91, 101, 113, 122, 123, 129, 141, 152, 159		5-V supply voltage
VCLK	137	I	Video clock. The ’AV220 outputs one pixel on PD23 – PD0 for each cycle of VCLK. VCLK can not run faster than one-half the frequency of SYSCLK and is typically 13.5 MHz. VCLK ties directly to the CLK135 output of the TMS320AV420 NTSC encoder.
$\overline{\text{VOE}}$	143	I	Video output enable, active low. $\overline{\text{VOE}}$ must be low for the ’AV220 to drive the pixel data bus (PD23 – PD0). When $\overline{\text{VOE}}$ is high, the pixel data bus is in a high-impedance state.
VSYNC	124	I	Vertical synchronization. VSYNC controls the ’AV220 pixel-data output frame timing. VSYNC ties directly to the VSYNC output of the TMS320AV420 .
$\overline{\text{WAIT}}$	85	O	Wait request to host, active low. $\overline{\text{WAIT}}$ low requests the host to wait during register read and write cycles. If an access is attempted during the reset period, the chip activates the $\overline{\text{WAIT}}$ line until the reset is completed. $\overline{\text{WAIT}}$ is an open-drain output.
$\overline{\text{WE}}$	15	O	Write enable, active low. When low, $\overline{\text{WE}}$ requests a write to the DRAM and reads from the DRAM when high.
$\overline{\text{WR}}$	90	I	Write strobe, active low. $\overline{\text{WR}}$ is used by the host when writing to ’AV220 registers.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

architecture

The TMS320AV220 is based on the C-Cube CL450 core with significant additional functionality as shown in Figure 1. While the video processing is done by the ’450 core, all user interaction is through a simplified user interface consisting of 14 control registers. The control logic automatically initializes all other registers and loads microcode from internal ROM into DRAM after each reset. This control philosophy was adopted to ensure ease of operation in a consumer environment.

Audio/video synchronization is done independently by both the video processor and the companion TMS320AV120 MPEG audio decoder. They both perform synchronization using the system clock reference (SCR) and presentation time stamp (PTS) in the MPEG-1 system stream either by delaying presentation or by skipping forward as needed. No user interaction is required for synchronization.

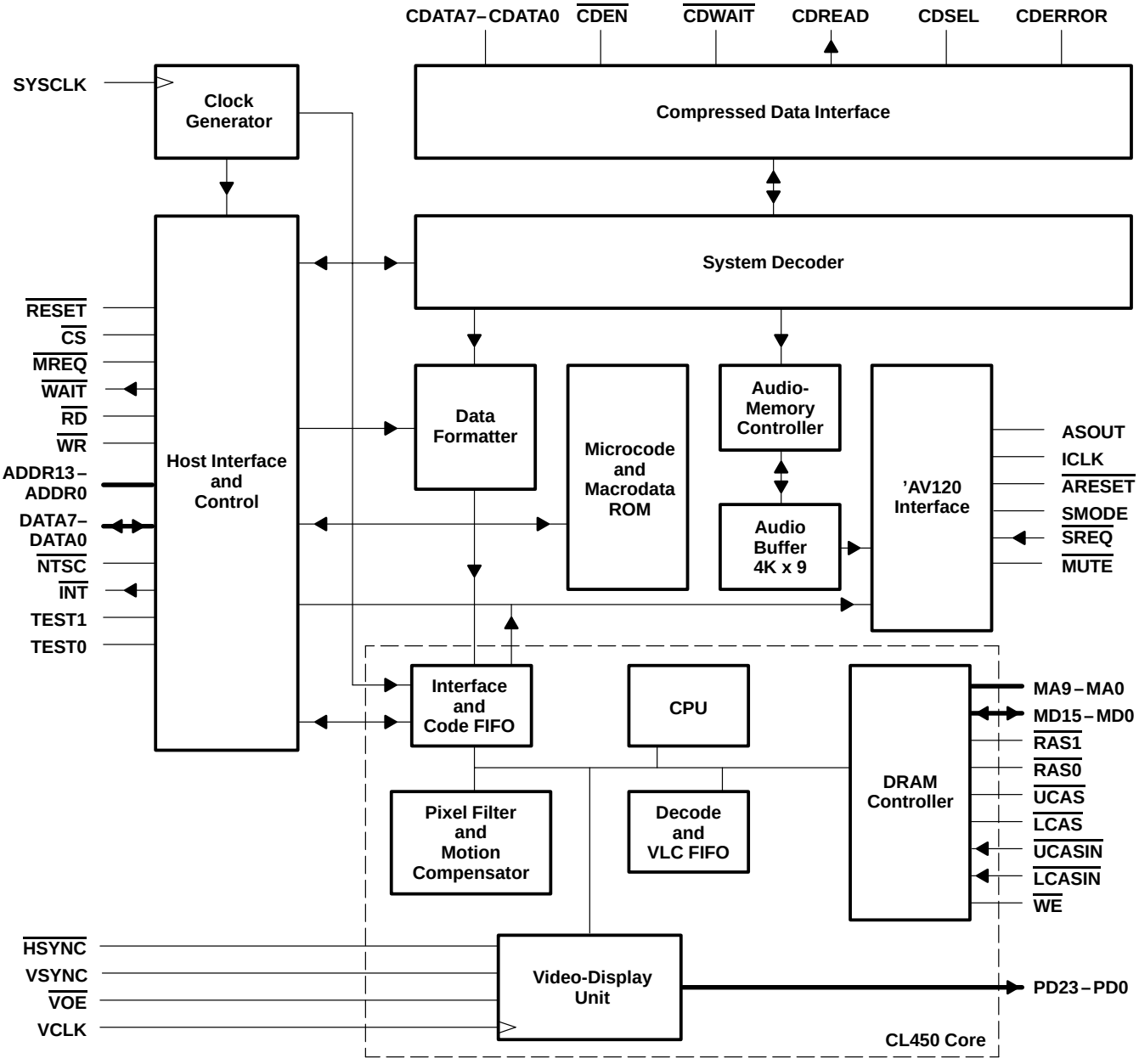


Figure 1. Functional Block Diagram

normal-play-mode operation

The ’AV220 is automatically set to normal-play mode upon completion of all reset, fast, and still operations. In normal-play mode, the ’AV220 decodes video streams with the video-stream identification (ID) selected in the VID_STRM_ID register. In still mode, the ’AV220 decodes streams with a video-stream ID of either 1 or the ID selected in the VID_STRM_ID register.

The ‘AV220 decodes the audio-stream ID selected in the AVD_STRM_ID register. The default audio- and video-stream ID is 0.

fast-forward and fast-reverse operation

Fast forward and fast reverse are done by displaying Intra-frames (I-frames) only with the host skipping to the next or previous I-frame at controlled intervals. The location of the next and previous I-frames are normally encoded in the user-data field associated with each I-frame and this information can be used by the host to control the process.

For fast-forward or fast-reverse operation, the host sets the FAST register to a 1. The ’AV220 responds with the following control sequence:

Clears the bit-stream input buffer
Disables A/V synchronization
Mutes the audio
Looks for the next I-frame in the input data stream
Generates an interrupt when the I-frame is found (if enabled)
Generates an interrupt if there is user data present (if enabled)
Places the 18-byte user data field into the user-data register
Decodes and displays the I-frame
Generates an interrupt when the I-frame is decoded (if enabled)
Looks for the next I-frame

The host skips to the CD-ROM sector indicated in the user-data register for the next I-frame after receiving the I-frame decoded interrupt. Waiting for this interrupt ensures that the current frame is completely decoded.

The above sequence is repeated as required. To return to normal operation, the host clears the FAST register.

still-mode operation

Normal-resolution still-picture display is also supported and controlled by the STILL_MODE register. It is done in a manner similar to the fast mode in that only I-frames are displayed, but the process is not continuous; the host controls stepping from one still to the next, and the audio is not muted. Muted audio can be selected through the ’AV220 DISPLAY_MODE register.

For still-mode operation, the host sets bit 1 of the STILL_MODE register to a 1. The ’AV220 responds with the following control sequence:

Clears the bit-stream input buffer
Disables A/V synchronization, but does not mute the audio
Finds and displays the next I-frame found
Enters the pause mode while holding the display

still-mode operation (continued)

To advance to the next frame, the host sets bit 0 of the STILL_MODE register to a 1. The ’AV220 then performs the following:

Finds and displays the next I-frame
Clears bit 0 of the STILL_MODE register
Enters the pause mode

Repeat the sequence as required. To terminate still mode, the host clears bit 1 of the STILL_MODE register.

’AV220 control registers

The ’AV220 is controlled by the host microprocessor by accessing 14 control registers listed in the following table. The registers are initialized to the default values when the ’AV220 is reset.

REGISTER NAME	ADDRESS (HEX)	LENGTH (BITS)	DESCRIPTION	DEFAULT VALUE (HEX)	ACCESS MODE
AUD_STRM_ID	2429	5	Selects the audio-stream ID to decode	0	W/R
DISPLAY_MODE	2423	2	Controls video- and audio-display modes	0	W/R
DMA_MODE	242C	5	Allows psuedo-DMA control of the ’AV220	0	W/R
DRAM_SEL	2428	6	DRAM partition select	0	W/R
FAST	2421	1	Selects fast-forward/fast-reverse mode	0	W/R
INTERRUPT	2425	7	Interrupt requests	0	R
INTR_EN	2426	7	Interrupt masks	0	W/R
RESET	2424	1	Software reset	0	W/R
STILL_MODE	2422	2	Controls still-picture display and advancement	0	W/R
STREAM_EN	2420	1	Enables direct data write to the 4-Mbit DRAM	0	W/R
SYNC_CTL	242B	8	Synchronization control	78	W/R
USERDATA [17:0]	2600-11	8 (each)	User data stored in RAM, byte addressable	N/A	R
VERSION	2427	8	Device version number		R
VID_STRM_ID	242A	4	Selects the video-stream ID to decode	0	W/R

AUD_STRM_ID, audio-stream ID select (2429h)

This register sets the audio-stream ID to decode. The MPEG-1 specification allows for 32 different audio stream IDs, all of which are supported with the ’AV220. The default is audio-stream ID zero.

DISPLAY_MODE, 1:0, video- and audio-display modes (2423h)

Bit 0 : 0 = Normal operation
1 = Picture blank

Bit 1: 0 = Normal operation
1 = Audio mute

Data is consumed at the normal rate when muting and/or blanking.

DMA_MODE, DMA control (242Ch)

This register allows pseudo-DMA control of the ’AV220. Pseudo DMA is DMA transfers with flow control via ’AV220 interrupts and registers. The DMA_MODE register’s primary use is with the ’AV220 SANYO transfer mode. The ’AV220 SONY mode is an on-demand mode and does not necessitate the use of this register. The DMA_MODE register is defined as follows:

BIT NO.	FUNCTION	DEFAULT VALUE
4	DMA-mode enable. When set pseudo-DMA control is enabled.	0
3:1	DMA-block size. Sets the amount of free space checked within the ’AV220 audio buffer. Sizes available are: 000 : no selction 001 : 0.5 Kbytes 010 : 1 Kbytes 011 : 1.5 Kbytes 100 : 2 Kbytes 101 : 2.5 Kbytes 110 : 3 Kbytes 111 : 3.5 Kbytes	000
0	DMA done. Set by the host when the current DMA operation is complete.	0

To operate in the pseudo-DMA mode, the DMA request interrupt must be enabled (bit 7 of INTR_EN), the DMA mode must be enabled (bit 4 of DMA_MODE), and the desired DMA-block size is selected (bits 3:1 of DMA_MODE). When the ’AV220 wants MPEG data a DMA_request (interrupt) is generated. When the host services the ’AV220 interrupt, it inquires on the ’AV220 video-buffer fullness using the steps listed below. After calculating the amount of room left in the buffer, the host determines if room is available for the desired DMA block size. If so, then a new block of MPEG data can be transferred using a host DMA mechanism. These DMA blocks can be transferred at the maximum transfer rate; that is, CDREAD occurs immediately after $\overline{\text{CDEN}}$ assertion.

To inquire on the video-buffer fullness, the following two writes must be performed. Two bytes are then read, which is the buffer fullness.

	ADDRESS	DATA	
1.	2088	w	0B
2.	2089	w	00
3.	208C	r	low byte
4.	208D	r	high byte

DRAM_SEL, DRAM page select, 5:0 (2428h)

DRAM_SEL selects one of 64 8-K DRAM pages and acts as the six most significant bits of the DRAM address for reads or writes. This register allows full random access to the DRAM. DRAM access takes multiple clock cycles.

FAST, fast-forward/fast-reverse mode (2421h)

0 = Normal operation
1 = Fast-forward/fast-reverse mode. The bit-stream buffer is flushed, PTS checking is disabled, only I-frames are displayed, and audio is muted.

FAST, fast-forward/fast-reverse mode (2421h) (continued)

When this register is set to 1, the device clears the input buffers, mutes the decoded audio output, and decodes/displays only I-frames. The user data associated with each I-frame is placed in the USERDATA registers. The user data normally contains pointers to the next/previous I-frame on the CD. An interrupt is generated when an I-frame is found and also when the I-frame is decoded (if enabled). This allows the host to skip on the CD to the sector containing the next I-frame. The user must not set the FAST and STILL_MODE registers to 1 at the same time.

INTERRUPT, interrupt-request register, 7:0 (2425h)

The interrupt register shows which interrupt caused the interrupt request. This is a read-only register; the interrupts are cleared when the host reads this register.

BIT NO.	FUNCTION
7	DMA request
6	Time-out error, a reset is required
5	I-frame decoded, still or fast mode only
4	I-frame found, still or fast mode only
3	User data found, still or fast mode only
2	DRAM full, streaming data mode only
1	MPEG data error
0	Bit-stream buffer underflow

INTR_EN, interrupt-enable register, 7:0 (2426h)

The INTR_EN register enables any interrupts that are needed by the host. A 1 in any bit position enables the corresponding interrupt in the INTERRUPT register. A 0 masks the interrupt. After reset, no interrupts are enabled.

RESET, reset the decoder (2424h)

0 = Normal operation
1 = Resets the video and audio. Clears all buffers, resets the video-decoder core, downloads microcode, and initializes registers. This bit is cleared by the 'AV220 at the completion of the reset cycle. Writing a 1 to this register is equivalent to asserting $\overline{\text{RESET}}$; however, $\overline{\text{RESET}}$ must be asserted to initialize the device on power up.

The host cannot read or write registers or memory until the internal reset sequence is completed, requiring up to 25 ms. If a register access is attempted during the reset period, the chip activates the $\overline{\text{WAIT}}$ line until the reset is completed. The CD interface does not accept data during this time. The 'AV220 activates CDREAD when the reset sequence is completed.

STILL_MODE, still-picture-display mode, 1:0 (2422h)

Bit 0: 0 = Normal operation
1 = Frame advance. Displays the next still picture (I-frame), then clears this bit.

Bit 1: 0 = Normal operation
1 = Still-picture mode. After the bit-stream buffer is flushed, displays the first I-frame only.

STILL_MODE, still-picture-display mode, 1:0 (2422h) (continued)

This register controls the display of normal-resolution still pictures. When bit 1 is set to 1, the input buffer is cleared, audio synchronization (PTS comparison) is disabled but the audio is not muted, and the first I-frame found is displayed. The 'AV220 enters a pause mode until bit 0 is set to 1 by a host, indicating a request to display the next I-frame. This bit is then cleared by the device. To return to normal play mode, bit 1 must be cleared. The user must not set the FAST and STILL_MODE registers to 1 at the same time.

STREAM_EN, stream enable (2420h)

0 = Normal operation
1 = Enables streaming data write from CDATA to the 4M-bit DRAM, starting at address 0. The data should not be sent until 600 ns after the write to this register is completed. This register must be cleared after the last data is written.

This register controls direct, high-speed data write from the CD-ROM decoder to the video-buffer DRAM. When set to 1, the device resets itself. The data on the compressed-data input is written into consecutive locations in the DRAM starting at address 0. Direct write stops when either this register is cleared by the host or the memory is full. The addresses do not roll over. A memory-full interrupt is also generated (if enabled). After the STREAM_EN bit returns to 0, the written data can be randomly accessed via the host interface. Microcode and working buffers are overwritten during this operation, and high-speed memory writes must be followed by a reset after the data is processed by the host.

SYNC_CTL, synchronization control (242Bh)

This register allows control of the incoming MPEG-stream time stamps. SYNC_CTL allows modification of the interval at which incoming SCR values (extracted from the incoming MPEG stream) are used to update the internal 90-kHz counter used for synchronization. This register also allows both audio and video synchronization to be disabled. The default value works well for most applications. For problem CDs, this register may need to be set to 34h or some other value. Video-only systems may require synchronization to be disabled to achieve the proper play rate. The SYNC_CTL register is defined as follows:

BIT NO.	FUNCTION	DEFAULT VALUE
7:6	Don't care	01
5	Audio-synchronization enable. When set enables audio synchronization; when cleared audio synchronization is disabled (PTS values are not sent to the 'AV120).	1
4	Video-synchronization enable. When set enables video synchronization; when cleared video synchronization is disabled (PTS values are not sent to the video core).	1
3	Don't care	1
2	1SCR – When set, the 'AV220 uses only the first SCR time stamp after a change in the PLAY mode (e.g., play to pause, still to play, etc.). SCRs that occur later in the MPEG stream are ignored and do not update the internal 90-kHz counter. Bits 1:0 have no affect when bit 2 is set. When bit 2 is cleared, bits 1:0 determine the SCR update interval.	0
1:0	SCR update control bits. Controls the rate at which incoming SCRs update the internal 90-kHz counter after the 1st SCR is received by the 'AV220. 00 : 720 mS (min) between SCR updates 01 : 360 mS (min) between SCR updates 10 : 180 mS (min) between SCR updates 11 : 90 mS (min) between SCR updates	00

USERDATA [17:0], user-data registers, 7:0 (2600-2611h)

This 18 bytes of user data is byte accessible in random order. When in fast mode, the first 18 bytes of user data associated with each I-frame is extracted and stored for the host to read out. A user-data interrupt is generated (when enabled). Stored data is overwritten when new user data is found and, if $\overline{INT}$ is low (previous interrupt not serviced), it remains low.

VERSION, device-version register, 7:0 (2427h)

Contains the version number of the ’AV220. This is a read-only register.

VID_STRM_ID, video-stream ID select (242Ah)

This register sets the video-stream ID to decode. The MPEG-1 specification allows for 16 different video-stream IDs, all of which are supported with the ’AV220. The default is video-stream ID zero. In still-mode, the ’AV220 decodes streams with ID = 1 or the value of VID_STRM_ID is decoded by the ’AV220 video decoder.

memory map

The memory map of the ’AV220 is shown in Figure 2.

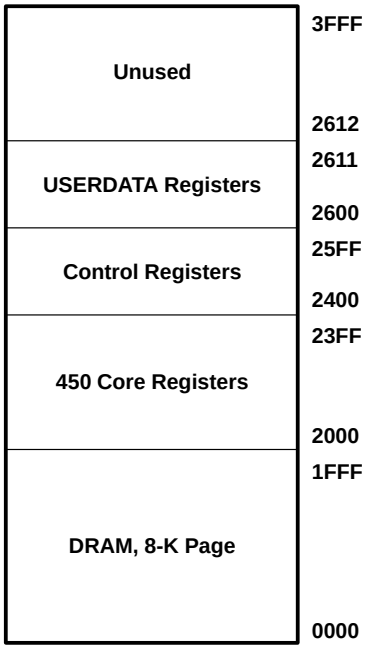


Figure 2. TMS320AV220 Memory Map

error handling

The CDERROR input signals an error in the compressed-data input stream. If the error is in the video portion of the input stream, the ’AV220 handles the error by either blanking or repeating the frame. If the error is in an audio frame, the ’AV220 instructs the TMS320AV120 to mute the offending frame. This is accomplished by sending a zero value PTS to the ‘AV120.

video data (GOPs), audio-frame data, and audio bypass

The ’AV220 decodes full MPEG-1 system streams (pack layer) and MPEG-1 packet streams. In order to decode non-packetized data [i.e., a video sequence (group of pictures, GOPs) or for the ’AV220 to pass audio-frame data or PCM data to the ’AV120], a packet header must precede the data. The packet headers for video and audio data, respectively, are 00 00 01 E0 XX XX FF 0F [data] and 00 00 01 C0 XX XX FF 0F [data], where XX XX is the data length plus two bytes and [data] is the video or audio data. Since the data length is represented by two bytes a header needs to precede at most every 64K minus two bytes of data. For reference, related MPEG-1 start codes are listed in the following table.

HEADER TYPE	START CODES (HEX)
Pack	00 00 01 BA
Video packets	00 00 01 E0 thru 00 00 01 EF
Audio packets	00 00 01 C0 thru 00 00 01 DF
Video sequence (GOPs)	00 00 01 B3

MPEG decoding with the ’AV220/’AV120

Implementation of a decoding engine with the ’AV220/’AV120 is a fairly straight-forward process, but a few points must be noted. In most consumer applications, such as video CD or Karaoke playback systems, a CD-ROM decoder receives MPEG-system data from the CD-ROM transport mechanism and forwards the data onto the ’AV220. The popular Sanyo and Sony CD-ROM decoders contain a FIFO buffer to allow for ’AV220 rate variations. In applications such as these, the receive rate is approximately constant at or about 1.2 Mbit/s to 1.5 Mbit/s. The ’AV220 does not accept data at an exact constant rate. The receive-data rate is slowed slightly when processing system or packet headers. These small rate variations are handled by the logic upstream of the ’AV220.

In other applications such as computer systems, a CD-ROM decoder is not necessarily used. CD data is usually read by a system mechanism and data is stored in the main computer memory. MPEG data is then transferred to the ’AV220 decoder under the main CPU or DMA control. In these circumstances, the MPEG data rate is not constant but rather of a bursty nature. One problem with bursty data is that it potentially could fill the ’AV220 internal buffers. When this occurs, data is only accepted as space becomes available. If the ’AV220 buffers are filled while receiving audio MPEG data, delays may take up to 30 ms for subsequent bytes; if the receiving data is video MPEG data, delays may take from tens to several hundred ms. These delays are short term and depend on the MPEG data and the requirements of the stream-decoding mechanism. These variations can be ignored if the SONY (on-demand) transfer mechanism is used, but if the SANYO mechanism is used, the system must ensure that these internal buffers are not overfilled or make provision for these long delays. If the SANYO mode is used in computer systems, it is recommended that the psuedo-DMA method be used (see DMA_MODE register for details about this mechanism).

Another problem with bursty environments is correlation of audio and video time stamps with the MPEG data display. The default values of the ’AV220 work well for most applications, but in some environments modification of the MPEG-stream time stamp handling may be required (see SYNC_CTL register for details about time stamp control).

interfacing the ’AV220 to the TMS320AV120

The ’AV220 and the ’AV120 MPEG audio decoders are designed to connect directly to each other with no glue logic. The following table shows how to connect the ’AV120 pins. For pins not shown, refer to the ’AV120 documentation. Because the ’AV220 does not send data to the audio decoder at a constant bit rate, the ’AV120 PCM_ERR signal should not be used.

TMS320AV120 PIN	CONNECT TO TMS320AV220 PIN
SIN	ASOUT
ICLK	ICLK
$\overline{\text{SREQ}}$	$\overline{\text{SREQ}}$
SMODE	SMODE
$\overline{\text{MUTE}}$	$\overline{\text{MUTE}}$
$\overline{\text{RESET}}$	$\overline{\text{ARESET}}$
$\overline{\text{HSYNC}}$	GROUND
BYPASS	GROUND
ERR_IN	GROUND

interfacing the ’AV220 to the TMS320AV420

The ’AV220 and the ’AV420 NTSC encoder connect directly to each other with no glue logic. The following table shows how to connect the ’AV420 pins. For pins not shown, refer to the ’AV420 documentation.

TMS320AV420 PIN	CONNECT TO TMS320AV220 PIN
CLK135	VCLK
D23 – D0	PD23 – PD0
$\overline{\text{HSYNC}}$	$\overline{\text{HSYNC}}$
VSYNC	VSYNC

digital-video standards

There are two primary standards for analog-video transmission commonly used: National Television Systems Committee (NTSC) standard and Phase Alternating Line (PAL) standard. The common interchange format (CIF) specification reflects these standards by defining two digital-video formats: 352 pixels × 240 lines × 30 Hz for compatibility with the NTSC standard and 352 pixels × 288 lines × 25 Hz for compatibility with the PAL standard. Because the CIF frame rates are half those of the standard field rates, the ’AV220 displays each decoded CIF picture nominally for two field periods.

video-display unit

The purpose of the video-display unit is to output the decompressed-video data in a form that can be displayed on either a television or a video monitor. To perform these functions, the ’AV220 video-display unit horizontally interpolates decompressed video, converts pixel data from YCbCr to the RGB color space, synchronizes it to the video clock, and outputs it to a display device. The pixels are clocked out by the video clock (VCLK) signal and are synchronized to external devices using the horizontal sync ($\overline{\text{HSYNC}}$) and vertical sync (VSYNC) signals.

In accordance with the MPEG standard, video is compressed using the YCbCr format with Y values ranging from 16 to 235. The ’AV220 automatically converts the YCbCr data to RGB using a matrix that preserves the 220 discrete levels encoded by MPEG, in which 16-16-16 RGB indicates the color black, and 235-235-235 indicates the color white. The equations used to convert to RGB maintain CCIR 601 chromaticity and are as follows:

$$\text{Red} = Y + 1.402 \times Cr$$
$$\text{Blue} = Y + 1.772 \times Cb$$
$$\text{Green} = Y - .334 \times Cb - .714 \times Cr$$

The video-display unit can also be programmed to output PD23–PD0 using the YCbCr format. The following steps must be followed after each reset to configure the ’AV220 to output YCbCr.

1. Poll register at address 2056h until bit 0 is 0.
2. Once a zero is read, the following ten writes must be performed in the order shown below.

WRITE NUMBER	ADDRESS	DATA
1	2088	00
2	2089	00
3	208C	11
4	208D	01
5	2088	01
6	2089	00
7	208C	00
8	208D	00
9	2056	01
10	2057	00

3. The ’AV220 now outputs pixel data in the YCbCr color space.

Figure 3 shows the video-bus connections.

video-display unit (continued)

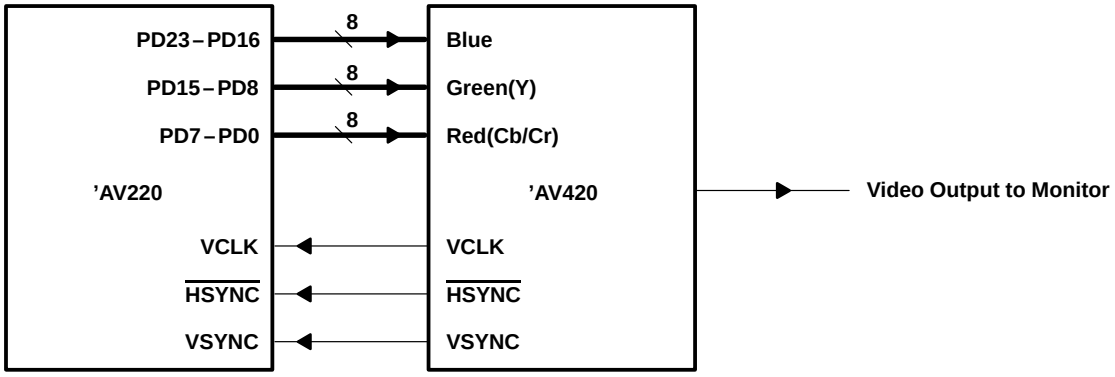


Figure 3. Typical Video-Bus Connections

video output

Figure 4 shows RGB outputs at PD23–PD0 and Figure 5 shows YCbCr outputs at PD15–PD0. The 'AV220 video output is compatible with MPEG, CCIR 601, and CD-I players, and uses a digital output-value range of 16–235 as opposed to the full range of 0–255. YCbCr output can begin with either Cb or Cr.

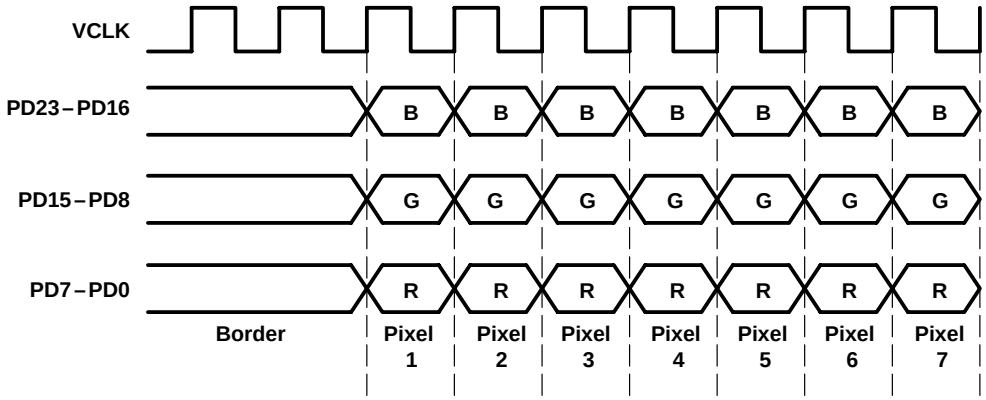


Figure 4. RGB-Display Mode

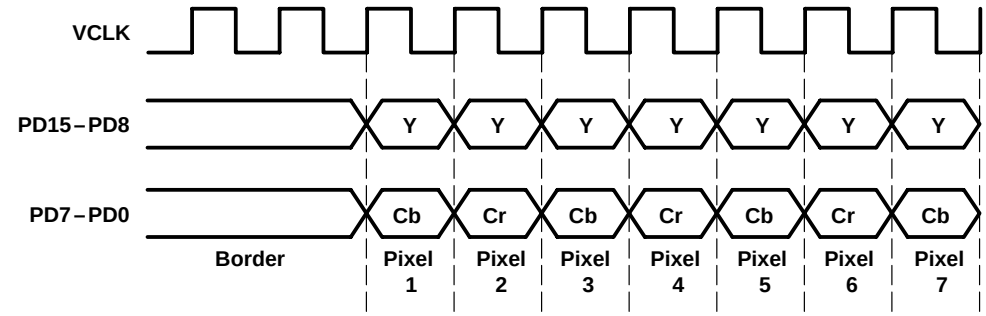


Figure 5. YCbCr-Display Mode

external DRAM

In addition to the ’AV220’s internal registers, the host has direct byte-wide access to the ’AV220’s external DRAM buffer. DRAM is addressed using the contents of register DRAM_SEL and inputs ADDR13–ADDR0. The value stored in DRAM_SEL selects one of 64 8K-DRAM pages. ADDR13–ADDR1 addresses each word in a selected partition and ADDR0 selects either the low byte (ADDR=0) or the high byte (ADDR=1) of the addressed word. The DRAM array is used to store:

Compressed-video data waiting to be decoded by the bit-stream buffer
The decoded video frame that is currently being displayed
Future and past decoded reference frames
Microcode instructions
Bit-stream header parameters

amount, type, and organization of DRAM

The ’AV220 must be connected to 4 Mbits of local dynamic RAM. The DRAM can consist of one 256K × 16 (such as the TMS45160) or four 256K × 4, using 80-ns fast-page-mode DRAMs.

DRAMs that are write per bit or have a write mask should not be used with the ’AV220. More specifically, the DRAM used must ignore the state of the $\overline{WE}$ signal during a CAS-before-RAS refresh cycle. Aside from this restriction, any normal 256K × 16 (or 256K × 4) fast-page-mode DRAM can be used and either 8/10 or 9/9 row/column address configurations can be used.

Figure 6 shows how the memory bus interface is connected when using a 256K × 16 DRAM, and Figure 7 shows how the interface is connected when using 256K × 4 DRAMs.

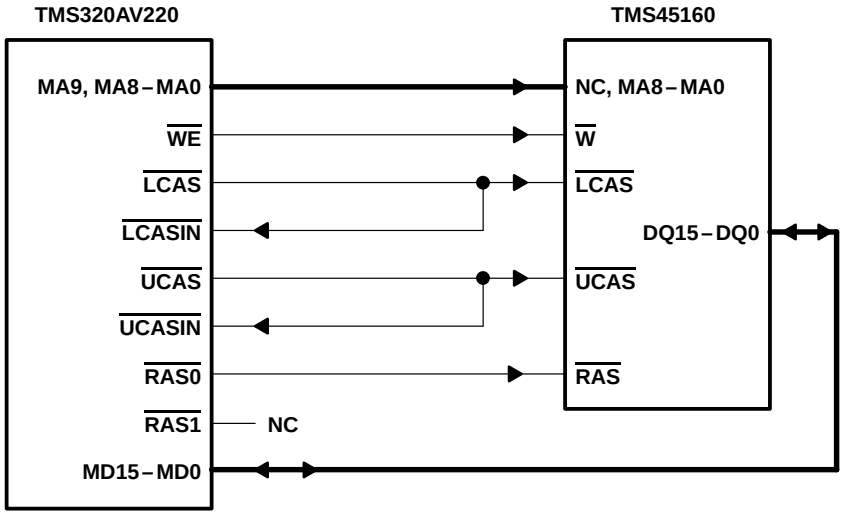


Figure 6. 256K × 16 DRAM Implementation Using the TMS45160

amount, type, and organization of DRAM

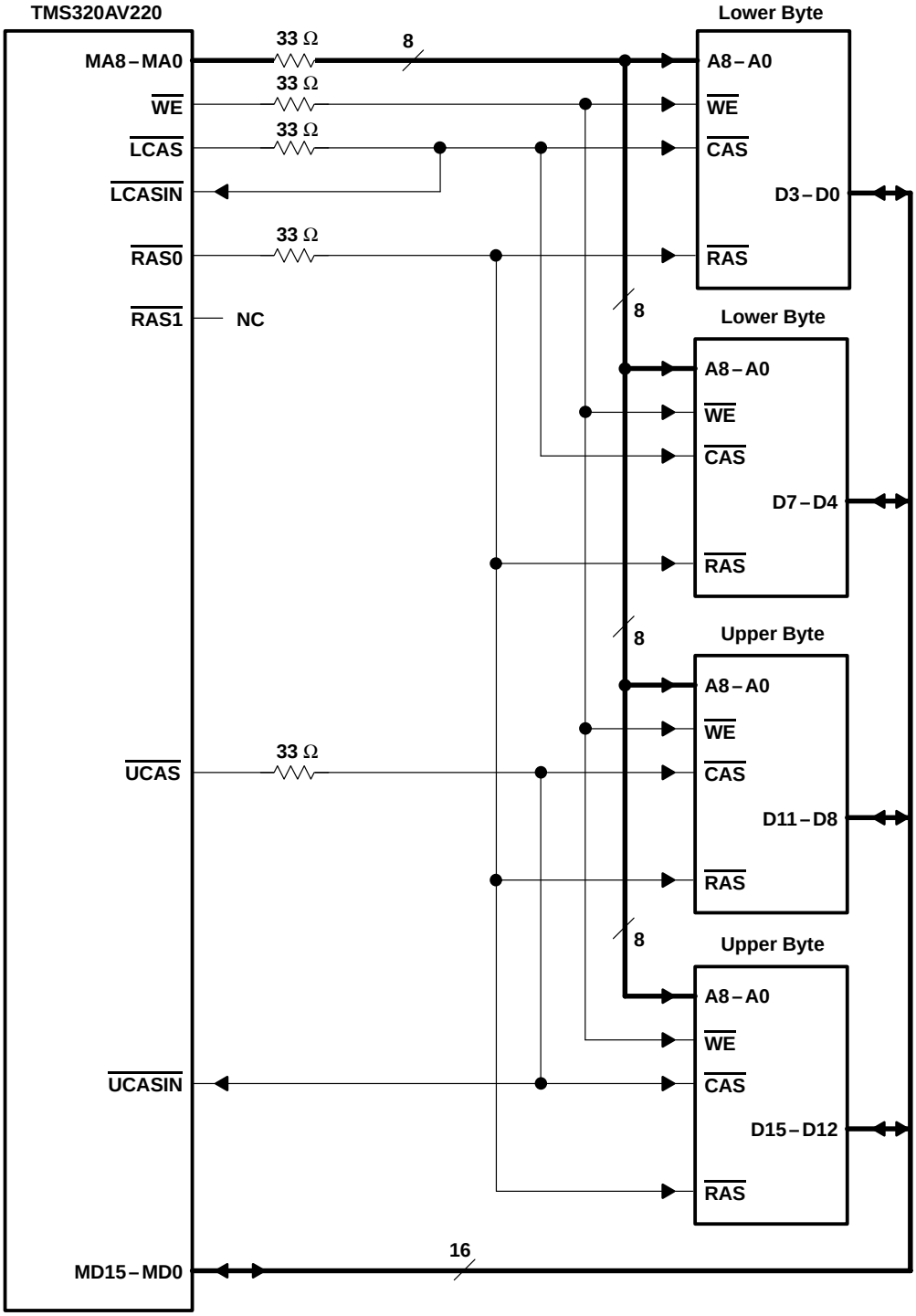


Figure 7. 256K × 4 DRAM Implementation

memory-design guidelines

When designing DRAM arrays for use with the ’AV220, the following guidelines should be followed:

When using 256K×16 DRAMs, connect all ten address lines to the DRAMs. This allows DRAMs with either ten row and eight column address lines or nine row and nine column address lines to be used. The tenth address bit on 256K×16 DRAMs is located on pin 15 of SOJ packages, pin 17 of TSOP packages and pin 25 of ZIP packages. This pin has no effect on DRAMs with nine row and nine column addresses. Memory arrays designed to use 256K×16 DRAMs should use only nine of the ten address lines (MA8–MA0). The ’AV220 supports both of these memory organizations by duplicating column address bit nine in the tenth location of the row address as shown in Figure 8.

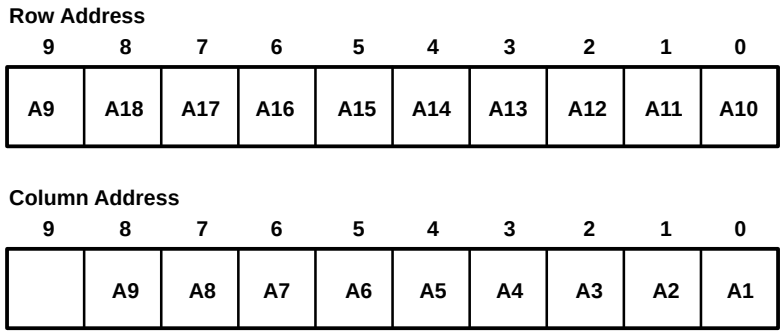


Figure 8. DRAM-Address-Bus Configuration

The $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ signals should be routed from the DRAM mechanically farthest from the ’AV220 to $\overline{\text{LCASIN}}$ and $\overline{\text{UCASIN}}$. This gives the $\overline{\text{CASIN}}$ signal a delay path similar to the path of the DRAM read data to the ’AV220. Since the ’AV220 performs byte-wide writes to DRAM; 256K×16 DRAMs with a single $\overline{\text{CAS}}$ input can not be used.

The elimination of all possible DRAM noise is critical to proper board layout. It is important that the DRAM be placed near the ’AV220. The layout should use terminations and have a clean ground and V_{CC} plane below the DRAM and those portions of the ’AV220 that connect to it. If possible, no other signals or clocks should be passed under the DRAMs or their traces.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 6 V
Input voltage range, V_I	–0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±20 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	VCLK	3.4		V_{CC}+0.5	V
		All others	2.4		V_{CC}+0.5	
V_{IL}	Low-level input voltage		–0.5		0.8	V
I_{OH}	High-level output current				–2	mA
I_{OL}	Low-level output current				8	mA
f_{clock}	Clock frequency, SYSCLK			40	40	MHz
f_{clock}	Clock frequency, VCLK			13.5	14.9	MHz
dt/dV	Input transition (rise or fall)				5	ns/V
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.75 V,	I_{OH} = –2 mA	2.8			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	I_{OL} = 8 mA			0.5	V
I_{OH}	High-level output current, $\overline{WAIT}$ and $\overline{INT}$	V_{CC} = 4.75 V,	V_{OH} = 5.25 V			10	µA
I_I	Input current	V_{CC} = 5.25 V,	V_I = V_{CC} or 0			±10	µA
I_{OZ}	Off-state output current, DATAx, MDx, PDx	V_{CC} = 5.25 V,	V_O = V_{CC} or 0			±10	µA
I_{CC}	Supply current	V_{CC} = 5.25 V,	SYSCLK = 40 MHz		380	500	mA
C_i	Input capacitance	f = 1 MHz			10		pF
C_o	Output capacitance‡	f = 1 MHz			12		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the capacitance at an output or I/O terminal.

timing requirements and switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

host interface, SYSCLK and $\overline{RESET}$ timing

		FIGURE	MIN	MAX	UNIT
t_{su1}	ADDR13–ADDR0 before $\overline{MREQ}$ low	9, 10	15		ns
t_{su2}	$\overline{CS}$ low before $\overline{MREQ}$ low	9, 10	0		ns
t_{su3}	ADDR13–ADDR0 before $\overline{RD}$ low	9	15		ns
t_{su4}	ADDR13–ADDR0 before $\overline{WR}$ low	10	65		ns
t_{su5}	$\overline{WAIT}$ high before $\overline{WR}$ high	10	50		ns
t_{su6}	DATA7–DATA0 before $\overline{WR}$ high	10	50		ns
t_{su7}	$\overline{RESET}$ high before $\overline{MREQ}$ low	13	2		ns
t_{h1}	DATA7–DATA0 after $\overline{WR}$ high	10	0		ns
t_{w1}	$\overline{RESET}$ low	13	300		ns
t_{w2}	SYSCLK high or low	14	10		ns
t_{pd1}	$\overline{MREQ}$ low to $\overline{WAIT}$ low	9, 10		10	ns
t_{pd2}	$\overline{RESET}$ high to CDREAD and $\overline{WAIT}$	13		25	ms
t_d	DATA7–DATA0 before $\overline{WAIT}$ high (read cycle)	9	15		ns
t_v	DATA7–DATA0 valid after $\overline{RD}$ high	9	10		ns

timing requirements and switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted) (continued)

Sony CD-ROM interface timing, CDSEL = 0 (see Figure 11)

		MIN	MAX	UNIT
t_1	$\overline{\text{CDEN}}$ high after CDREAD output high	120		ns
t_2	$\overline{\text{CDEN}}$ low	55		ns
t_3	CDATA before $\overline{\text{CDEN}}$ high	50		ns
t_4	CDATA hold time after $\overline{\text{CDEN}}$ high	20		ns
t_5	CDERROR before $\overline{\text{CDEN}}$ high	50		ns
t_6	CDERROR after $\overline{\text{CDEN}}$ high	20		ns

Sanyo CD-ROM interface timing, CDSEL = 1 (see Figure 12)

		MIN	MAX	UNIT
t_7	$\overline{\text{CDEN}}$ low to CDREAD output low	0		ns
t_8	CDREAD output low time	310		ns
t_9	CDREAD output high time	50		ns
t_{10}	$\overline{\text{CDWAIT}}\downarrow$ after CDREAD output low		80	ns
t_{11}	CDREAD output high after $\overline{\text{CDWAIT}}$ high	50		ns
t_{12}	$\overline{\text{CDWAIT}}$ low time		625	ns
t_{13}	CDATA before CDREAD output high	50		ns
t_{14}	CDATA hold after CDREAD output high	0		ns
t_{15}	CDATA before $\overline{\text{CDWAIT}}$ high	0		ns
t_{16}	CDERROR high before CDREAD output high	50		ns
t_{17}	CDERROR hold after CDREAD output high	0		ns

video bus timing (see Note 2 and Figure 15)

		MIN	MAX	UNIT
f_{clock}	VCLK frequency		14.9	MHz
t_{w3}	VCLK high or low	20		ns
t_{su8}	$\overline{\text{HSYNC}}$ before VCLK high	10		ns
t_{h2}	$\overline{\text{HSYNC}}$ after VCLK high	0		ns
t_{pd3}	VCLK high to PD23–PD0		20	ns
t_{en}	$\overline{\text{VOE}}$ low to PD23–PD0		20	ns
t_{dis}	$\overline{\text{VOE}}$ high to PD23–PD0 (see Notes 3 and 4)		20	ns

NOTES: 2. Inputs switch between 0 V and 3.5 V at 1 V/ns. Measurements are made at 1.5 V. Output load capacitance = 50 pF.
3. Not 100% tested, specified by design and characterization
4. Time at which output achieves the high-impedance condition; not referenced to an output-voltage level

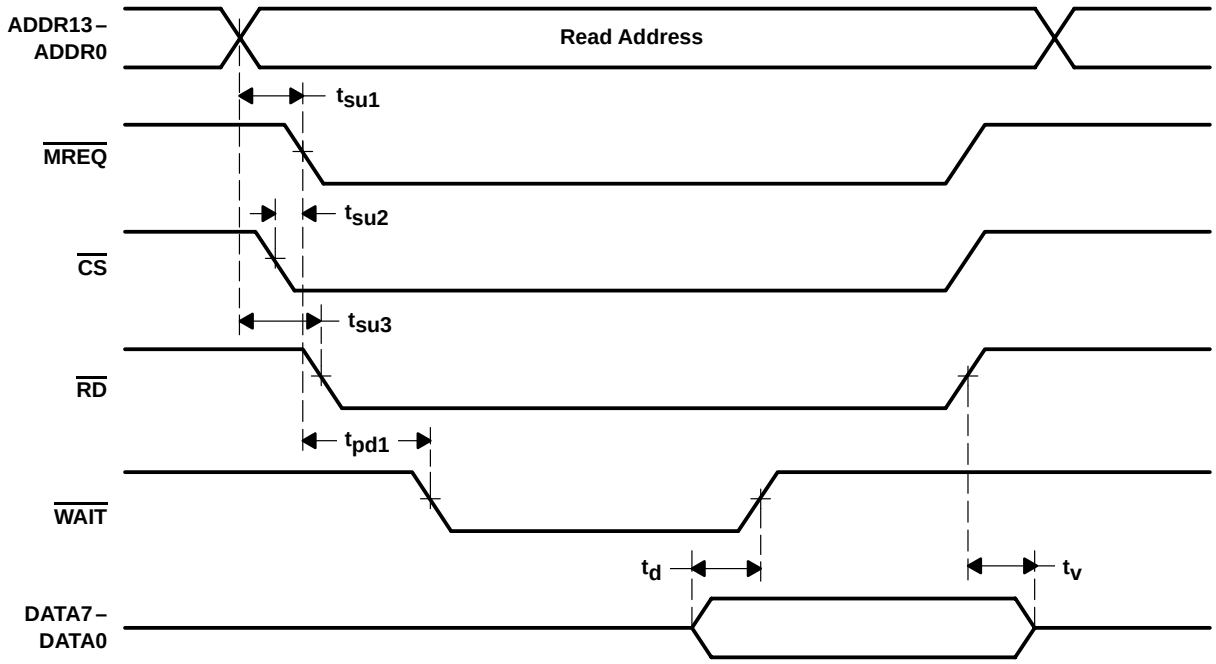


Figure 9. Host-Interface Read Timing

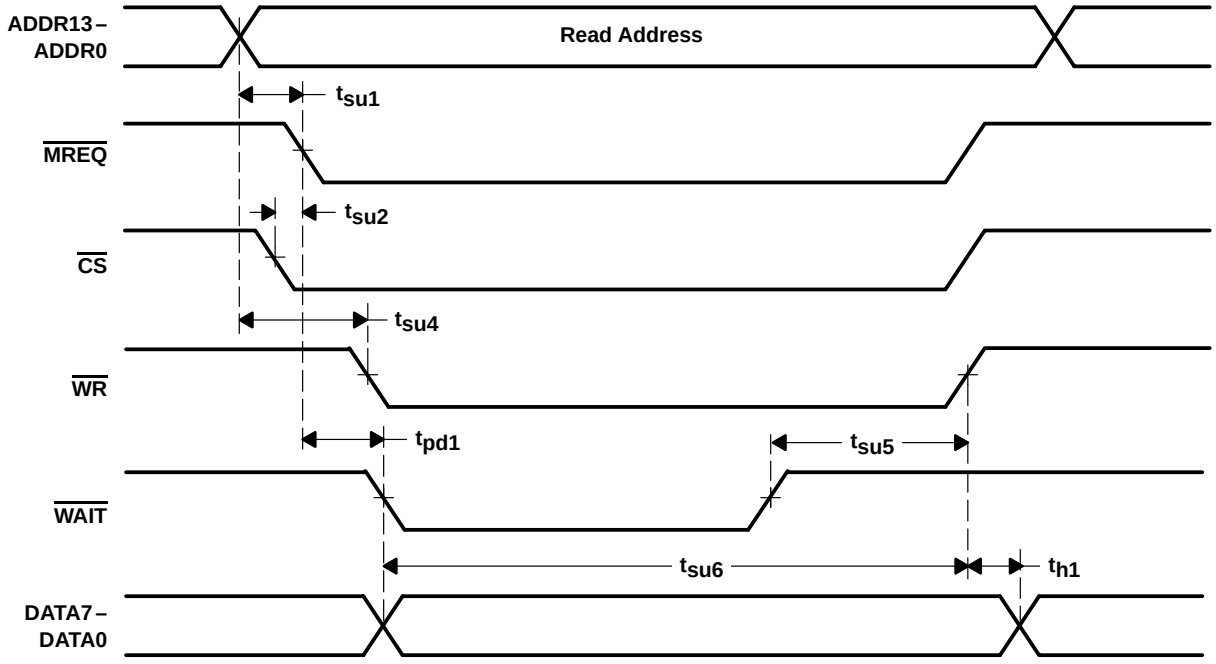


Figure 10. Host-Interface Write Timing

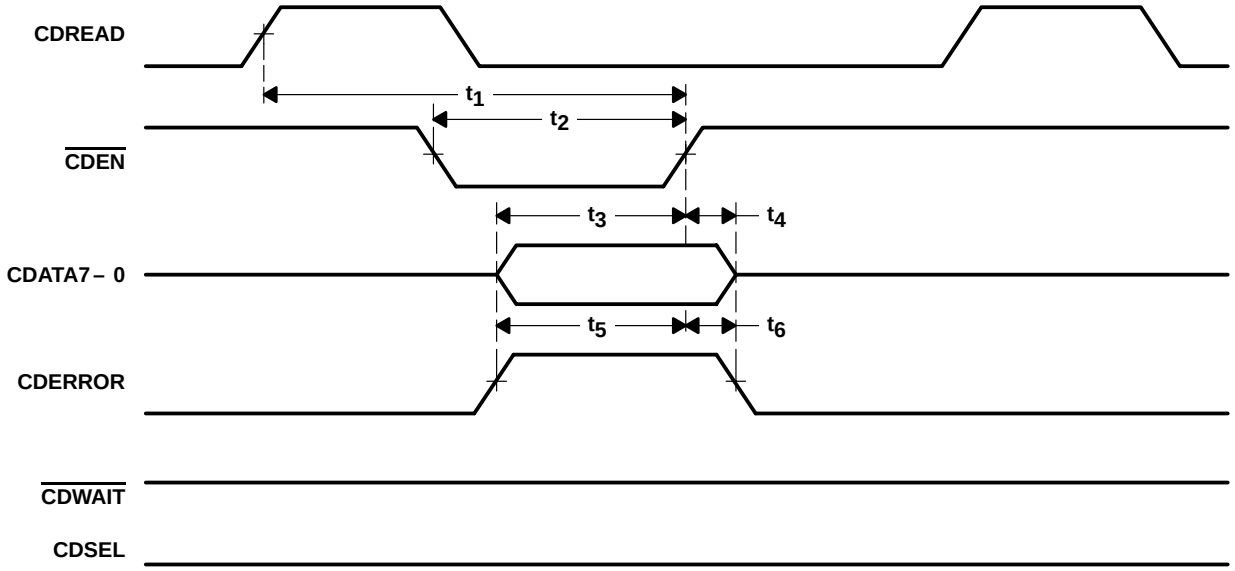


Figure 11. Compressed-Data Input, CDSEL = 0 (Sony) Timing

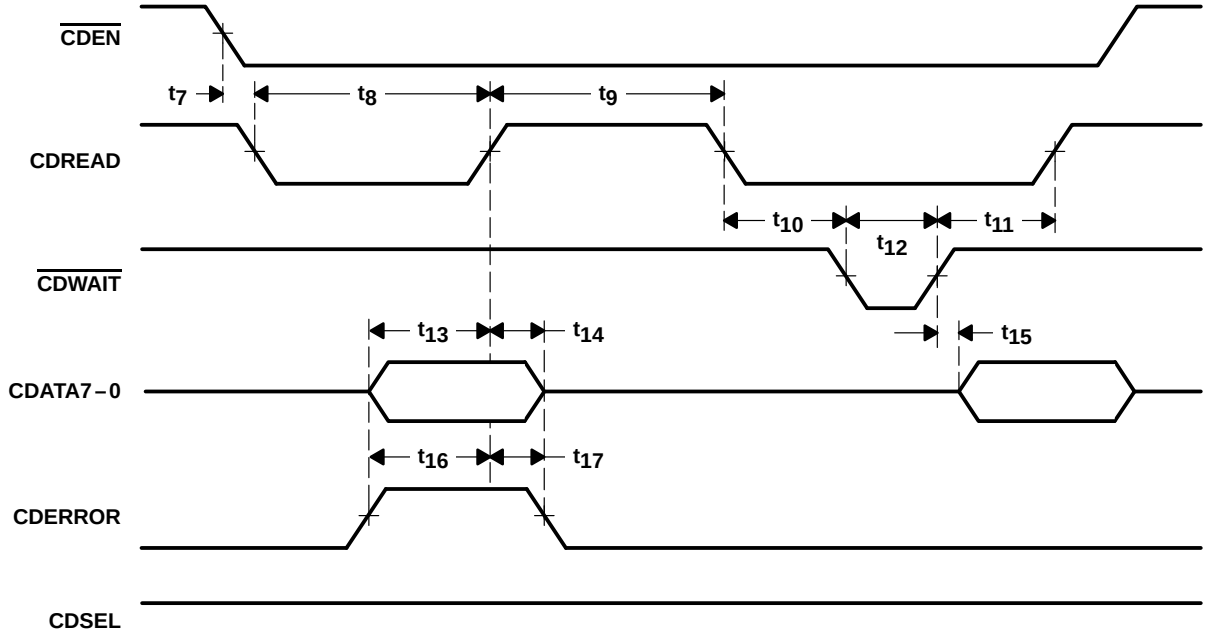
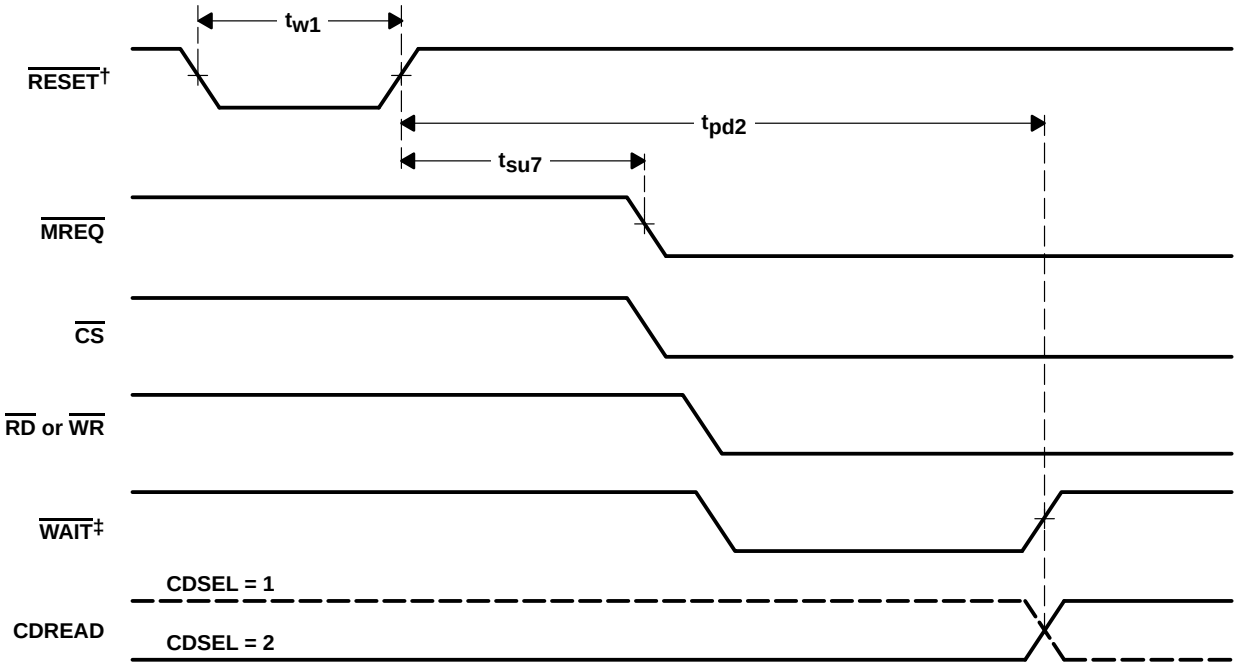


Figure 12. Compressed-Data Input, CDSEL = 1 (Sanyo) Timing



† Setting the RESET register to 1 is equivalent to a RESET pulse.
‡ If a read or write is attempted during the reset sequence, WAIT goes low until the sequence is completed in a maximum of 25 ms.

Figure 13. RESET-Sequence Timing

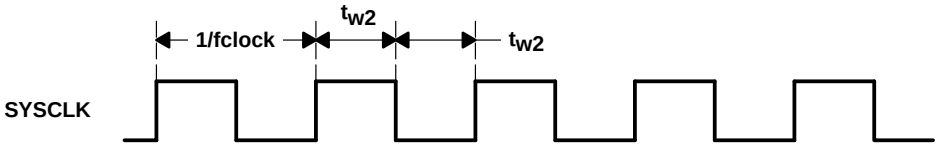


Figure 14. SYSCLK Timing-Diagram Timing

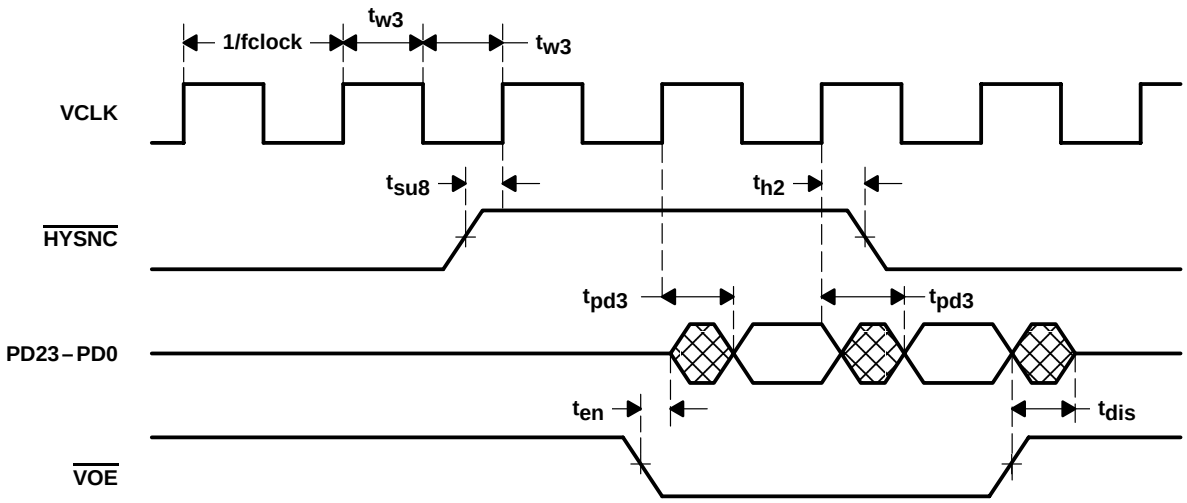


Figure 15. Video-Bus-Inputs Timing

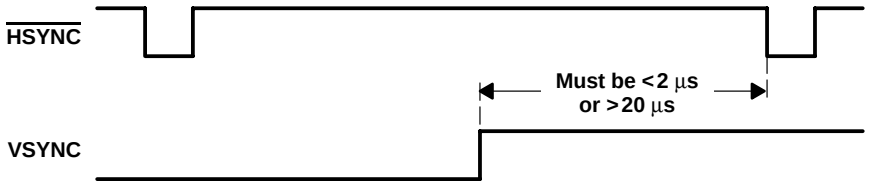


Figure 16. VSYNC Timing Restriction

local-DRAM-bus timing

Local-DRAM-bus timing is specified differently than the other timing parameters. The DRAM interface times are specified at 0.8 V and 2.4 V instead of at 1.5 V. This allows the designer to cross reference 'AV220 timing values to DRAM specifications easily.

timing requirements and switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

local DRAM timing (see Note 5, Figure 17, and Figure 18)

		MIN	MAX	UNIT
t_c	SYSCLK period	25		ns
t_{pd3}	SYSCLK high to $\overline{RAS}$ low (see Note 6)		30	ns
t_{pd4}	SYSCLK high to $\overline{CAS}$ high (see Note 6)		25	ns
t_{pd5}	SYSCLK high to memory data high or low (DRAM write) (see Note 6)		30	ns
t_{pd6}	SYSCLK high to $\overline{WE}$ high or low (see Note 6)		22	ns
t_{pd7}	SYSCLK high to memory address high or low (see Note 6)		24	ns
t_{su8}	Read data setup time before $\overline{CASIN}$ high	5		ns
t_{h2}	Read data hold time after $\overline{CASIN}$ high	5		ns
t_{ASR}	Row address setup time (see Note 5)	t_c-10		ns
t_{DS}	Write data setup time before $\overline{CAS}$ low (see Note 6)	t_c-15		ns
t_{DH}	Write data hold time after $\overline{CAS}$ low (see Note 6)	t_c-10		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low (see Note 6)	t_c-5		ns
t_{RRH}	Read command hold time from $\overline{RAS}$ high (see Note 6)	t_c-15		ns
t_{RCS}	Read command setup time to $\overline{CAS}$ low (see Note 6)	$5t_c-10$		ns
t_{ASC}	Column address setup time to $\overline{CAS}$ low (see Note 6)	t_c-15		ns
t_{CAH}	Column address hold time from $\overline{CAS}$ low (see Note 6)	t_c-10		ns
t_{RAH}	Row address hold time from $\overline{RAS}$ low (see Note 6)	$2t_c-15$		ns
t_{CAS}	$\overline{CAS}$ low time (see Note 6)	t_c-5		ns
t_{CP}	$\overline{CAS}$ high time (see Note 6)	t_c-10		ns
t_{RP}	$\overline{RAS}$ high time (see Note 6)	$3t_c-5$		ns
t_{RAS}	$\overline{RAS}$ low time (see Note 6)	$4t_c-15$		ns
t_{WCS}	Write command setup time to $\overline{CAS}$ low (see Note 6)	$2t_c-15$		ns
t_{WCH}	Write command hold time from $\overline{CAS}$ low (see Note 6)	$2t_c-10$		ns
t_{CAL}	Column address to $\overline{CAS}$ high (see Note 6)	$2t_c-5$		ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay (see Note 6)	$3t_c-15$		ns
t_{CSR}	$\overline{CAS}$ setup time to $\overline{RAS}$ (memory refresh cycle) (see Note 6)	t_c-10		ns
t_{CHR}	$\overline{CAS}$ hold time from $\overline{RAS}$ (memory refresh cycle) (see Note 6)	$3t_c-15$		ns
t_{RPC}	$\overline{RAS}$ high to $\overline{CAS}$ low delay (memory refresh cycle) (see Note 6)	$2t_c-10$		ns
t_{RAL}	Column address to $\overline{RAS}$ high (see Note 6)	$2t_c-10$		ns
t_{CSH}	$\overline{RAS}$ low to $\overline{CAS}$ high (see Note 6)	$4t_c-15$		ns
t_{RHCP}	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge (see Note 6)	$2t_c-5$		ns
t_{RCH}	Read command hold time from $\overline{CAS}$ high	t_c-15		ns

NOTES: 5. Not 100% tested, specified by design and characterization
6. MD15–MD0 are driven only when next cycle is a write.

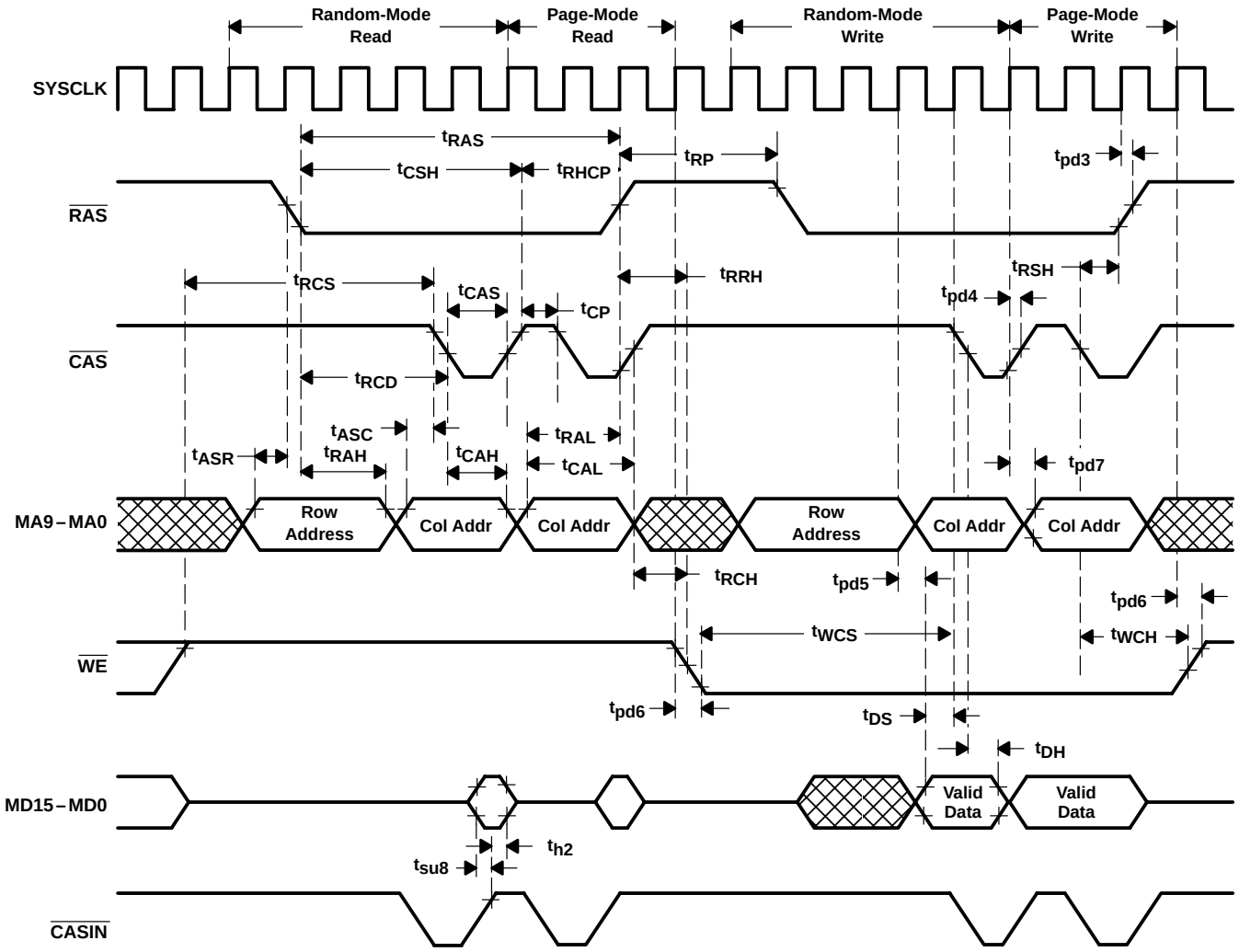
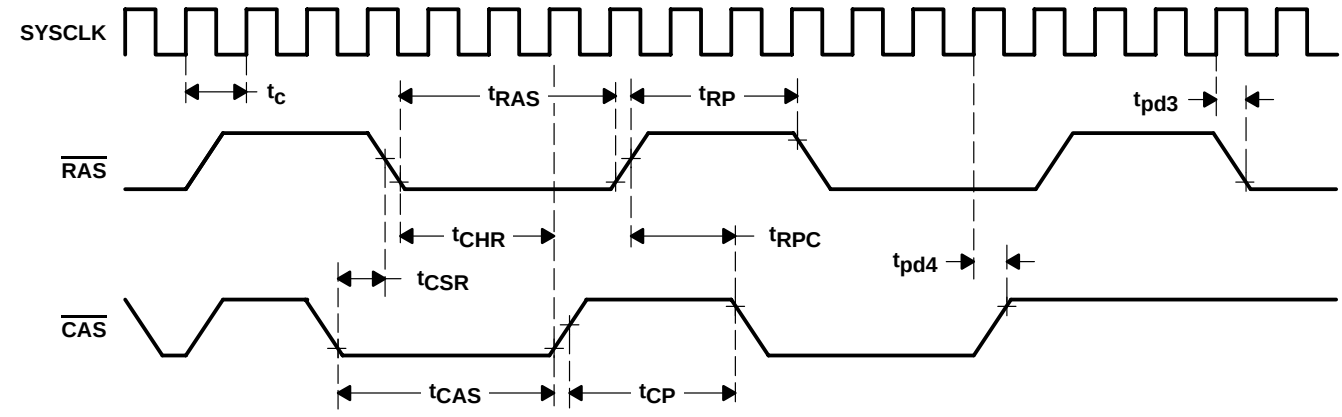


Figure 17. Local-DRAM-Bus Timing



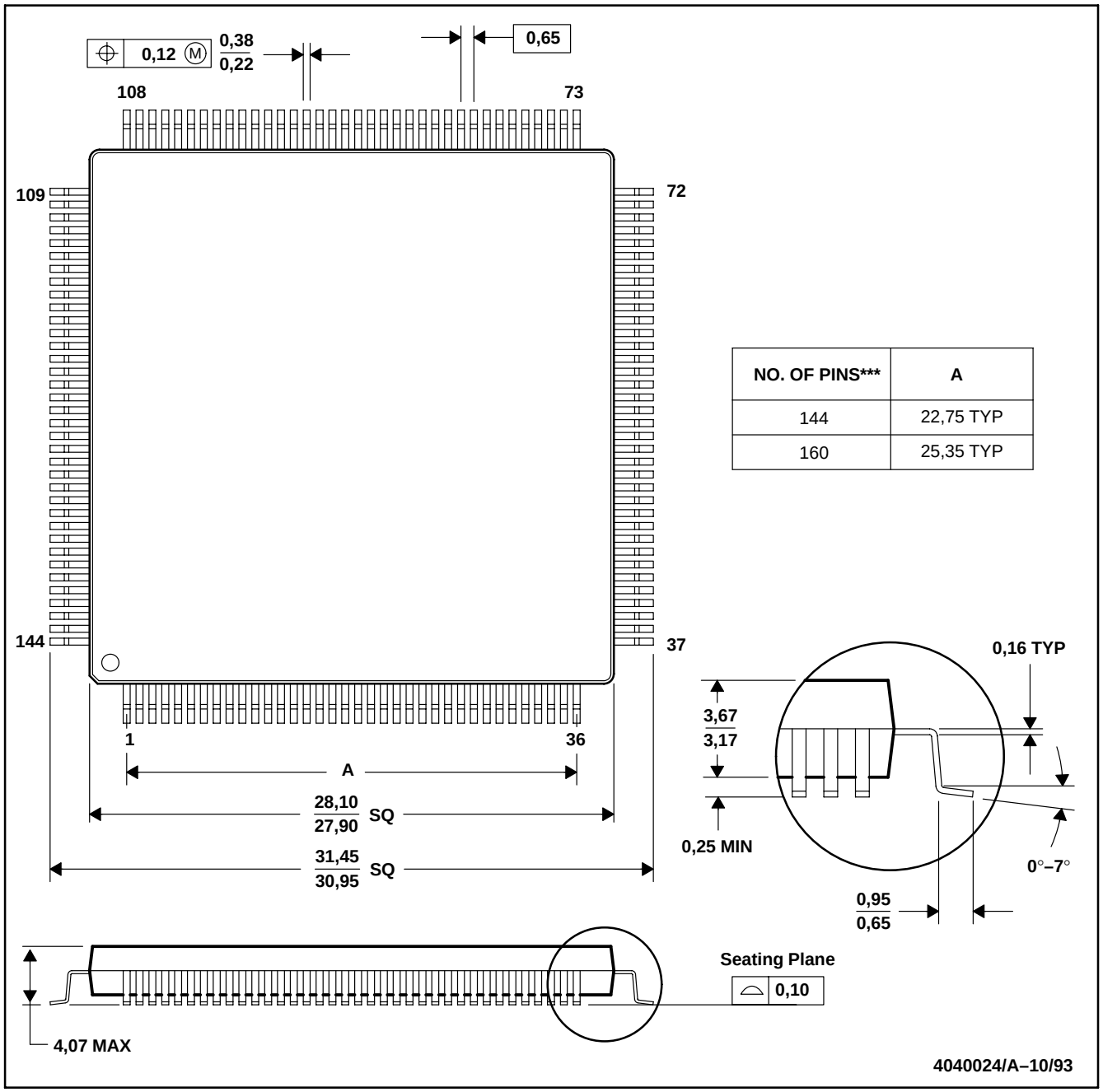
NOTE A: The 'AV220 $\overline{WE}$ signal does not necessarily go inactive during DRAM refreshes. Use DRAMs that do not acknowledge the state of $\overline{WE}$ during DRAM refresh timing (i.e., when $\overline{CAS}$ is asserted while the $\overline{RAS}$ line is inactive).

Figure 18. Local DRAM $\overline{CAS}$-before-$\overline{RAS}$ Refresh Timing

MECHANICAL DATA

PCM/S-PQFP-G* ** **PLASTIC QUAD FLATPACK**

144-PIN SHOWN



NO. OF PINS***	A
144	22,75 TYP
160	25,35 TYP

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-108
D. The 144PCM is identical to 160PCM except for 4 leads per corner that are removed.

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