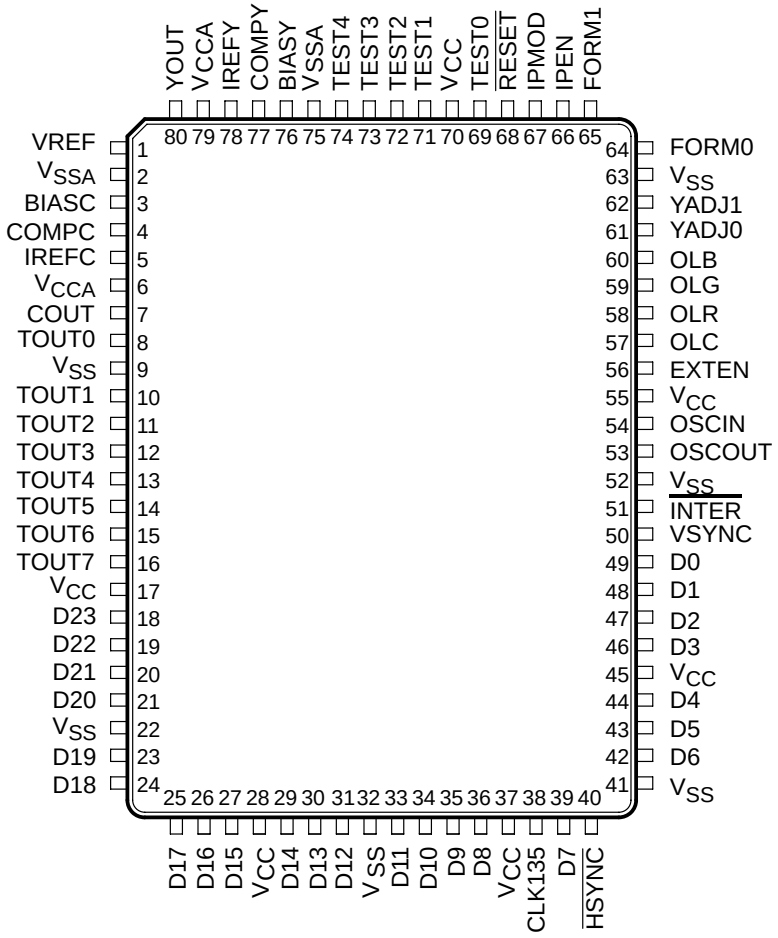
SCSS015A – AUGUST 1994 – REVISED SEPTEMBER 1995

- **Single-Chip Digital NTSC Encoder**
- **Input: RGB, YUV 4:4:4 or YUV 4:2:2**
- **Output: S-Video (Y and C)**
- **Y and C Conform to the RS170A Standard**
- **On-Chip Sync-Signal-Generator Circuitry**
- **Internal and External Synchronization Capability**
- **Interlaced and Noninterlaced Operation**
- **Vertical-Line Interpolation for MPEG-1 Video**
- **Overlay Function for On-Screen Display**
- **Direct Interface to the TMS320AV220 Video CD MPEG Decoder**
- **80-Pin Quad Flat Package**

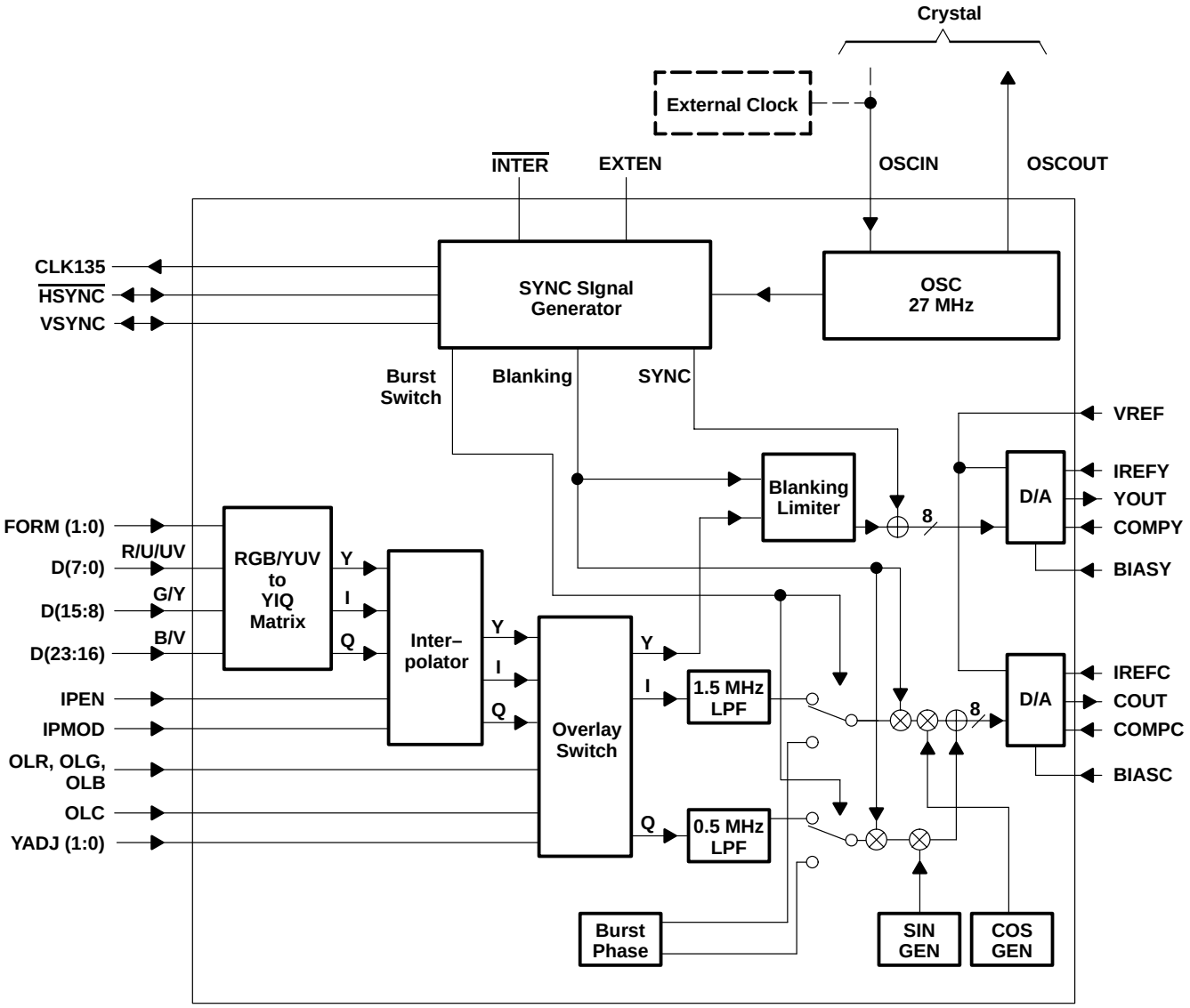
PH PACKAGE
(TOP VIEW)



description

The TMS320AV420 is a video encoder that converts the RGB or YUV pixels to the analog S-video signal using digital-signal-processing techniques. The pixels are input to the ’AV420 using a 13.5-MHz clock. S-video is output from the ’AV420 on two separate RS170A-compatible analog channels, the luminance (Y) channel and the chrominance (C) channel. The ’AV420 operates in either interlaced or noninterlaced mode. The internal and external synchronization capabilities, vertical line interpolation, on-screen display, and direct interfacing features provide the ’AV420 video quality and facilitate video-system design.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
OSCIN	54	I	Oscillator or external clock input
OSCOUT	53	O	Oscillator output
$\overline{\text{RESET}}$	68	I	Reset input
V_{CC}	17, 28, 37, 45, 55, 70	I	Supply voltage
V_{CCA}	6, 79	I	Analog power supply
V_{REF}	1	I	D/A reference voltage input
V_{SS}	9, 22, 32, 41, 52, 63	I	Ground
V_{SSA}	2, 75	I	Analog ground
Analog Video			
BIASC	3	I	C D/A bias-capacitor terminal
BIASY	76	I	Y D/A bias-capacitor terminal
COMPC	4	I	C compensation-capacitor terminal
COMPY	77	I	Y compensation-capacitor terminal
COUT	7	O	C signal output
IREFC	5	I	C reference-current input
IREFY	78	I	Y reference-current input
YOUT	80	O	Y signal output
Digital Video			
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23	49 48 47 46 44 43 42 39 36 35 34 33 31 30 29 27 26 25 24 23 21 20 19 18	I	Digital video input. Data is read at the rising edge of CLK135. FORM1 = L, FORM0 = L (RGB) D[7:0] – R[7:0] input D[15:8] – G[7:0] input D[23:16] – B[7:0] input FORM1 = H, FORM0 = L (YUV 4:4:4) D[7:0] – U[7:0] input D[15:8] – Y[7:0] input D[23:16] – V[7:0] input FORM1 = H, FORM0 = H (YUV 4:2:2) D[7:0] – U, V[7:0] input D[15:8] – Y[7:0] input D[23:16] – Should be connected to ground or to the power supply.
FORM0 FORM1	64 65	I	Input-mode select: FORM1 = L, FORM0 = L – RGB input FORM1 = L, FORM0 = H – Invalid FORM1 = H, FORM0 = L – YUV 4:4:4 input FORM1 = H, FORM0 = H – YUV 4:2:2 input

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
			Overlay Interface
OLB	60	I	Overlay-B signal input
OLC	57	I	Overlay / video-signal select L: Output video signal H: Output overlay signal
OLG	59	I	Overlay-G signal input
OLR	58	I	Overlay-R signal input
YADJ0 YADJ1	61 62	I	Overlay luminance adjust
			Select and Enable
EXTEN	56	I	External / internal sync select L: Internal sync H: External sync
$\overline{\text{INTER}}$	51	I	Interlaced / noninterlaced operation select L: Interlaced mode H: Noninterlaced mode
IPEN	66	I	Vertical interpolation enable L: No vertical interpolation H: Vertical interpolation enabled (interlaced mode only)
IPMOD	67	I	Vertical interpolation mode select L: Vertical interpolation at even field H: Vertical interpolation at odd field
			Test Circuit
TEST0 TEST1 TEST2 TEST3 TEST4	69 71 72 73 74	I	Test-mode pins. Tie these pins to ground for normal operation.
TOUT0 TOUT1 TOUT2 TOUT3 TOUT4 TOUT5 TOUT6 TOUT7	8 10 11 12 13 14 15 16	O	Output for TESTx. Do not connect.
			Video Timing
CLK135	38	O	13.5-MHz clock output
$\overline{\text{HSYNC}}$	40	I/O	HSYNC output (in case EXTEN = 0) HSYNC input (in case EXTEN = 1)
VSYNC	50	I/O	VSYNC output (in case EXTEN = 0) VSYNC input (in case EXTEN = 1)

functional description

input format

The ’AV420 accepts input pixels in 24-bit RGB, 24-bit YUV 4:4:4 or the 16-bit YUV 4:2:2 formats. The input format is controlled by FORM0, FORM1, and the pixels are input into the ’AV420 on the D0–D23 pixel bus. Figure 1 shows the relationship between the input pixel R, G, B, Y and U, V values, and the corresponding analog output waveform luminance and chrominance parameters.

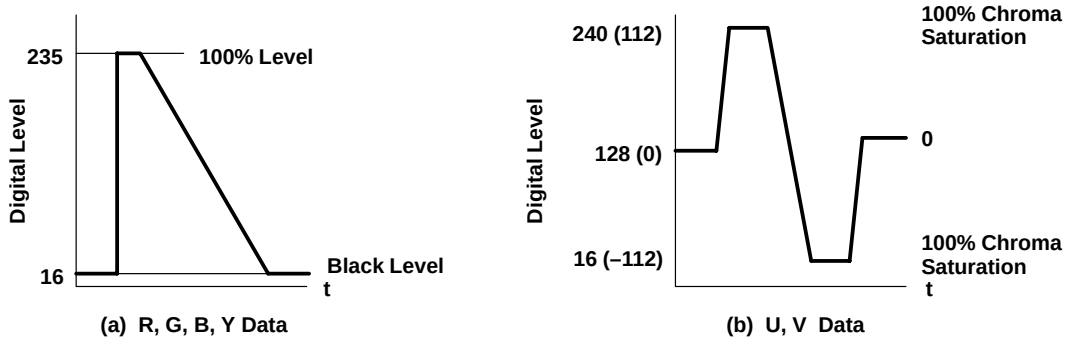


Figure 1. Video Input Data and Waveform Parameters

The first 20 H of each field in the interlaced mode and of each frame in the noninterlaced mode are used for vertical blanking (H is the RS170A line period of 63.56 μs). The active video lines are the subsequent 242.5 lines in the interlaced mode and 242 lines in the noninterlaced mode. The first 128 pixels of each active video line are used for horizontal blanking. The active video pixels are the subsequent 710 pixels. Figure 2 shows the RGB and the YUV 4:4:4 video-input timing. Figure 3 shows the YUV 4:2:2 video-input timing.

		MIN	TYP	MAX	UNIT
t_{su1}	Data setup timing	10			ns
t_{h1}	Data hold timing	10			ns
t_{start}	Data input start timing			$\frac{128}{13.5 \cdot 10^6} \cdot 10^9$	ns
t_{active}	Data input duration	$\frac{710}{13.5 \cdot 10^6} \cdot 10^9$			ns

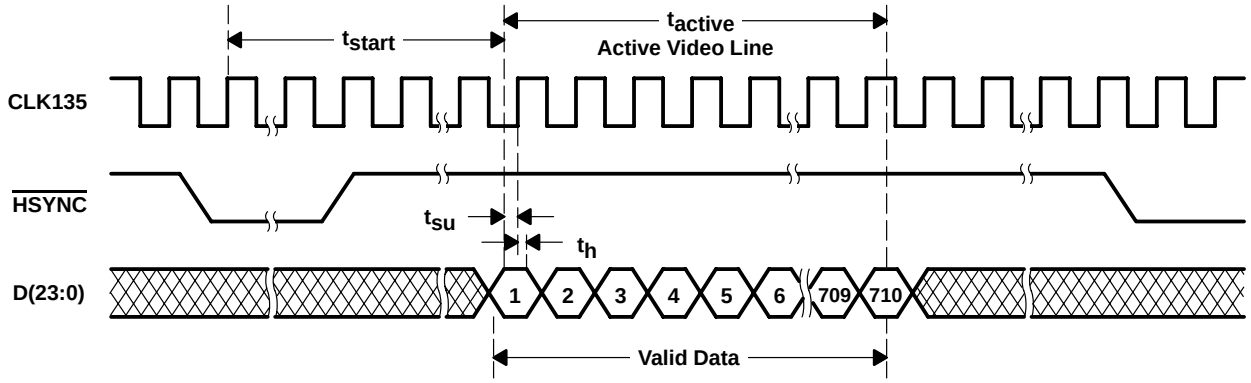


Figure 2. RGB and YUV 4:4:4 Video Data-Input Timing

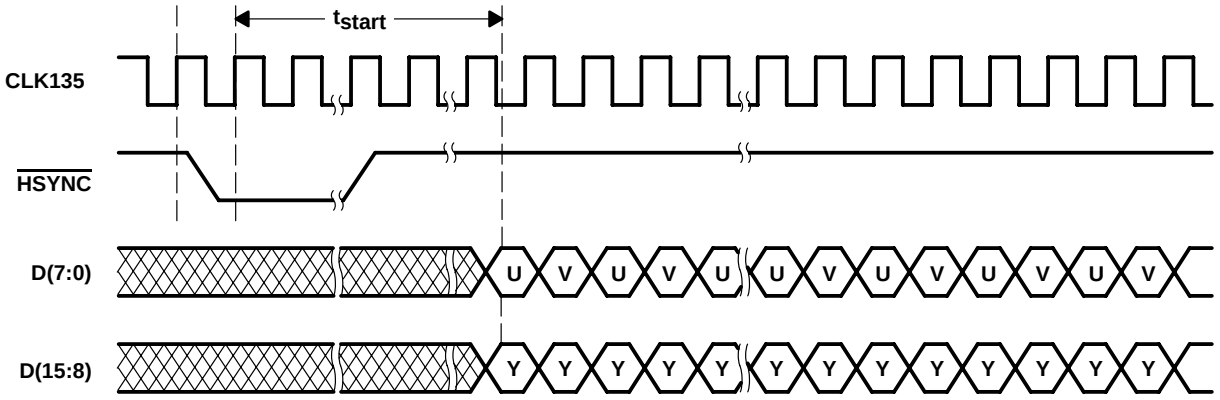


Figure 3. YUV 4:2:2 Video Data-Input Timing

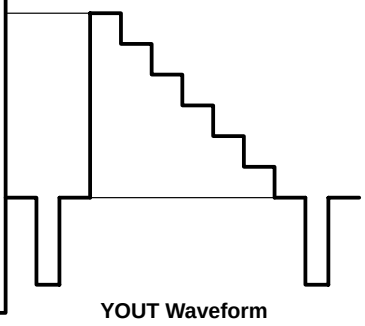
output format and output filter

The ’AV420 outputs the analog video signal in the S-video format on two separate channels, the luminance (Y) channel and the chrominance (C) channel. The Y and the C signals are RS170A-compatible, except for the setup level that is zero IRE units in the ’AV420. The Y and the C signals are output on the YOUT and the COUT terminals under the controls applied through the IREFY, COMPY, BIASY and the IREFC, COMPC, BIASC terminals.

The S-video signal can be used as is or it can be improved by the use of an external signal reconstruction filter. The RS170A composite video signal can be generated by the use of an external Y/C-combining circuit.

The ’AV420 D/As update the video-signal waveform at the 13.5-MHz pixel clock (CLK135) rate. This update rate is sufficient to completely reconstruct the analog-video signal from its samples synthesized inside the ’AV420, because the Y, C, synchronization, and color-burst signals are contained in the 6.75-MHz signal bandwidth. Figure 4 shows the levels of the Y and C signals for 100% saturation NTSC color bars.

DAC Data	V_{YOUT} (mV)	Luma (IRE)
235	4836	100
70	3547	0
4	3031	–40



DAC Data	V_{COUT} (mV)	Chroma (IRE)
245	4914	47
165	4289	20
128	4000	0
91	3711	–20
11	3086	–47

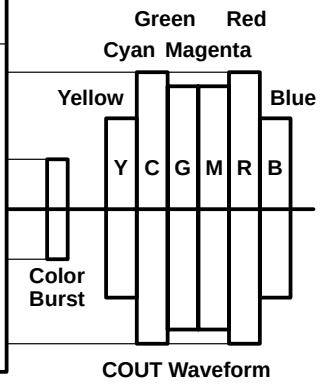


Figure 4. YOUT and COUT for a 100% Saturation Color Bar Signal

As a first-order approximation, a sample-and-hold circuit inside the D/As can be used to reconstruct the video signal. This reconstruction is equivalent to using a zero-order-hold (ZOH) and is not the optimal reconstruction method. The ZOH reconstruction allows the ’AV420 to be used as is.

A better video-signal-reconstruction method involves passing the ’AV420 Y and C signals through low-pass filters (LPFs). This method is based on the exact bandlimited signal reconstruction using an ideal LPF with a bandwidth equal to the signal bandwidth. This method requires two identical external LPF circuits as shown in Figure 5. The example LPFs in Figure 5 limit the bandwidth of the Y and the C signals to the video-broadcast bandwidth of 4.2 MHz.

Figure 5 shows additional ’AV420 analog-interface signals: reference, compensation, and bias, and their external circuits. An external circuit that generates the composite video signal is also shown. This circuit scales and sums the Y and the C signals and forms the composite-video-signal output on one terminal. All component and other parameter values are given in the figure or in the recommended operating conditions section.

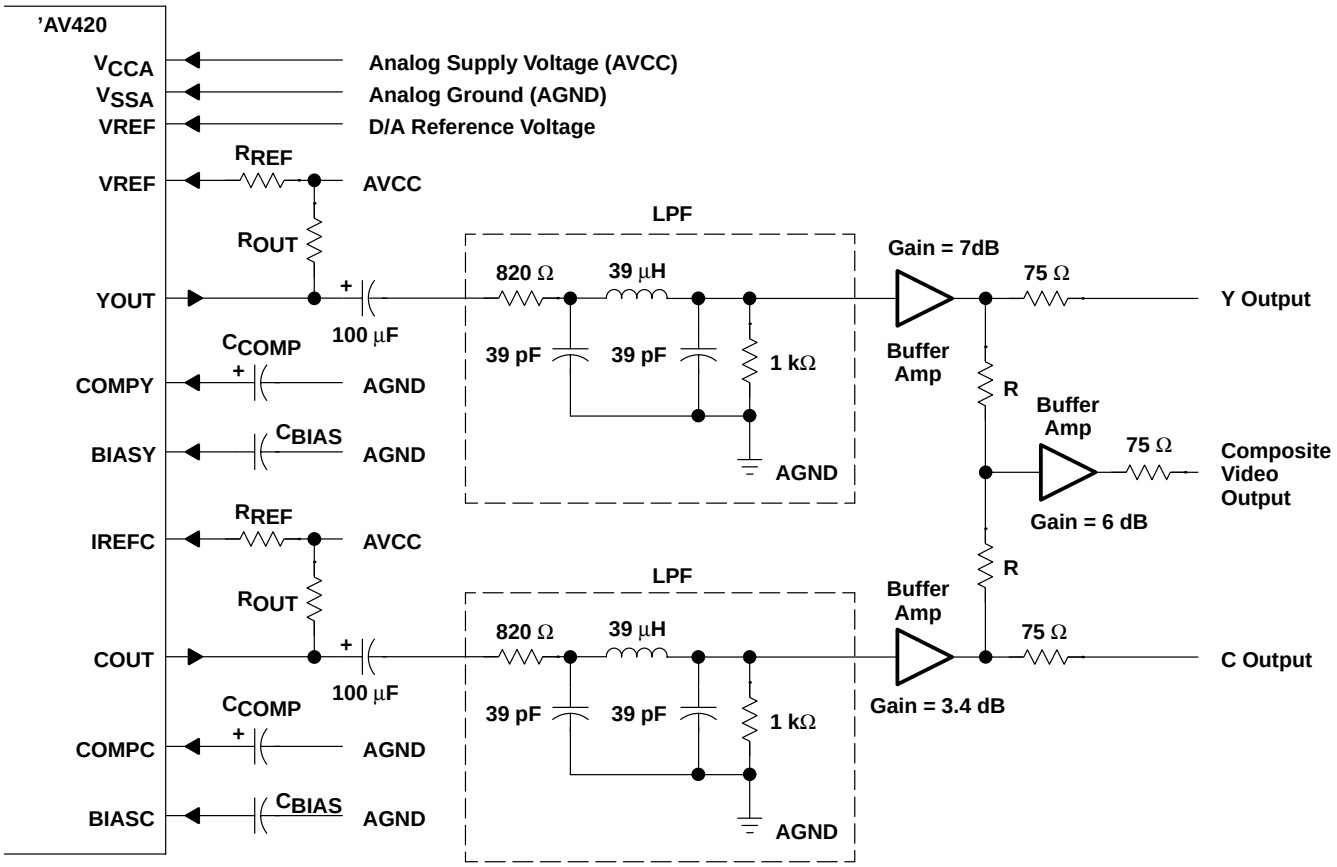


Figure 5. ’AV420 Analog Signals, Output Filters, and the Composite Video Generator

interlaced and noninterlaced operation

The ’AV420 generates interlaced or noninterlaced video signals. The $\overline{\text{INTER}}$ terminal controls the interlacing operation.

In the interlaced mode, the ’AV420 generates the 4-field, 262.5 lines/field, RS170A-compatible video signal at 59.94 fields/s. The Y and the C signals are output on two separate terminals: luminance and sync on the YOUT terminal and chrominance and subcarrier burst on the COUT terminal. The signal levels and the phase relationship (SCH) between the Y and the C signals conform to RS170A. Figure 6 shows the interlaced output.

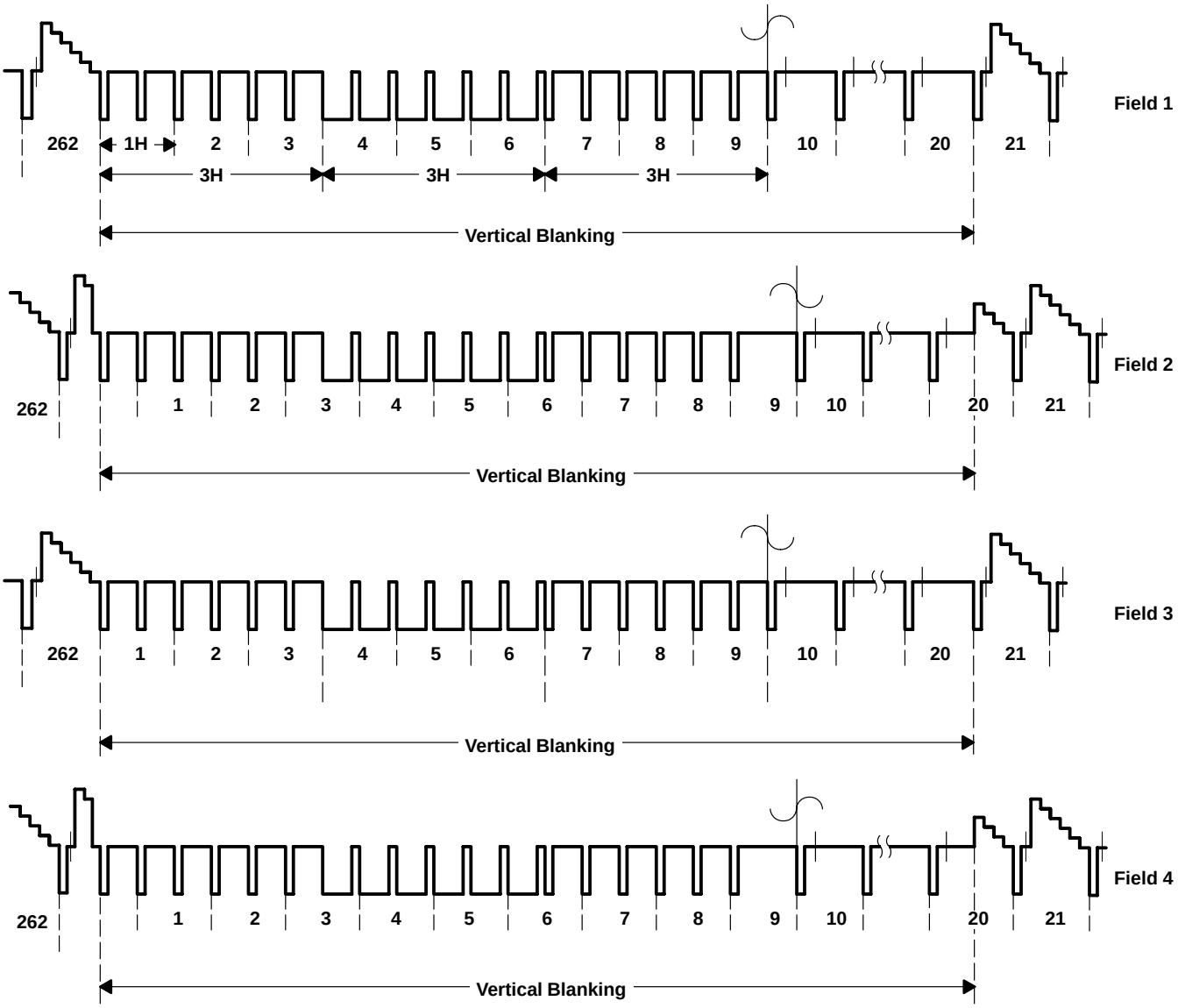


Figure 6. Interlaced Video Signal Output

In the noninterlaced mode, the ’AV420 generates the 1-frame, 262-lines/frame video signal. Since the subcarrier frequency and the line frequency are RS170A-compatible, the frame rate is 60.05 frames/s. The Y and the C signals are output on two seperate terminals, and their signal levels and the phase relationship (SCH) are RS170A-compatible. Figure 7 shows the noninterlaced output.

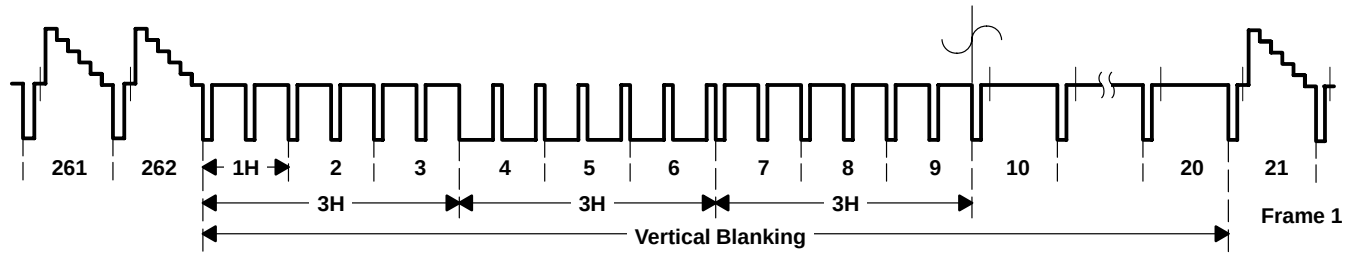


Figure 7. Noninterlaced Video Signal Output

internal and external synchronization

The ’AV420 is capable of generating internal and accepting external horizontal and vertical video-synchronization signals. These signals are connected to the ’AV420 $\overline{\text{HSYNC}}$ and VSYNC bidirectional terminals. The terminal EXTEN controls the synchronization operation.

In the internal synchronization mode, the $\overline{\text{HSYNC}}$ and the VSYNC are output terminals. The internal sync-signal generator (SSG) generates all the $\overline{\text{HSYNC}}$ and the VSYNC timing. Figure 8 through Figure 10 show different aspects of the ’AV420 internal synchronization timing.

timing requirements

		MIN	TYP	MAX	UNIT
t_{w1}	Pulse duration, $\overline{\text{RESET}}$ low	100			ns
t_{w2}	Pulse duration, internal $\overline{\text{HSYNC}}$ low		4.9		µs

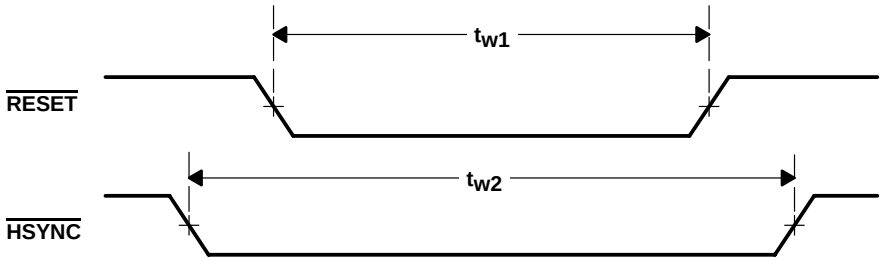


Figure 8. Internal Sync Pulse Width: $\overline{\text{HSYNC}}$ and $\overline{\text{RESET}}$

timing requirements

		MIN	TYP	MAX	UNIT
t_{d1}	Delay time, CLK135 to $\overline{\text{HSYNC}}$, VSYNC			15	ns

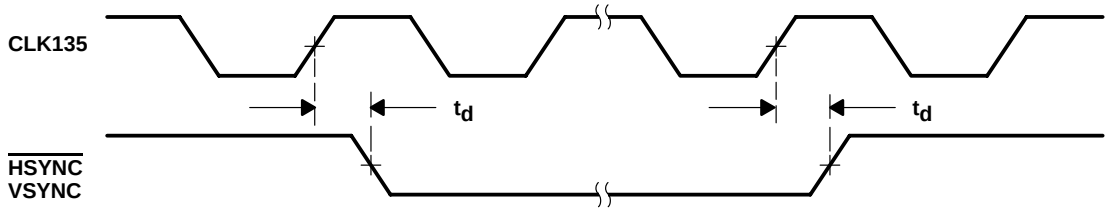


Figure 9. Internal Sync $\overline{\text{HSYNC}}$, VSYNC and CLK135 Timing

timing requirements

		MIN	TYP	MAX	UNIT
t_{w3}	Pulse duration, VSYNC		3		H

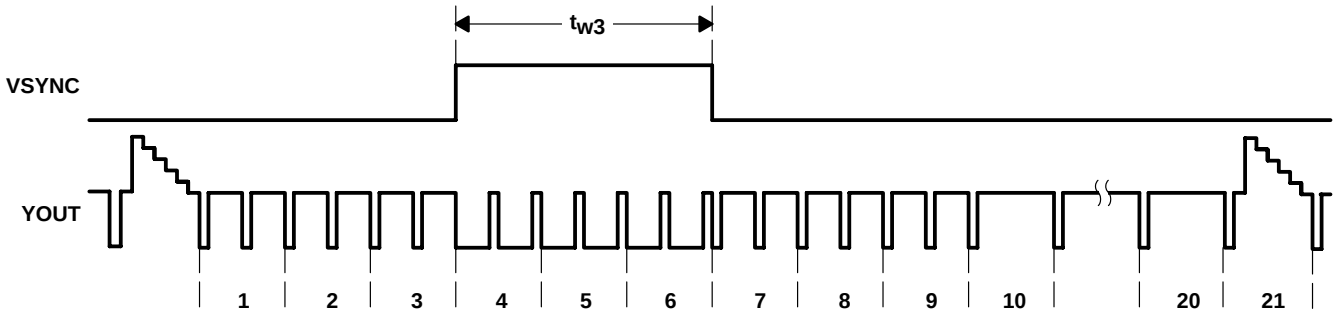


Figure 10. Internal Sync VSYNC Timing

In the external synchronization mode, the $\overline{\text{HSYNC}}$ and the VSYNC are input terminals. The $\overline{\text{HSYNC}}$ and the VSYNC signals are generated by an external device. In the ’AV420 interlaced mode, the timing of the $\overline{\text{HSYNC}}$ and the VSYNC signals must be RS170A-compatible. In the ’AV420 noninterlaced mode, the timing of the $\overline{\text{HSYNC}}$ signal is RS170A-compatible and the period of the VSYNC signal is 262H (H is the RS170A line period). Figure 11 and Figure 12 show the ’AV420 external synchronization timing.

timing requirements

		MIN	TYP	MAX	UNIT
t_{w4}	Pulse duration, external $\overline{\text{HSYNC}}$	300			ns
t_{su2}	Setup time, $\overline{\text{HSYNC}}$	10			ns
t_{d2}	Delay time, OSCIN to CLK135	30		45	ns

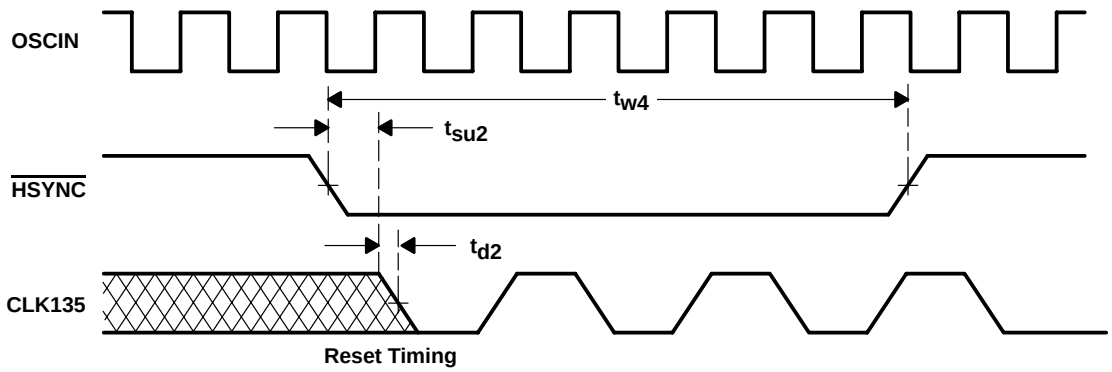


Figure 11. External Sync $\overline{\text{HSYNC}}$ and CLK135 Timing

timing requirements

		MIN	TYP	MAX	UNIT
t_{su3}	Setup time, VSYNC	–0.5		30	µs

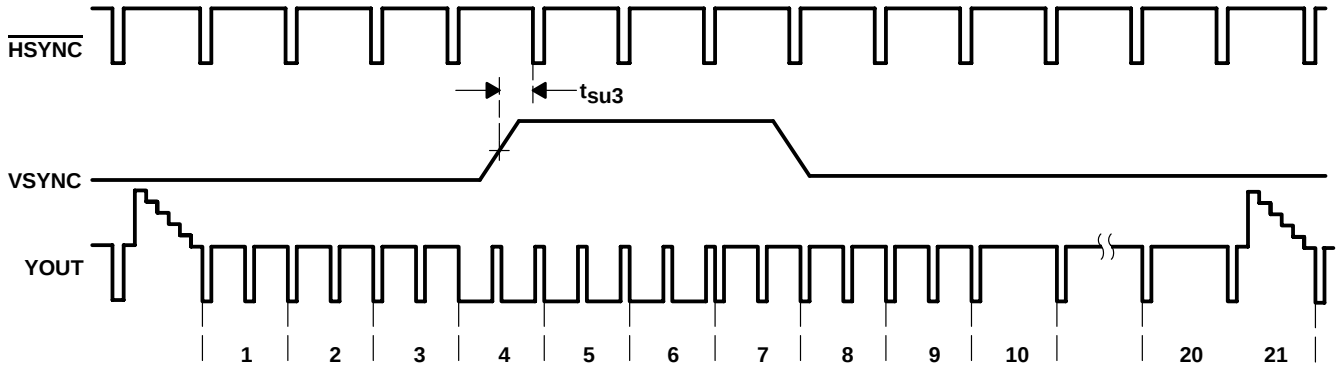


Figure 12. External Sync VSYNC Timing

vertical-line interpolation

The ’AV420 vertical-line interpolation (VLI) function optimizes the processing of MPEG-1 pictures. VLI is selectable by the user. When selected, VLI reduces the jaggedness of slanted straight lines and video flicker due to the low resolution and low decoding rate of MPEG-1 SIF pictures. VLI applies to the interlaced display mode only and can be selected when the same decoded MPEG-1 picture is displayed twice as two consecutive video fields. The IPEN and IPMOD terminals control the VLI operation.

The VLI is performed by vertical pixel averaging between two adjacent lines in either the odd or the even video fields. It is performed on the YIQ data, Y component only. The user can use VLI on the odd fields and then VLI on the even fields and select the one that yields the highest video quality. Figure 13 shows the results of VLI performed on odd and even video fields.

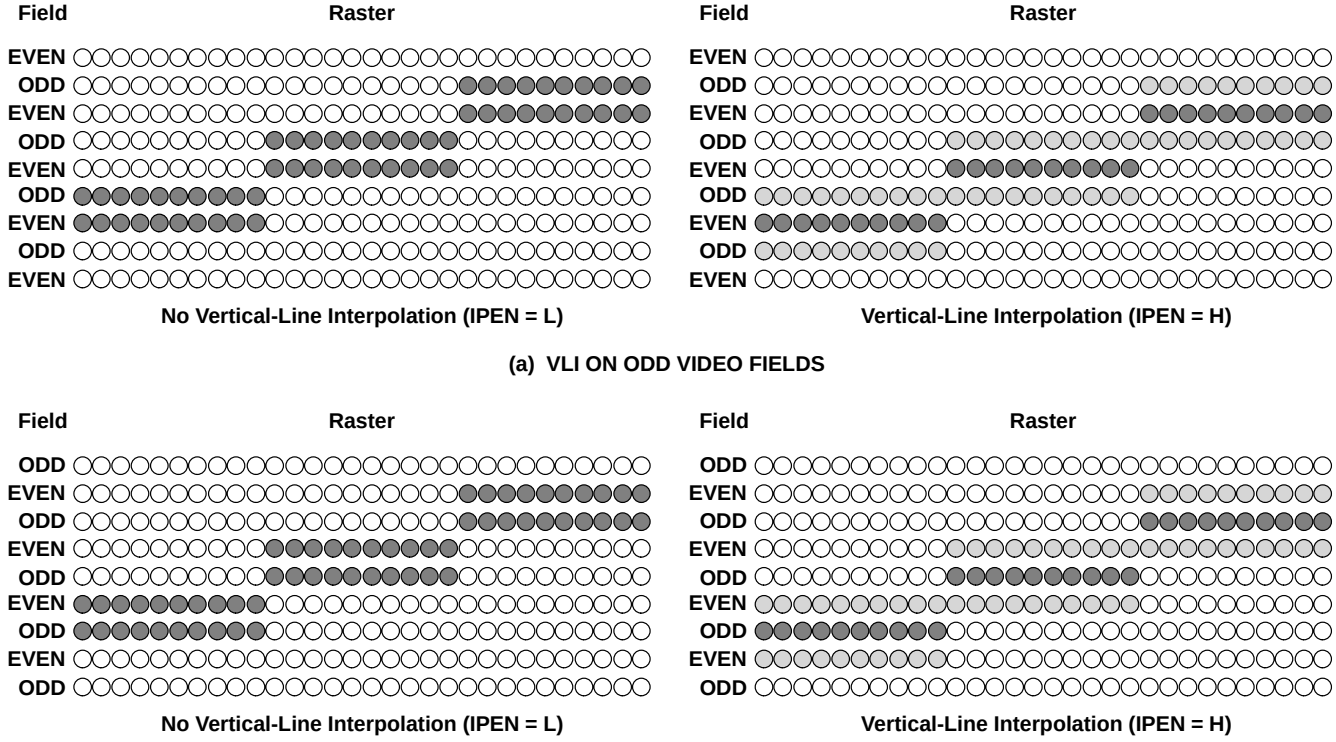


Figure 13. Vertical-Line Interpolation (VLI)

overlay function

The ’AV420 overlay function enables the superposition of text and graphics on the video. This function is also known as the on-screen display (OSD) and works by replacing the selected ’AV420 video-input pixels with the overlay-generated pixels. The signals at the ’AV420 overlay interface control the overlaying operation. After overlaying, the video-input pixels and the overlay-generated pixels are encoded together to form the analog waveforms.

The ’AV420 overlay interface is composed of the overlay/video-select signal (OLC), the overlay color-setting signals (OLR, OLG, and OLB) and the overlay luminance-setting signals (YADJ0 and YADJ1). All signals are inputs to the ’AV420, and their timing is the same as the pixel-input timing. Four overlay luminance levels and eight overlay colors are available. Table 1 and Table 2 show the overlay color and luminance settings, respectively.

overlay function (continued)

Table 1. Overlay Color Settings

OLR	OLG	OLB	OVERLAY COLOR
L	L	L	black
L	L	H	blue
L	H	L	green
L	H	H	cyan
H	L	L	red
H	L	H	magenta
H	H	L	yellow
H	H	H	white

Table 2. Overlay Luminance Settings

YADJ1	YADJ0	OVERLAY-LUMINANCE LEVEL
L	L	25%
L	H	50%
H	L	75%
H	H	100%

A possible design of a video-overlay system uses an overlay controller. This controller is not a part of the ’AV420. The overlay controller monitors the video-timing signals (VSYNC, $\overline{\text{HSYNC}}$, CLK135) between the ’AV420 and the pixel source. The controller causes the ’AV420 to replace the specified video input pixels with the overlay-generated pixels by appropriately asserting the signals at the ’AV420 overlay interface. A state-machine, a microcontroller, etc., can function as an overlay controller.

The following considerations apply for the ’AV420 overlay-system design:

- Since the ’AV420 overlay function works on a pixel-by-pixel basis, the controller must be fast enough to perform the overlaying operations in one period of the ’AV420 pixel clock (CLK135), about 74 ns. The operations include detection of the overlay-pixel positions and assertion of the ’AV420 overlay-interface signals subject to all required setup time conditions.
- If a fast controller is not possible or if lower overlay resolution is acceptable, a slower controller can be used. For example, a slower controller may be able to perform the overlaying operations in two periods of the ’AV420 pixel clock (about 148 ns) and replace every other ’AV420 video input pixel with the overlay-generated pixel.
- The programming and the effects of the overlay algorithms are affected by the ’AV420 interlaced/noninterlaced mode. For example, in the interlaced mode, the overlay pixels may need to be aligned in related odd and even fields, and in the noninterlaced mode, the overlay symbol size may need to be scaled appropriately.
- The ’AV420 overlay function is not affected by VLI in the ’AV420 because VLI takes place before the overlaying operation is performed.
- The ’AV420 overlay function can be used for video-test-pattern generation, without the external pixel source. For example, the ’AV420 can generate the video-timing signals, and the overlay controller can generate the ’AV420 overlay-interface commands required to produce the desired video test pattern.

oscillator circuit

The ’AV420 has an internal oscillator circuit used as the 27-MHz frequency reference. Figure 14 shows a recommended crystal circuit that needs to be connected between the ’AV420 OSCIN and OSCOUT terminals. The circuit includes a third-overtone 27 MHz crystal, with an equivalent series resistance under 40 Ω. Alternatively, a 27-MHz external clock with the minimum 60/40 duty cycle can be input on the OSCIN terminal. The accuracy and stability of the color subcarrier signal and other signals generated in the ’AV420 are directly dependent on the accuracy and stability of the crystal circuit or the external clock.

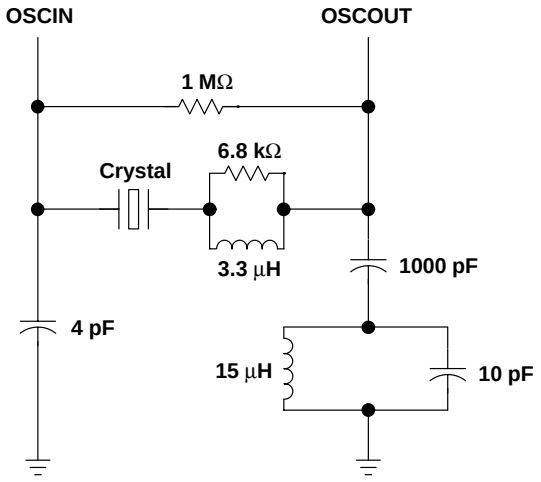


Figure 14. Recommended Crystal Circuit

test circuit

The ’AV420 has test terminals TEST0 through TEST4 and TOUT0 through TOUT7. These terminals are provided for future expansion and should be either grounded (TESTs) or left unconnected (TOUTs).

interface to the TMS320AV220

The ’AV420 interfaces directly to the TMS320AV220 video CD MPEG decoder. The ’AV220 is the pixel source for the ’AV420, and the ’AV420 can provide the video-synchronization timing to the ’AV220. The ’AV220 needs to be programmed appropriately to provide the required number of pixels per line and the required number of lines per field or frame to the ’AV420. Figure 15 shows an example of the 24-bit RGB interface between the ’AV420 and the ’AV220.

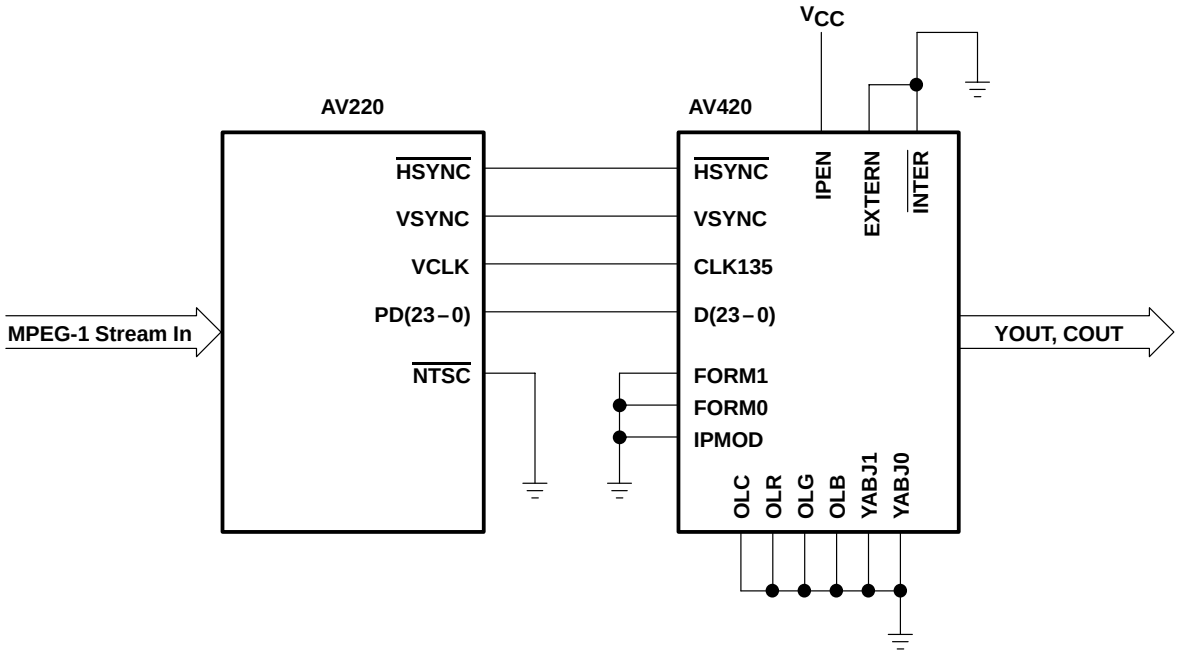


Figure 15. ’AV420 to ’AV220 Interface

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 6 V
Analog supply voltage range, V_{CCA} . . . . . –0.5 V to 6 V
Input voltage range . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range . . . . . –0.5 V to V_{CC} + 0.5 V
Output clamp current . . . . . ±20 mA
Operating free-air temperature range, T_A . . . . . –10°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

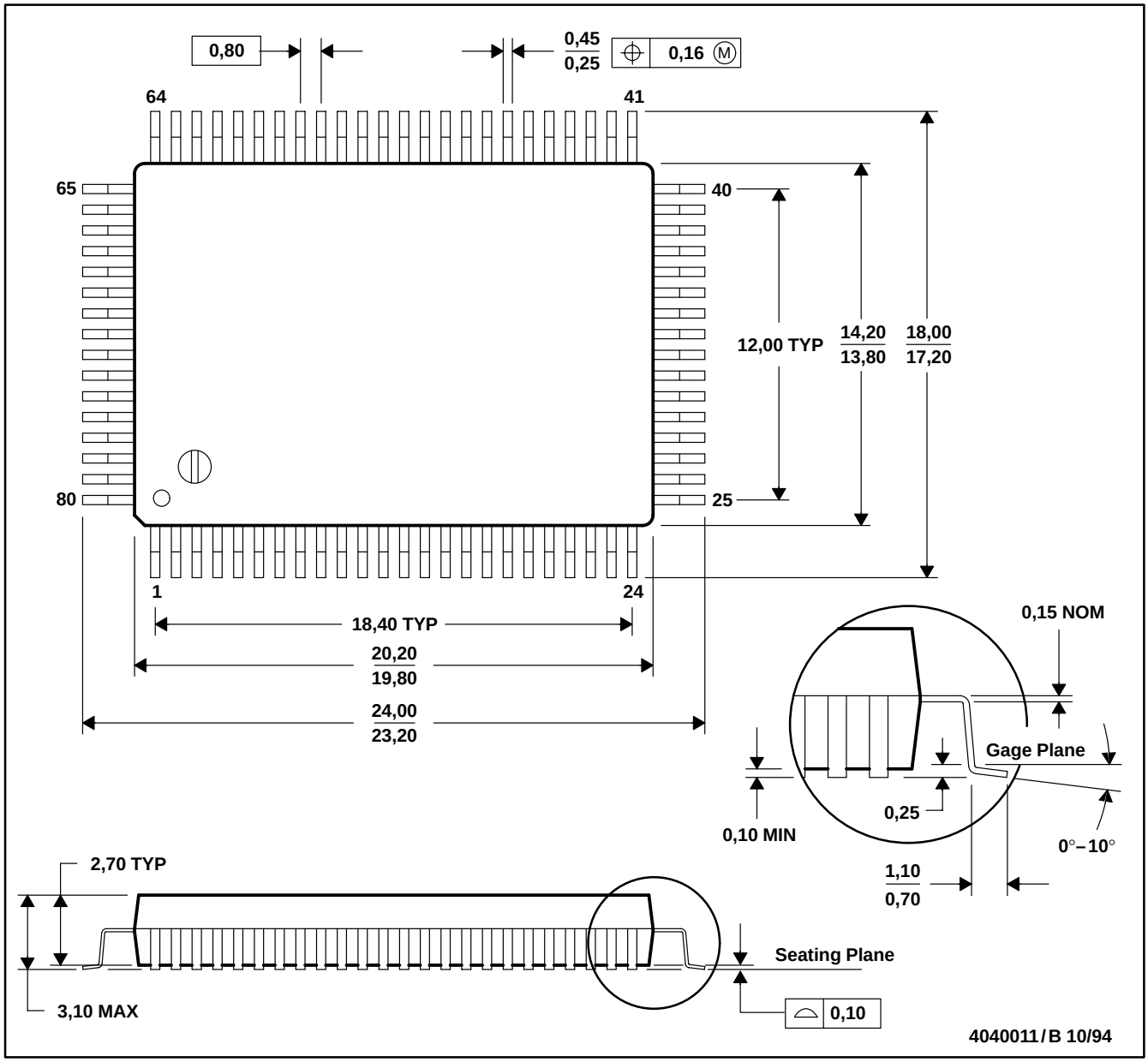
			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{CCA}	Analog supply voltage		4.75	5	5.25	V
VREF	D/A reference voltage			3		V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current		–1			mA
I_{OL}	Low-level output current				1	mA
f_{clock}	Clock frequency		–	27	–	MHz
R_{ext}	D/A output resistor	YOUT, COUT		200		Ω
	D/A reference resistor	IREF, IREFC		1600		
C_{ext}	D/A compensation capacitance	COMPY, COMPC		1		µF
	D/A bias capacitance	BIASY, BYASC		0.1		
T_A	Operating temperature range		–10	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = 1 mA	V_{CC}–0.8			V
V_{OL}	Low-level output voltage		I_{OL} = –1 mA			0.5	V
V_O	Output voltage	YOUT, COUT		VREF		V_{CC}	V
I_I	Input current		V_{CC} = 5.25 V, V_I = 0 to V_{CC}			1	µA
I_{CC}	Supply current		V_{CC} = 5.25 V		30		mA
I_{CCA}	Analog supply current	With ROUT	V_{CC} = 5.25 V		30		mA
C_i	Input capacitance		f = 1 MHz		8		pF

MECHANICAL DATA

PH (R-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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