SCSS013C – MAY 1993 – REVISED AUGUST 1995

- **Single-Chip ISO-MPEG (Layers 1 and 2) Audio Decoder**
- **Decodes Mono, Dual, Stereo, and Joint Stereo Modes**
- **Supports All MPEG Sampling and Data Rates, Including Free Format**
- **Complete With Stereo Level Control**
- **Input May Be MPEG Audio Frames or the Full-Multiplexed MPEG System Stream**
- **Accepts Compressed Audio at up to 15-Mbits/Second Burst Rate**
- **Bit-Serial or Byte-Parallel Compressed Data Input**
- **16- or 18-Bit Serial PCM Output Directly Interfaces to Most Serial D/A Converters**
- **8-Bit Microprocessor Control Interface**
- **Optional DRAM Interface for Audio Delay and More Robust Error Concealment**
- **Low-Power Submicron CMOS Technology, Fully TTL Compatible**
- **Small Footprint 120-Pin Plastic Quad Flat Package**
- **IEEE Standard 1149.1 (JTAG) Compatible**

description

The Texas Instruments TMS320AV110 MPEG audio decoder implements in a single chip, the International Standards Organization — Moving Picture Expert Group (ISO-MPEG) audio decompression algorithm. The ’AV110 accepts an MPEG-compliant compressed audio stream at any of the valid MPEG data and sampling rates and produces decompressed 2s complement audio output in either 16- or 18-bit serial pulse-code modulation (PCM) format. The PCM data stream is suitable for direct input to most commercially available digital-to-analog (D/A) converters.

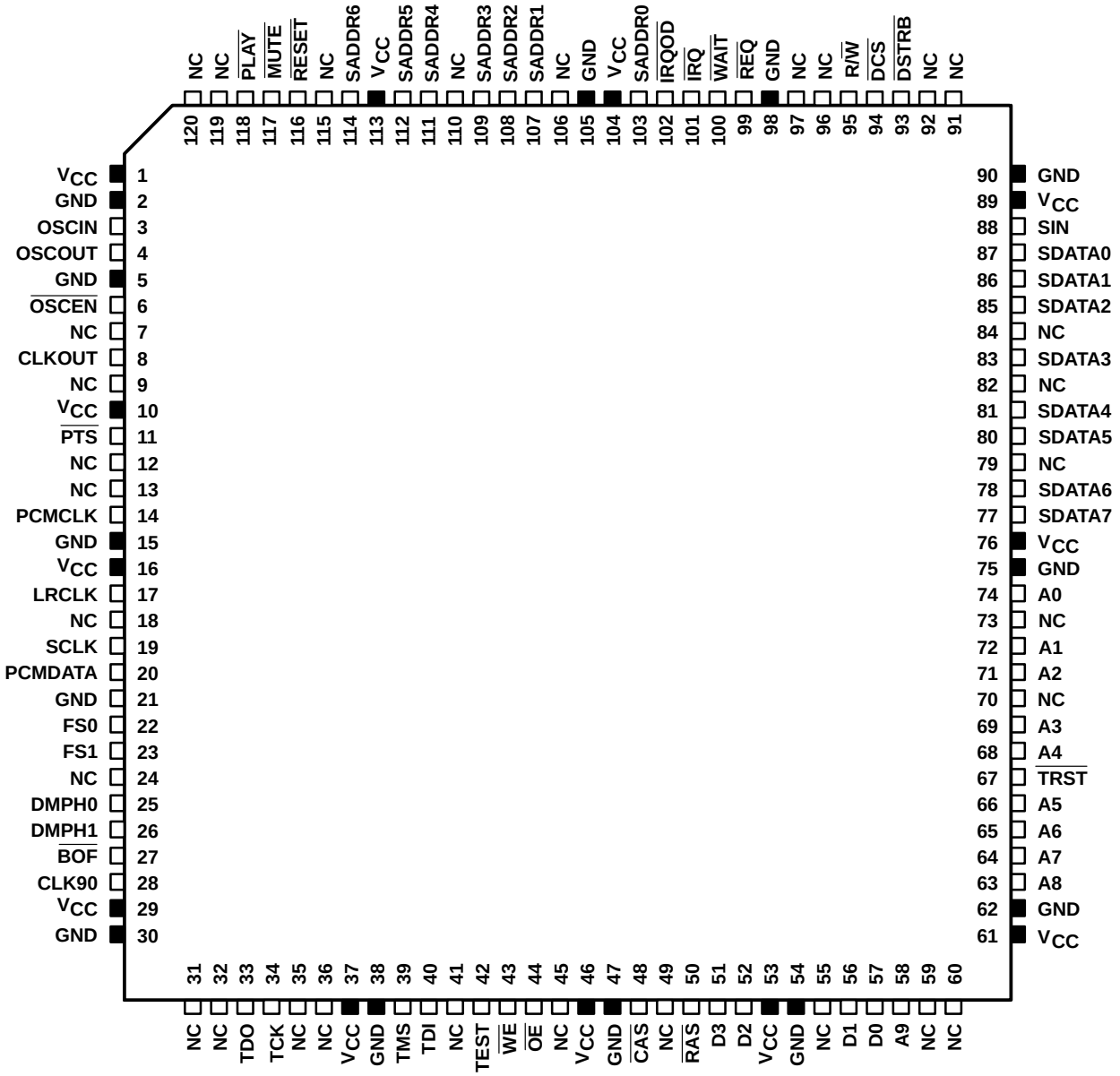
Both MPEG layers one and two are implemented. The ’AV110 decodes a single monaural channel, two independent mono channels, stereo channels, and joint stereo channels. The compressed audio may be input either as MPEG audio frames or as the full-multiplexed system stream containing multiple audio and/or video packets. The input may be at the actual bit rate or it may be in bursts at up to 15 Mbits/s.

Compressed audio may be input in either bit-serial or byte-parallel formats. An eight-bit microprocessor interface is provided for control and status register access with maskable interrupts for the critical status and error flag registers.

While the ’AV110 can operate as a single, stand-alone decoder, provision is also made for using a 256K×4 DRAM device if buffering of the audio stream is required. With the external memory in place, audio may be buffered for synchronization purposes. The external memory also allows the employment of more robust error-concealment techniques if cyclic redundancy check (CRC) or synchronization errors are detected by the decoder.

The TMS320AV110 is implemented in the Texas Instruments EPIC™ CMOS submicron, triple-level-metal technology.

PBM PACKAGE
(TOP VIEW)



NOTE: Pins labeled NC are used for factory test purposes and should be tied to GND.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	58 63 64 65 66 68 69 71 72 74	O	DRAM address bus output
$\overline{\text{BOF}}$	27	O	Beginning of frame signal. The falling edge of $\overline{\text{BOF}}$ signals the beginning of a new audio frame. The first bit of the new frame is on the PCMDATA output at the falling edge of $\overline{\text{BOF}}$. The falling edge of $\overline{\text{BOF}}$ will occur synchronous to the OSCIN clock and will occur from one to two OSCIN clocks prior to the first rising edge of SCLK after a rising LRCLK edge. It varies from one to two clocks because OSCIN may be asynchronous to SCLK. The low pulse width is four periods of the OSCIN clock, and the rising edge of $\overline{\text{BOF}}$ is also synchronous to OSCIN.
$\overline{\text{CAS}}$	48	O	DRAM column address strobe
CLK90	28	I	90-kHz reference clock input. Optionally used for audio/video synchronization. Provides the clock for the internal reference counter. CLK90 should be tied to GND if the ’AV110 is not used for synchronization.
CLKOUT	8	O	Buffered system clock (OSCIN) output
D3 D2 D1 D0	51 52 56 57	I/O	DRAM data bus
$\overline{\text{DCS}}$	94	I	Register access chip select
DMPH1 DMPH0	26 25	O	Decoded deemphasis select output. The audio deemphasis information is decoded from the header and is output on DMPH0 and DMPH1. The information is also available in the DMPH register, and an interrupt is generated on a change in the DMPH value. The interrupt and DMPH0 and DMPH1 change state when the corresponding frame is at the PCM output stage. (DMPH1, DMPH0) 00 = none, 01 = 50/15 microseconds, 10 = reserved, 11 = CCITT J.17.
$\overline{\text{DSTRB}}$	93	I	Data strobe. DSTRB is used to load compressed audio data into the ’AV110 in both bit-serial and byte-parallel modes.
FS1 FS0	23 22	O	Decoded sampling frequency output. The ’AV110 decodes the sampling frequency from the MPEG header. This data is also available in the PCM_FS register. The FS0 and FS1 terminals reflect the current sampling frequency when the first data point of the frame is at the PCM output stage. If enabled and the FS value has changed, an interrupt is generated. (FS1, FS0): 00 = 44.1 kHz, 01 = 48 kHz, 10 = 32 kHz, 11 = reserved.
GND	2, 5, 15, 21, 30, 38, 47, 54, 62, 75, 90, 98, 105		Ground
$\overline{\text{IRQ}}$	101	O	Interrupt request output. This is an active-low pulse that is triggered by one of the bits being set in the INTR register, unless the corresponding bit is masked in the INTR_EN register.
$\overline{\text{IRQOD}}$	102	O	Interrupt request, open-drain output
LRCLK	17	O	Left/right channel PCM-data-sampling clock. A high logic level selects left PCM data, and a low logic level selects right PCM data.
$\overline{\text{MUTE}}$	117	I	Forces the output of muted PCM data when $\overline{\text{MUTE}}$ is low. PCM muting is in effect if either this line or the MUTE register is asserted. Muting does not affect the actual audio decoding process (see Table 1).

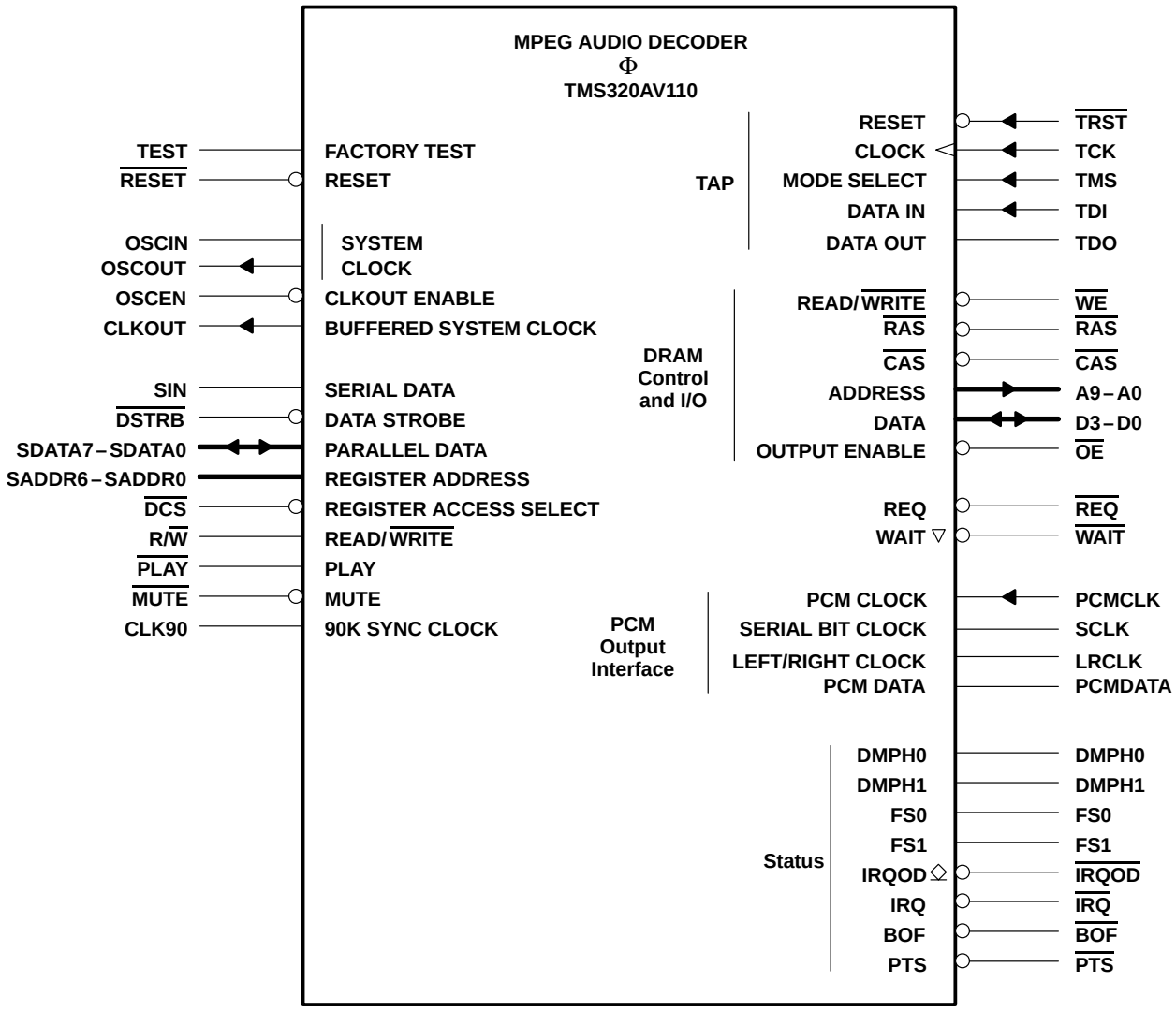
Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
NC	7, 9, 12, 13, 18, 24, 31, 32, 35, 36, 41, 45, 49, 55, 59, 60, 70, 73, 79, 82, 84, 91, 92, 96, 97, 106, 110, 115, 119, 120		No Connect. These terminals are used for factory testing and should be tied to GND.
$\overline{OE}$	44	O	DRAM output enable
$\overline{OSCEN}$	6	I	Buffered oscillator (CLKOUT) output enable
OSCIN	3	I	Oscillator input or crystal connection. Asynchronous system clock.
OSCOUT	4	O	Crystal connection (crystal low side)
PCMCLK	14	I	PCM clock input. Used with PCM_DIV register value to generate SCLK and LRCLK.
PCMDATA	20	O	PCM serial data output
$\overline{PLAY}$	118	I	Enables the output of decoded audio data. Output of decoded audio data is enabled only if both this line and the PLAY register are asserted. Does not affect the output of muted audio (see Table 1).
$\overline{PTS}$	11	O	Presentation time stamp output. $\overline{PTS}$ goes low when the first data word associated with a frame that contains a PTS is at the PCM output stage. $\overline{PTS}$ pulses low for every PTS if the PTS interrupt is not enabled. When the PTS interrupt is enabled, $\overline{PTS}$ will continue to pulse low if the PTS register is read after each PTS pulse.
$\overline{RAS}$	50	O	DRAM row address strobe
$\overline{REQ}$	99	O	Data request
$\overline{RESET}$	116	I	Resets the audio decoder. Functionally equivalent to asserting the RESET register except that the MUTE and PLAY registers are deasserted and the PCM_DIV register is affected. $\overline{RESET}$ must be asserted after power up. $\overline{RESET}$ low disables register accesses.
R/$\overline{W}$	95	I	Register read/write select
SADDR6 SADDR5 SADDR4 SADDR3 SADDR2 SADDR1 SADDR0	114 112 111 109 108 107 103	I	Register address bus
SCLK	19	O	Serial PCM output bit clock
SDATA7 SDATA6 SDATA5 SDATA4 SDATA3 SDATA2 SDATA1 SDATA0	77 78 80 81 83 85 86 87	I/O	8-bit parallel data bus for register input/output and audio data input
SIN	88	I	Serial compressed audio data input
TCK	34	I	Test Access Port (TAP) test clock input. Should be tied low for normal operation.
TDI	40	I	TAP test data input
TDO	33	O	TAP test data output
TEST	42	I	Test enable. TEST must be tied low.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TMS	39	I	TAP test mode select
$\overline{\text{TRST}}$	67	I	TAP test reset input, active low. $\overline{\text{TRST}}$ should be tied low for normal operation or connected to the $\overline{\text{RESET}}$ input.
V_{CC}	1, 10, 16, 29, 37, 46, 53, 61, 76, 89, 104, 113	I	5-V supply voltage
$\overline{\text{WAIT}}$	100	O	Wait request — 3-state output. Used during register read and write operations.
$\overline{\text{WE}}$	43	O	DRAM read/write control

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

architecture

The TMS320AV110 architecture is shown in Figure 1. The ’AV110 is a combination of a hardwired, dedicated high-speed arithmetic unit and a microcoded input processor. Functionally, it may be divided into the following major blocks:

- Host bus interface
- Input processor
- DRAM buffer interface
- Arithmetic unit
- PCM output interface

This document covers only the host bus interface and the PCM output interface because they are the only blocks the user will interface to. The input processor, DRAM interface, and the arithmetic unit may be considered a black box that is preconfigured to implement the MPEG audio algorithm.

The primary architectural consideration is application flexibility. Although the MPEG audio standard was developed in conjunction with the video compression standard, it is also suited for many nonvideo applications.

The TMS320AV110 can be used in two primary modes. In audio-only systems, the ’AV110 functions as a single-chip decoder with no support circuitry except a 24-MHz crystal or an external clock input. If the application also includes video decoding, an external 256K $\times$ 4 DRAM may be used to delay the audio stream for synchronization purposes. The ’AV110 accepts the full MPEG system data stream and decodes the presentation time stamp (PTS) and the system reference clock (SRC) to aid in system synchronization.

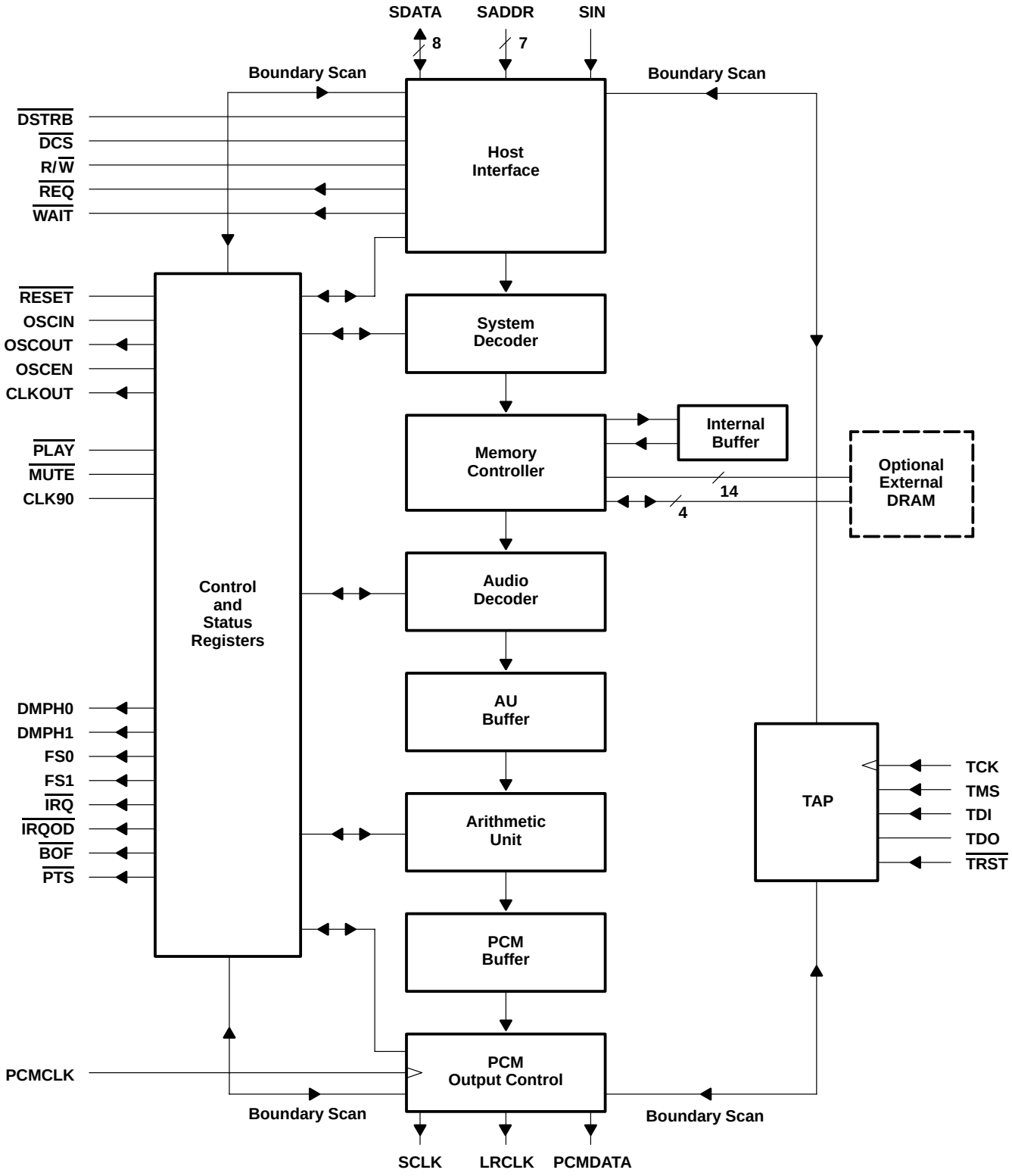


Figure 1. Functional Block Diagram

host bus interface

The host bus interface handles all communication with the user, both for compressed audio data input and for control information. It consists of an 8-bit generic microprocessor interface, a DMA interface, a serial data input interface, and a number of individual control lines and internal registers. Interrupt capability to the host processor is also provided with a single interrupt line ($\overline{IRQ}$) driven by the interrupt register and the interrupt mask register (INTR_EN).

input format

The compressed audio stream can be input using one of three modes. The content of the SIN_EN control register selects serial or parallel data formats. If set to a 1, input is a serial bit stream using the SIN input for data and $\overline{DSTRB}$ as the input clock.

If the control register is set to a 0, parallel data format is selected and data may be input in the byte-parallel format on the SDATA (7:0) inputs. Clocking can be initiated either by using the $\overline{DSTRB}$ or $\overline{DCS}$ lines. If $\overline{DSTRB}$ is used, the operation resembles a DMA access with no register addressing involved. If the DATAIN register is being written to using the $\overline{DCS}$ line, it must be addressed before each byte like any other register access.

compressed data format

The format of the compressed data stream is selected by the STR_SEL register. This is a two-bit register, with the following selections:

00 = MPEG audio stream
01 = MPEG audio packets
10 = Input is a multiplexed MPEG system stream. It may contain one or more audio and/or video streams.
11 = Audio bypass

If an MPEG packet or system stream is selected, two additional registers can be used. AUD_ID_EN enables or disables the audio ID field decoding. If this AUD_ID_EN register is set to 1, the ID field is compared with the contents of the AUD_ID register and the audio is decoded if the ID fields match. If AUD_ID_EN is cleared to 0, the ID field is ignored.

MPEG audio data input

bit-serial data input

Bit-serial data input is performed using the serial data input (SIN) and the data strobe input ($\overline{\text{DSTRB}}$) (see Figure 2). Data is set up on SIN and strobed into the chip on the rising edge of $\overline{\text{DSTRB}}$. Audio data transfer to the ’AV110 is requested by assertion of the request line ($\overline{\text{REQ}}$) signaling that the ’AV110 is ready to accept data and is awaiting service.

’AV110 CONTROL REGISTER

SIN_EN	Serial input enable	0 = Parallel (byte) data input (see Figure 3)
		1 = Serial (bit) data input (see Figure 2)

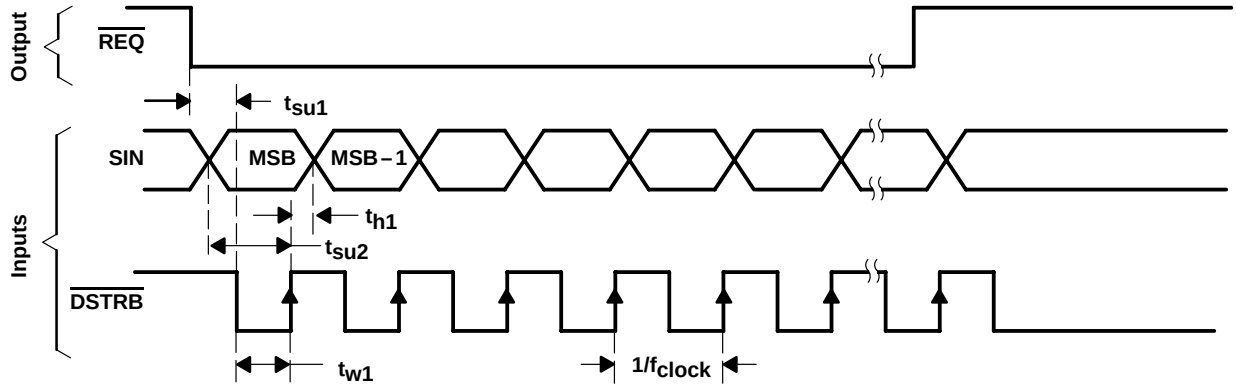


Figure 2. Bit-Serial Data-Input Timing

In bit-serial data-input mode, any of the following conditions will cause $\overline{\text{REQ}}$ to go high:

- $\overline{\text{RESET}}$ goes active.
- Restart is initiated.
- The input buffer is full.

If the input buffer becomes full, the $\overline{\text{REQ}}$ output goes high asynchronous to $\overline{\text{DSTRB}}$. After $\overline{\text{REQ}}$ goes high, two additional data bits can be strobed into the ’AV110 on the rising edge of $\overline{\text{DSTRB}}$.

byte-parallel data input

Byte-parallel data input is performed using the data I/Os (SDATA[7:0]) and the data strobe ($\overline{\text{DSTRB}}$) input. Data is strobed into the chip on the rising edge of $\overline{\text{DSTRB}}$. $\overline{\text{REQ}}$ goes high after every rising edge of $\overline{\text{DSTRB}}$. $\overline{\text{REQ}}$ remains high only when the input buffer is full (see Figure 3). One additional byte of data can be input after $\overline{\text{REQ}}$ signals that the input buffer is full. $\overline{\text{REQ}}$ returns low synchronous to the system clock (OSCIN) when the ’AV110 is ready for more data.

’AV110 CONTROL REGISTER

SIN_EN	Serial input enable	0 = Parallel (byte) data input (see Figure 3)
		1 = Serial (bit) data input (see Figure 2)

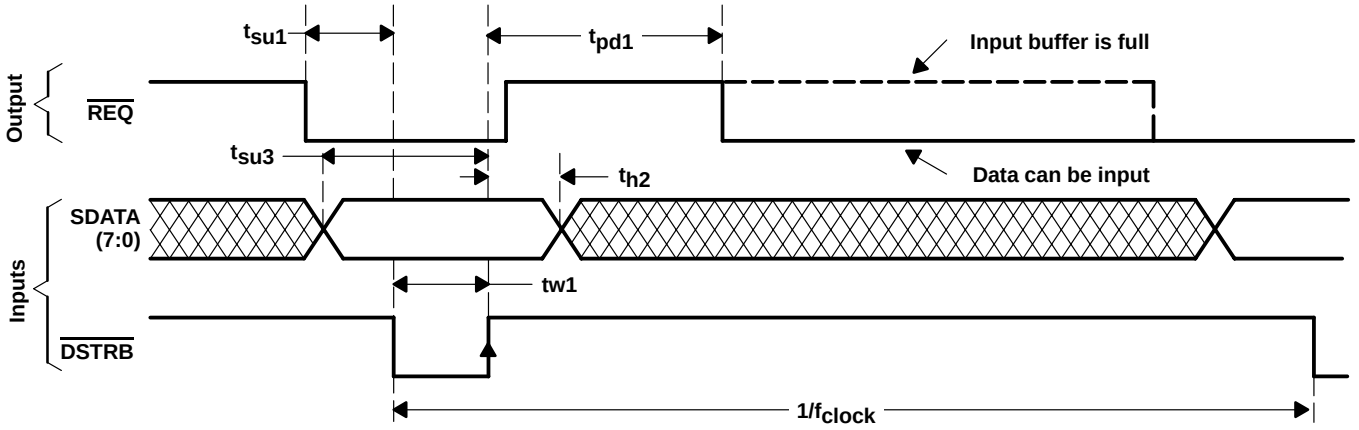


Figure 3. Byte-Parallel Data-Input Timing

memory mapped byte-parallel data input

Memory mapped byte-parallel data input is performed as a register access to the primary data-input register (DATAIN[7:0]). This procedure is described in the following section. $\overline{\text{REQ}}$ goes high on the falling edge of DCS whenever the DATAIN register is addressed. $\overline{\text{REQ}}$ remains high when the input buffer is full (see Figure 4). One additional byte of data can be input after $\overline{\text{REQ}}$ signals that the input buffer is full. $\overline{\text{REQ}}$ returns low synchronous to the system clock (OSCIN) when the device is ready for more data.

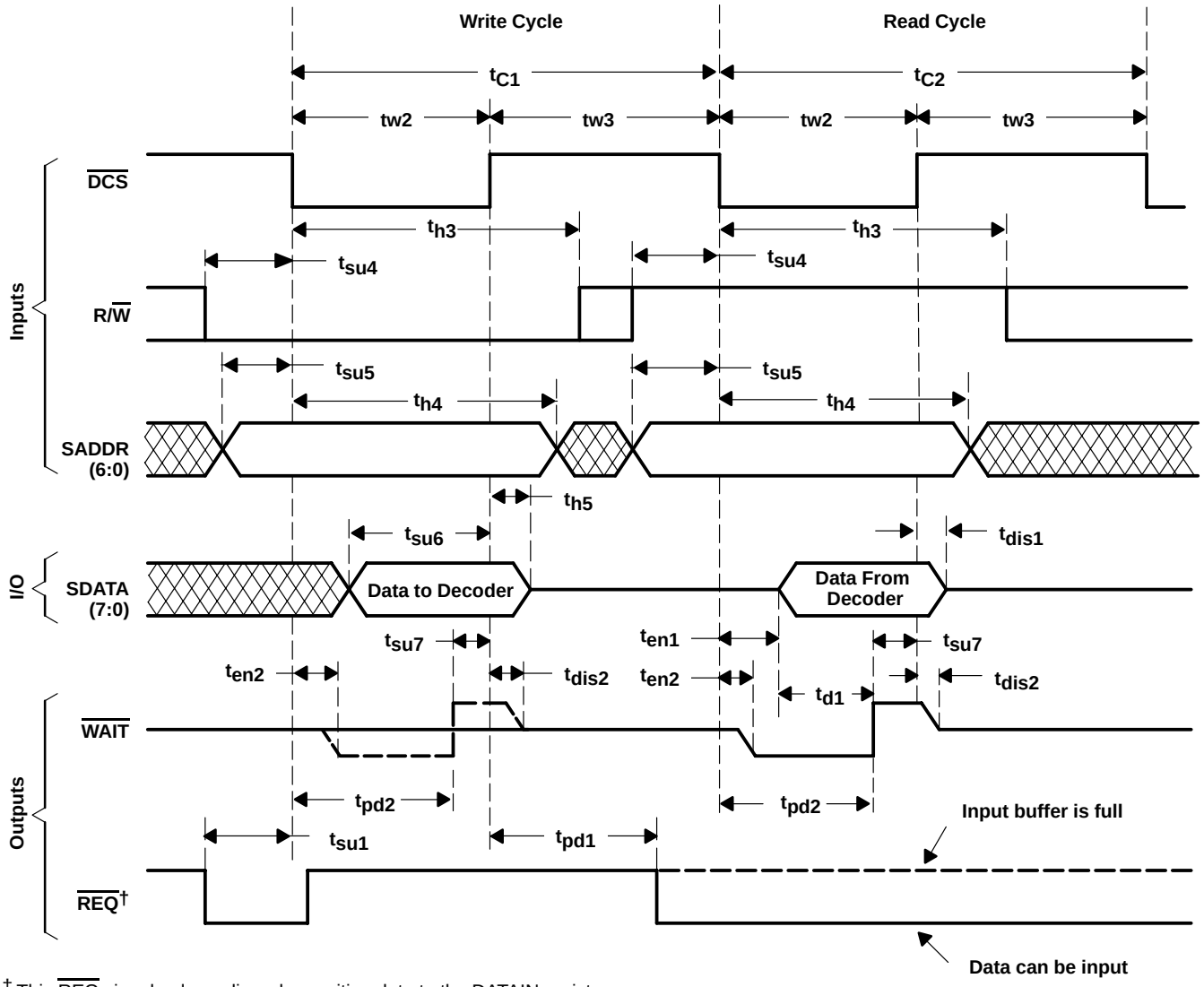
access to control and status registers

A register access chip select ($\overline{\text{DCS}}$) and a seven-bit address (SADDR[6:0]) are used to address the ’AV110 control and status registers including the data-input register. Read/write operations are designated with R/$\overline{\text{W}}$.

Register access is performed utilizing the chip select, read/write, data, and address lines. The host first sets up the address, read/write, and data inputs. The $\overline{\text{DCS}}$ line is then asserted by the host. When R/$\overline{\text{W}}$ is high (read), assertion of the $\overline{\text{DCS}}$ line drives the SDATA lines. For R/$\overline{\text{W}}$ low (write), the ’AV110 latches the data on the SDATA I/O lines when $\overline{\text{DCS}}$ is deasserted.

register-access read cycle timing

Register-access read is initiated when the host sets R/$\overline{W}$ high and sets up the address of the register that is to be read (see Figure 4). A setup time (t_{su4}) later, the host asserts $\overline{DCS}$. The 'AV110 uses the falling edge of $\overline{DCS}$ to store the state of R/$\overline{W}$ and SADDR. The 'AV110 register-access controller drives $\overline{WAIT}$ low. The $\overline{WAIT}$ line being low prevents the host from deasserting $\overline{DCS}$. The 'AV110 completes the read cycle by taking $\overline{WAIT}$ high and driving SDATA[7:0] with valid data. The host detects $\overline{WAIT}$ high and takes $\overline{DCS}$ high to latch the valid data on SDATA[7:0]. When the 'AV110 releases $\overline{WAIT}$, another read or write cycle can occur.



† This $\overline{REQ}$ signal only applies when writing data to the DATAIN register.

Figure 4. Register-Access Read and Write Cycle Timing

register-access write cycle timing

The host can initiate a register access request while the 'AV110 is still busy with the prior request because an access cycle requires from 166 ns to 250 ns w; the minimum $\overline{DCS}$ period is only 100 ns. The 'AV110 stores the state of R/$\overline{W}$ and SADDR on the falling edge of $\overline{DCS}$ and drives $\overline{WAIT}$ low if it has not completed the prior request. The $\overline{WAIT}$ output is used to prevent the host from deasserting $\overline{DCS}$ (see Figure 4). When the prior write request is completed, the 'AV110 drives $\overline{WAIT}$ high. The host detects the $\overline{WAIT}$ high output and takes $\overline{DCS}$ high. The 'AV110 then releases $\overline{WAIT}$ and stores the data on the SDATA lines.

wait timing

The $\overline{\text{WAIT}}$ output is used by the ’AV110 to control memory-mapped communications between the host and the ’AV110. The $\overline{\text{WAIT}}$ line can be shared among devices and therefore it is in the high-impedance state when not in use. The $\overline{\text{WAIT}}$ line is driven within 20 ns of the $\overline{\text{DCS}}$ assertion (falling edge) and is in the high-impedance state within 20 ns of the release of the $\overline{\text{DCS}}$ line.

register accesses and data inputs

If register accesses and data inputs (serial or parallel) are performed back-to-back, the timing relationships shown in Figure 5 must be met. These setup times provide sufficient time to assure that these operations do not interfere with each other.

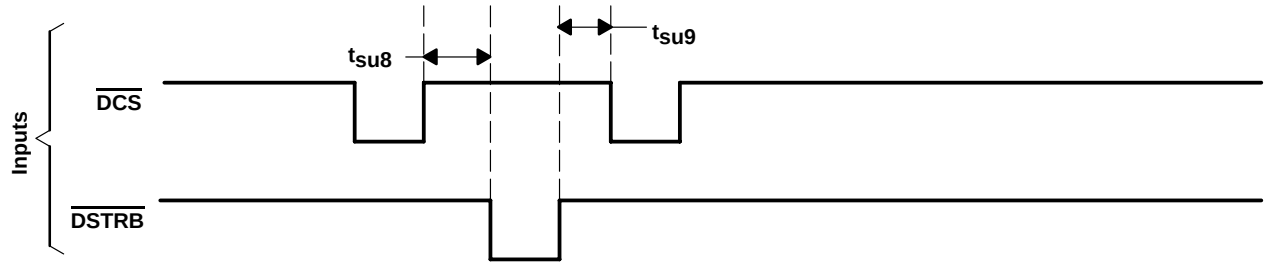
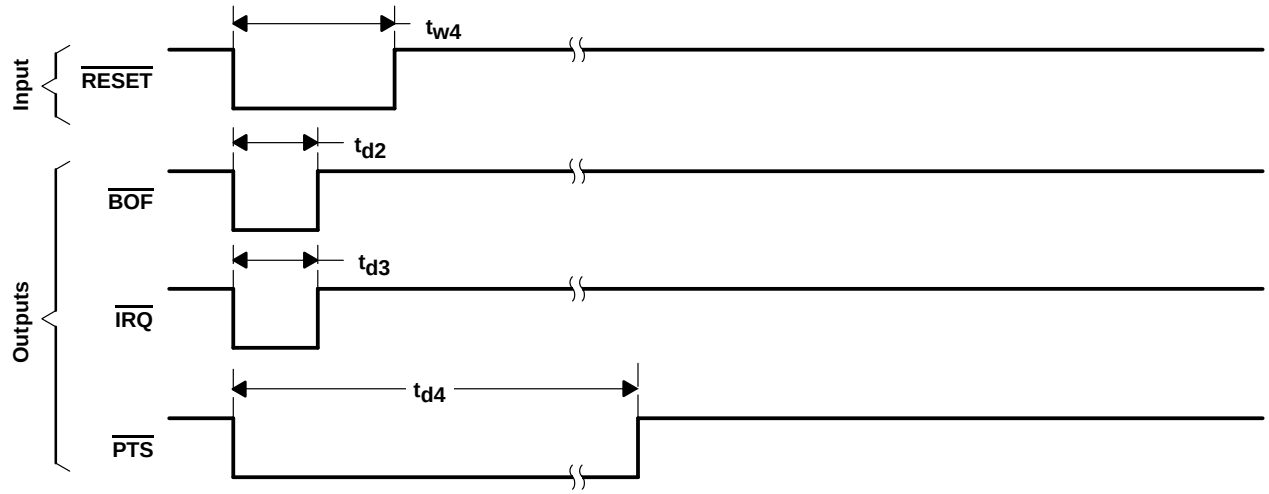


Figure 5. Data-Strobe Timing

reset operations

There are no default settings of the control and status registers; the audio decoder requires that the host set all control register settings using register-access mode. Reset can be initiated by the $\overline{\text{RESET}}$ input or by the host writing to the RESET register via register access. (Upon power up, the $\overline{\text{RESET}}$ input must be used.) Figure 6 shows $\overline{\text{RESET}}$, $\overline{\text{BOF}}$, $\overline{\text{IRQ}}$, and $\overline{\text{PTS}}$ timing.



NOTE: This diagram shows individual signal timing only. The signals are shown together for convenience and do not show their relationship.

Figure 6. $\overline{\text{RESET}}$, $\overline{\text{BOF}}$, $\overline{\text{IRQ}}$, and $\overline{\text{PTS}}$ Signal Timing

reset and restart actions

Reset, initiated either by the $\overline{\text{RESET}}$ input or a register-access write initiates the following actions:

- The reset (RESET) register is set.
- The $\overline{\text{REQ}}$ output goes high.
- The interrupt request (INTR) and interrupt enable (INTR_EN) registers are cleared.
- The buffer (BUFF) register is cleared.
- The DRAM goes through power-up refresh cycling (pin reset only).
- All data buffers are cleared. This takes multiple clock cycles.
- The ’AV110 checks for the presence of external DRAM and the size of the external DRAM.
- The MUTE and PLAY registers are deasserted (pin reset only). This inhibits the output clocks, LRCLK and SCLK, and zeros the data out.
- The PCM_DIV register is affected by pin reset; otherwise all other control registers remain in their existing states.
- Register accesses by the host interface are disabled only when $\overline{\text{RESET}}$ is low. Audio data can be input only after $\overline{\text{REQ}}$ has gone low.
- The ’AV110 terminates the reset cycle. It clears the reset register and $\overline{\text{REQ}}$ goes low. Reset cycles last approximately 700 μs without DRAM and 3.7 ms with DRAM (OSCIN 24 MHz).

Restart can be initiated by the host writing to the RESTART register (flush data buffers), which starts the following actions:

- The RESTART register is set.
- The $\overline{\text{REQ}}$ output goes high.
- The interrupt registers (INTR and INTR_EN) are cleared.
- The BUFF register is cleared.
- The DRAM does not go through power-up refresh cycling.
- All data buffers are cleared.
- MUTE, PLAY, and all other control and status registers remain at their existing state.
- Register accesses by the host interface are not disabled. However, when $\overline{\text{REQ}}$ is high, the host cannot register-access the primary data input.
- The ’AV110 terminates the restart cycle and clears the RESTART register. $\overline{\text{REQ}}$ goes low.

resetting/initializing upon power up

Upon powering up the system, the host takes the following actions:

Resets the ’AV110 by using the $\overline{\text{RESET}}$ input. A few of the important actions that affect the user are:

- $\overline{\text{REQ}}$ is high for the duration of the reset cycle.
- The PCM output clocks are turned off and the PCMDATA out is zero.
- Upon conclusion of the reset cycle, $\overline{\text{REQ}}$ goes low. The PCM output clocks and data remain zero.

The host must configure all ’AV110 control registers. The host can begin configuring the ’AV110 when $\overline{\text{RESET}}$ is returned high. The host should set the PCM_DIV register before changing $\overline{\text{MUTE}}$ and $\overline{\text{PLAY}}$. The host asserts $\overline{\text{MUTE}}$, which allows the PCM output clocks to start. Because $\overline{\text{PLAY}}$ is deasserted, PCMDATA out will be zero (see Table 1). With $\overline{\text{MUTE}}$ asserted and $\overline{\text{PLAY}}$ deasserted, the host can begin supplying data and fill the pipe while the D/A converter is initializing. After the required number of clocks to initialize the D/A, the host can assert $\overline{\text{PLAY}}$ and deassert $\overline{\text{MUTE}}$.

Table 1. Mute and Play Functional Summary

MUTE	PLAY	FUNCTION
Deasserted	Deasserted	Stops output clocks and PCMDATA output. LRCLK completes its current cycle and stops. The SCLK completes the last cycle for the low period of the LRCLK and stops. PCMDATA stops synchronous to LRCLK. Decoding stops when all internal buffers are full. At this time, $\overline{\text{REQ}}$ goes high and the ’AV110 stops accepting data. When PLAY is reasserted, PCMDATA output resumes where it left off, no data is lost.
Deasserted	Asserted	Normal decoding and playing
Asserted	Deasserted	Stops outputting data from PCM buffer; PCMDATA output is forced low synchronous to LRCLK. SCLK and LRCLK are not stopped. Decoding stops when all internal buffers are full. At this time, the $\overline{\text{REQ}}$ goes high and the ’AV110 stops accepting data. When PLAY is reasserted, PCMDATA output resumes where it left off, no data is lost.
Asserted	Asserted	Decoding and muting (soft mute). The PCMDATA output gradually decays to zero. Decoding continues as normal. When the PCMDATA output is low, PCM data is internally consumed as if it were being output at PCMDATA.

NOTE: MUTE is asserted when either $\overline{\text{MUTE}}$ is low or the MUTE register is high. PLAY is asserted when both $\overline{\text{PLAY}}$ is low and the PLAY register is high.

PCM output interface

The decoded audio data is output in a serial PCM data format. Output precision is selectable to be either 16 bits/word or 18 bits/word by setting the output precision select register (PCM_18). The data may be output either with the most significant bit first or least significant bit first as selected by the contents of the output order select register (PCM_ORD). When 18-bit data is selected, 24 bits of PCM data is output for each channel. The data-in-front (DIF) register is used to select 18-bit data in front (at the beginning) or 18-bit data in the back (or end) of the 24 bits (see Figure 8 through Figure 10).

The MPEG audio decoder requires a clock input (PCMCLK) that is externally synchronized to the compressed audio bit stream. This clock can be at the actual PCMDATA output bit rate or it can be an integer multiple of the bit rate. The decoder derives the PCM bit clock (SCLK) from this input (PCMCLK) by dividing it by the contents of the divider value register (PCM_DIV). This value can be an integer from 1 to 32 and allows the use of oversampling D/A converters. Values of SCLK and LRCLK are:

SCLK = (PCMCLK) / (PCM_DIV)
LRCLK = (SCLK) / (32); for 16-bit PCM output
LRCLK = (SCLK) / (48); for 18-bit PCM output

Table 2. Typical PCMCLK Values

LRCLK SAMPLING FREQUENCY (kHz)	16-BIT PCM WORD LENGTH		18-BIT† PCM WORD LENGTH	
	SCLK (MHz)	PCMCLK PCM_DIV = 8 (MHz)	SCLK (MHz)	PCMCLK PCM_DIV = 8 (MHz)
32	1.024	8.192	1.536	12.288
44.1	1.4112	11.2896	2.1168	16.9344
48	1.536	12.288	2.304	18.432

† With 18-bit PCM word lengths, 24 bits are output for each channel.

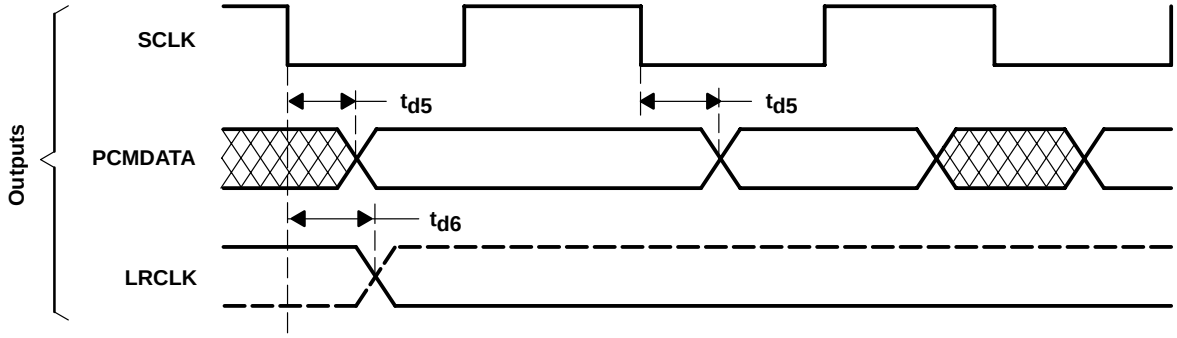


Figure 7. Serial PCM Data-Out Timing

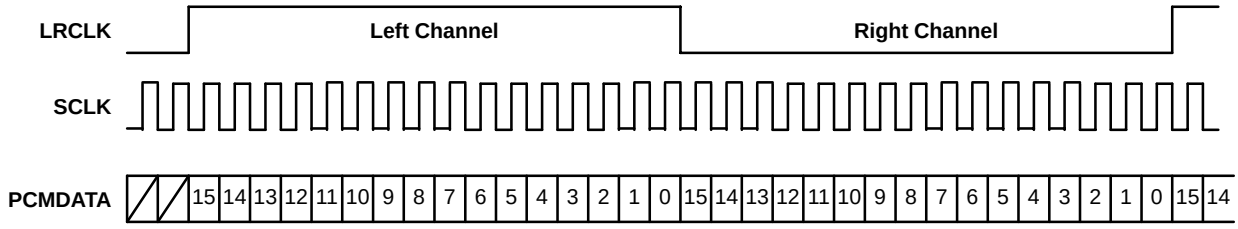


Figure 8. 16-Bit PCM Data Output (PCM_ORD = 0)

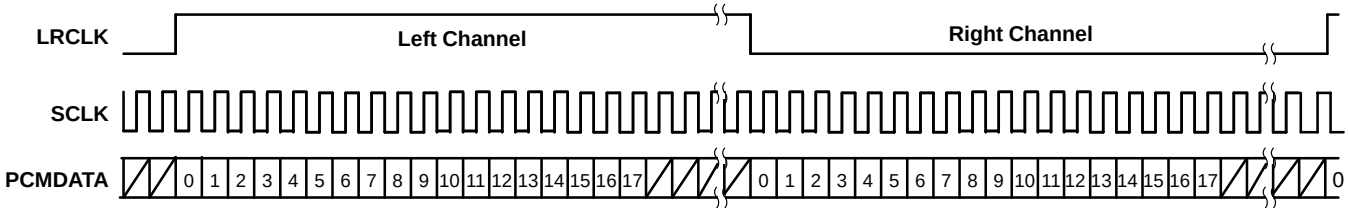


Figure 9. 18-Bit PCM Data Output (DIF = 1, PCM_ORD = 1)

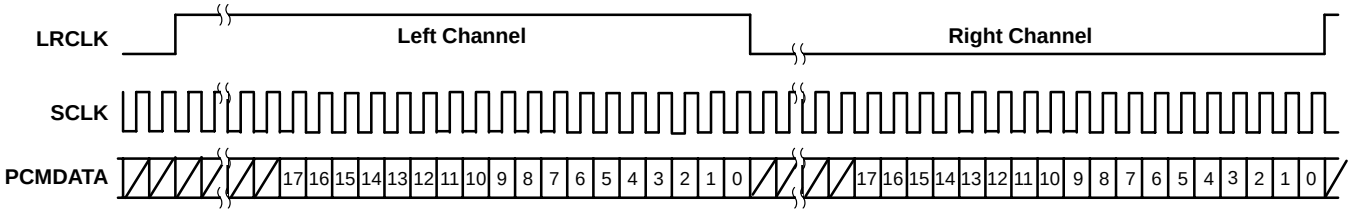


Figure 10. 18-Bit PCM Data Output (DIF = 0, PCM_ORD = 0)

audio/video synchronization

The ’AV110 extracts from the bit stream all information necessary for synchronization of the audio and video bit streams. At the packet level, it extracts the presentation time stamp (PTS) and makes it available to the host. An interrupt is generated when the first bit of the frame associated with the PTS is at the PCM output. This allows the host to control the presentation of the audio data with the repeat and skip register (and possibly mute and play) commands and to eliminate any drift between the PCM clock and the MPEG system clock.

At the full-MPEG system level, the audio decoder also extracts the system reference clock (SRC) value. An internal reference clock (IRC) is driven by the 90-kHz local system clock input. This IRC is optionally initialized by the SRC extracted from the bit stream. Each time a new SRC is received, the value of the IRC is stored in the IRC register. The host then reads both values and makes the required adjustment. The IRC counter value is not loaded into the IRC register for PTS to IRC comparisons. However, the present IRC counter value can be read by accessing the IRC_CNT register in response to a PTS interrupt or to a low level at the $\overline{\text{PTS}}$ output. The host can then take into account the time required to read the IRC counter value when comparing PTS to IRC.

bit-stream synchronization

The compressed-input bit stream must be synchronized before the decompression step begins. This is done by looking for synchronization words inserted into the data stream at encoding. Synchronization must be done both at the audio frame and at the system layer level (if present). The actions taken by the ’AV110 on initial synchronization acquisition and recovery after synchronization loss are similar.

At the system level, the audio decoder looks for a valid start code, with a bit-by-bit search. Once found, it continues to search for a system reference clock (SRC) and a valid audio packet. Once an audio packet is found, the audio decoder extracts the PTS, if present, and starts the audio bit stream synchronization described below.

At the audio frame level, a nonunique synchronization word is at the beginning of the header. The ’AV110 attempts to synchronize with a bit-by-bit search for this word. When found, the action taken depends on the contents of the SYNC_LCK and LATENCY registers.

The SYNC_LCK register specifies when synchronization can be considered as locked. The LATENCY register is used to enable a precheck for false synchronization words or missing data in a frame before that frame is decoded. When LATENCY is set to 1, a synchronization word is considered valid only after its associated header information is proven to point to the next synchronization word. If the next synchronization word is not found, the search for a new synchronization word starts at the beginning of the erroneous frame. When LATENCY is set to 0, a synchronization word is considered valid before reading the rest of the header. If the header information is incorrect or if data is missing, the subsequent synchronization word may not be found resulting in a branch to synchronization recovery.

If LATENCY is set to 0 (low) and SYNC_LCK contains 0, the ’AV110 goes to the locked state after the first synchronization word is found and starts decoding the frame.

If LATENCY is set to 1 and SYNC_LCK contains 0, the ’AV110 calculates where the next synchronization word should be and looks for it in the incoming data stream. If found in the right place, the ’AV110 goes to the locked state and decoding begins with the initial frame. If not found, a bit-by-bit search is entered again.

If LATENCY is 1 and SYNC_LCK contains an integer N (from 1 to 3), the ’AV110 determines the presence of valid synchronization words in N+2 consecutive frames before it goes to the locked state. The synchronization error-concealment step consumes all the data (N frame) before decoding is started with the data in the N+1th frame.

bit-stream synchronization (continued)

If LATENCY is 0 and SYNC_LCK contains an integer N (from 1 to 3), the ’AV110 determines the presence of valid synchronization words in N+1 consecutive frames before it goes to the locked state. The synchronization error-concealment step consumes all the data (N frame) before decoding is started with the data in the N+1th frame.

error recovery and concealment

The ’AV110 attempts to recover from errors it detects and has a number of user-selectable error-concealment modes. Errors may be detected by a bad CRC or by a loss of synchronization. Concealment is similar in both cases but may be selected independently by setting the CRC_ECM and SYNC_ECM registers. These registers have the following functions:

CRC_ECM 00 = CRC detection is disabled. The ’AV110 ignores the CRC that may be present in the audio header.

01 = CRC calculation is enabled. If the calculated CRC value does not agree with the CRC in the header, the decoder mutes the audio associated with the frame.

10 = CRC calculation is enabled. If an error is detected, the action depends on the hardware configuration. If external DRAM is present, the last valid audio frame is repeated. If successive frames are also faulty, the ’AV110 mutes the faulty frames in layer two or repeats the last good frame up to three times in layer one, and then mutes the faulty frames. If there is no external memory, the audio decoder defaults to mode 01.

11 = CRC calculation is enabled. If an error is detected, the invalid frame is skipped. If external memory is present, this occurs rapidly. If there is no external buffer, there may be partial frame muting depending on the state of the device’s internal buffers. In layer one, up to three consecutive frames can be skipped. Subsequent invalid frames are muted. In layer two, one frame can be skipped and the next invalid frame is muted.

SYNC_ECM 00 = Synchronization errors are ignored. This selection can be used when the audio output is muted. If synchronization status is ignored, the audio stream may not be properly aligned and the probability of generating usable audio output is remote.

01 = Mute on synchronization error. The audio output is muted when a loss of synchronization is detected and the ’AV110 enters synchronization-recovery mode.

10 = Upon detection of loss of synchronization, the ’AV110 enters the synchronization-recovery mode. Concealment action is identical to that of CRC error: repeat last valid frame once if layer two, three times if layer one, and mute thereafter. If no external memory is present, the output is muted.

11 = In case of synchronization loss, the audio decoder skips the audio input until a valid synchronization is found. Muting occurs only if there is an output buffer underflow.

Synchronization error concealment is active only when SYNC_LCK is greater than zero. Figure 11 shows the overall input-processing flow. Figure 12 and Figure 13 show synchronization-lock-recovery and error-concealment flows.

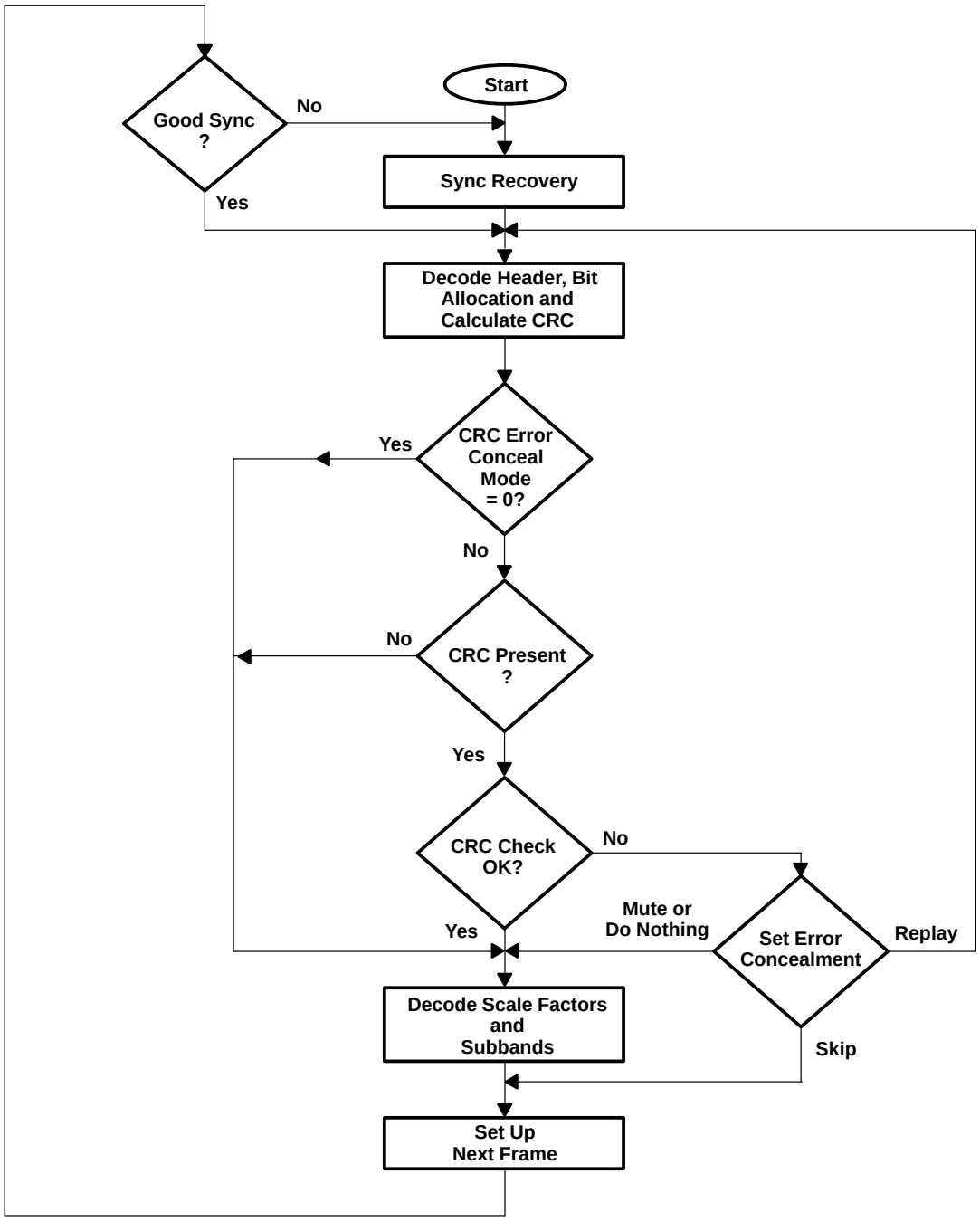


Figure 11. Input-Processor Flowchart

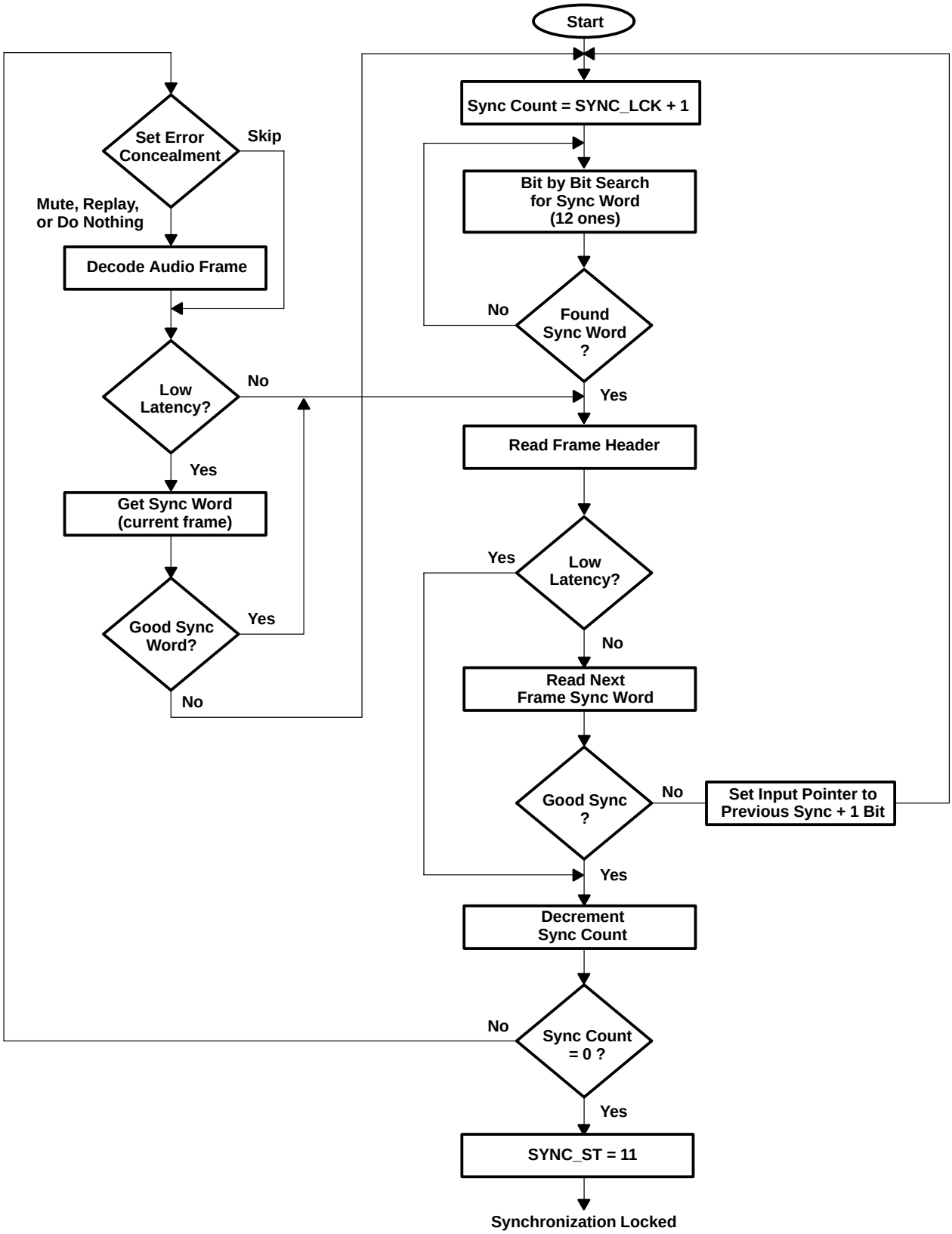


Figure 12. Synchronization-Lock-Recovery Flowchart

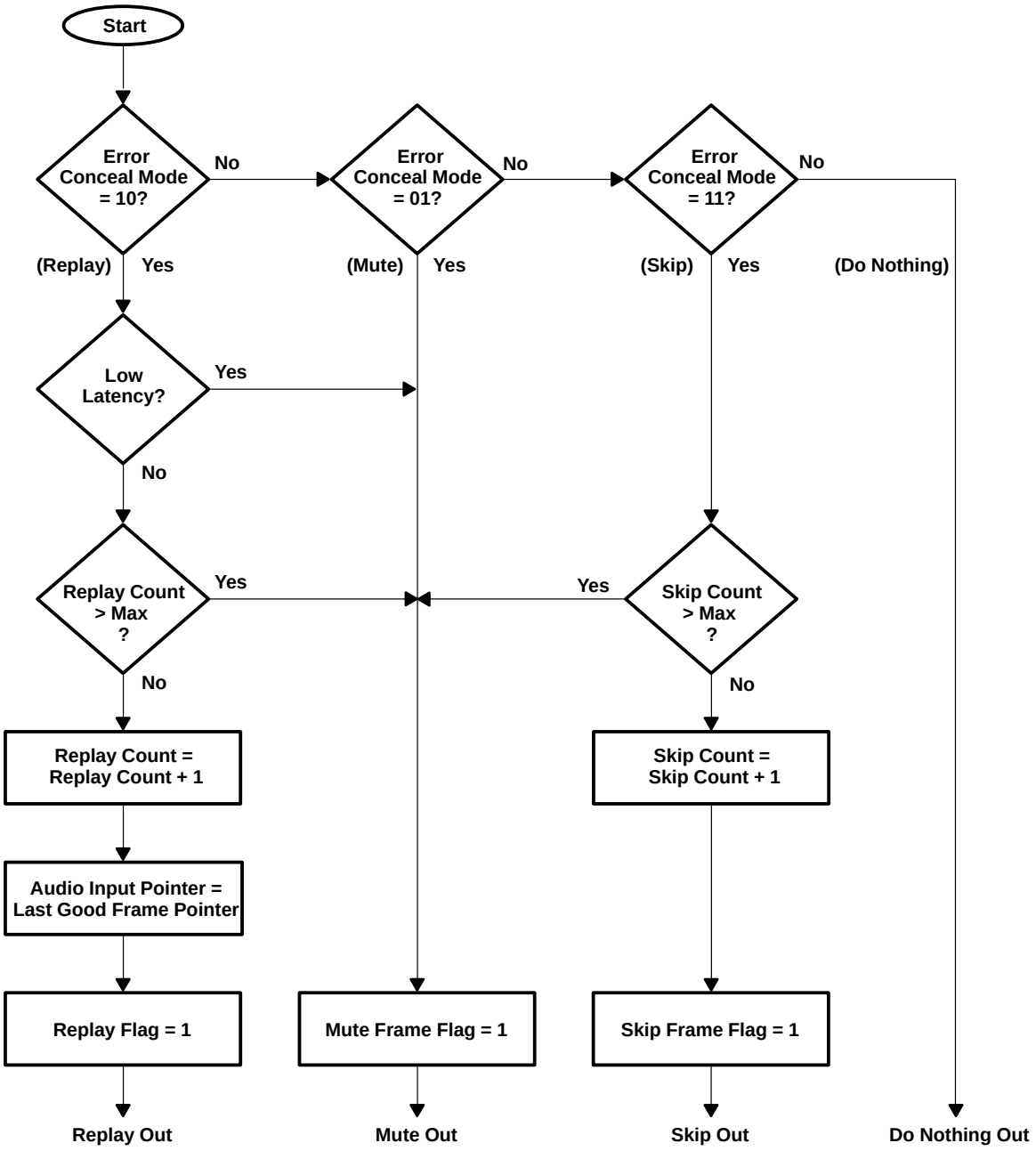


Figure 13. Error-Concealment Flowchart

ancillary data handling

The handling of ancillary data is controlled by the contents of the ancillary data register (ANC) and the ancillary data available (ANC_AV) registers in conjunction with interrupt request bits 6 and 7. If interrupts 6 and 7 are masked, ancillary data is ignored. If interrupt 6 is enabled, incoming ancillary data is placed in an internal buffer. This buffer is treated as a FIFO; it always holds the last 32 bits. If interrupt 7 is masked, the oldest data is replaced with new data on a bit-by-bit basis. If interrupt 7 is enabled, a full interrupt is generated when the FIFO is full and further processing of audio data is halted until either the data is read or interrupt 7 is masked.

The ancillary data available (ANC_AV) register always holds the number of bits available in the ancillary buffer. Interrupt 6 is generated when either 16 bits of data are available or the end of a frame is reached. Interrupt 7 is generated when 32 bits of data are available, and all processing stops until the ANC_AV register is read.

Before reading the ANC register, the host must read the ANC_AV register to determine the number of valid ancillary data bits available. The register must be read, even if the number of valid bits is known. When the ANC_AV register is read, the contents of the internal ancillary FIFO are transferred to the ANC register and the ANC_AV register is cleared. The ancillary data bits are loaded into the least significant bits of the ANC register. The host can then read the specified number of bits by accessing the ANC register addresses. This sequence ensures that the data is available for reading without conflict with any additional data coming in. If the ANC_AV register is read a second time, the ANC register is updated with any new data, whether the host has completed reading the ANC register or not. All 32 bits of the ANC register are overwritten each time ANC_AV is read.

external DRAM

The ’AV110 is designed to interface with a fast page-mode 256K×4 DRAM (100 ns maximum). The ’AV110 uses only the enhanced page-mode read and write cycles and the automatic $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle timing. The ’AV110 provides a 665-µs minimum power-up pause with 16 initialization cycles. The ’AV110 is designed to support a 1M×4 DRAM (TMS44400) in the event that the 1M×4 DRAM becomes less expensive than the 256K×4. When a 1M×4 DRAM is used, only 256K×4 of the 1M×4 is utilized by the ’AV110. Upon power up, the ’AV110 determines if external DRAM is present. If a DRAM is present, the DRAM_EXT register is set and the ’AV110 uses it as an input buffer. The following lists the trade-offs of using external DRAM versus internal SRAM only for the input buffer.

with DRAM

- Audio can be buffered for audio/video synchronization purposes
- Allows more robust error concealment
- Both register skip and register repeat functions are supported
- Synchronization look ahead (high latency) is supported

without DRAM

- Input buffer is only 256 bytes
- A register repeat command causes a muted frame to be inserted
- No synchronization look ahead (low latency)
- Buffer almost empty (BALE) and buffer almost full (BALF) interrupts still work, but $\overline{\text{REQ}}$ should be monitored

system clock

The system clock (OSCIN) can be totally asynchronous with respect to the other ’AV110 clocks and to the input data rate. OSCIN can be driven from an oscillator as a clock input, or a crystal can be used to generate this clock. If a crystal is used, it should be a fundamental-mode, parallel-resonant, 15-pF (typical) crystal connected to OSCIN and OSCOUT. The crystal needs two 30-pF capacitors to ground and a 91-kΩ resistor across the crystal as shown in Figure 14.

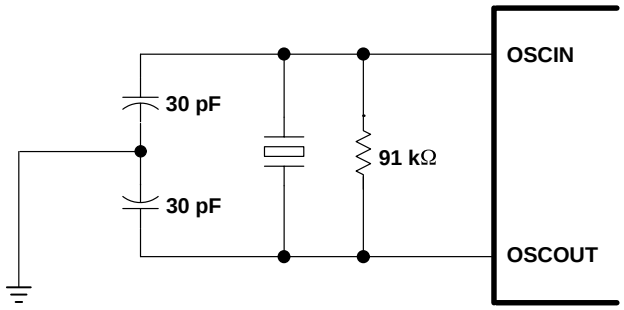


Figure 14. Crystal Circuit

audio bypass

The ’AV110 has an audio-bypass feature that allows 16-bit PCM data to be loaded into the device and passed through to the PCMDATA output. To use the audio-bypass feature, the STR_SEL register must be set to the bypass mode and then a reset or restart sequence must be executed. Once the $\overline{\text{REQ}}$ output goes low, PCM data can be loaded into the device directly. The data is loaded exactly the same as compressed data, using one of the three loading mechanisms available. The data can be entered at up to the maximum burst rate. The rate control features of the device can be used to check for buffer full and buffer empty. Blocks of 32 stereo samples (32 16-bit words left, 32 16-bit words right) must be loaded with the data ordered as follows: 2 bytes left, 2 bytes right, 2 bytes left, and so on. For each 2 bytes (left or right), the most significant byte is loaded first. If an incomplete block is loaded at the end, the entire block will not be output. PCM data starts to output after 4 blocks (512 bytes) have been loaded. The 18-bit PCM data is not supported for audio bypass.

To switch back to compressed data input, the STR_SEL register must be changed back to the proper input configuration and then a reset or restart sequence must be executed. The PCM underflow interrupt can be used to detect when all of the bypass data has been output.

decoding MPEG-2 streams

The ’AV110 accepts MPEG-2 frame data since it is the same as MPEG-1 frame data. In order for the ’AV110 to be able to accept MPEG-2 packet data, the MPEG-2 packets must be converted to MPEG-1 packets. The difference is in the packet headers; the MPEG-2 packet header must be converted to a MPEG-1 packet header that includes the PTS values. This allows the ’AV110 to extract the PTS values and present them at the appropriate time.

CONTROL AND STATUS REGISTERS†

register address allocation

REGISTER NAME	REGISTER ADDRESS (HEX)	ACCESS MODE
ANC		R
7:0	06	
15:8	07	
23:16	08	
31:24	09	
ANC_AV	6C	R
ATTEN_L	1E	R/W
ATTEN_R	20	R/W
AUD_ID	22	R/W
AUD_ID_EN	24	R/W
BALE_LIM		R/W
7:0	68	
14:8	69	
BALF_LIM		R/W
7:0	6A	
14:8	6B	
BUFF		R
7:0	12	
14:8	13	
CRC_ECM	2A	R/W
DATAIN	18	W
DIF	6F	R/W
DMPH	46	R
DRAM_EXT	3E	R
FREE_FORM		R/W
7:0	14	
10:8	15	
HEADER		R
7:0	5E	
15:8	5F	
23:16	60	
31:24	61	
INTR		R
7:0	1A	
15:8	1B	
INTR_EN		R/W
7:0	1C	
15:8	1D	
IRC		R
7:0	78	
15:8	79	
23:16	7A	
31:24	7B	

REGISTER NAME	REGISTER ADDRESS (HEX)	ACCESS MODE
IRC_CNT		R
7:0	54	
15:8	55	
23:16	56	
31:24	57	
32	58	
IRC_LOAD	7E	R/W
LATENCY	3C	R/W
MUTE	30	R/W
PCM_DIV		R/W
5:0	6E	
PCM_18	16	R/W
PCM_FS	44	R
PCM_ORD	38	R/W
PLAY	2E	R/W
PTS		R
7:0	62	
15:8	63	
23:16	64	
31:24	65	
32	66	
REPEAT	34	R/W
RESET	40	R/W
RESTART	42	R/W
SRC		R
7:0	72	
15:8	73	
23:16	74	
31:24	75	
32	76	
SIN_EN	70	R/W
SKIP	32	R/W
STR_SEL	36	R/W
SYNC_ECM	2C	R/W
SYNC_LCK	28	R/W
SYNC_ST	26	R
VERSION	6D	R

† All single-bit registers are accessed by the least significant data bit, SDATA0. All other bits, SDATA7 – SDATA1, are ignored.

ANC, ancillary data buffer, 31:24, 23:16, 15:8, 7:0 (09-08-07-06h)

A FIFO that holds the last 32 bits of ancillary data in the data stream. The ANC is updated only when the corresponding IRQ is enabled and after the ANC_AV register has been read.

ANC_AV, ancillary data available, 5:0 (6Ch)

Holds the number of bits of ancillary data available in the ANC buffer. This register must be read by the host before reading the ANC register.

ATTEN_L, left channel attenuator, 5:0 (1Eh)

Minimum = 0, maximum = 63 in 2-dB steps.

ATTEN_R, right channel attenuator, 5:0 (20h)

Minimum = 0, maximum = 63 in 2-dB steps.

AUD_ID, audio stream, 4:0 (22h)

Specifies 1 of 32 possible audio streams in the MPEG system or packet layer to be decoded. AUD_ID is ignored if AUD_ID_EN is not asserted.

AUD_ID_EN, audio stream ID enable, (24h)

0 = Audio stream ID is ignored.
1 = Audio stream ID is decoded and only the selected stream is decoded.

BALE_LIM, buffer almost empty limit, 14:8, 7:0 (69-68h)

Sets the almost empty limit for the input buffer. Values may be from 0000h to 6600h for DRAM (0000h to 003Dh for SRAM) and specifies the number of 32-bit words in the input buffer before INTR bit 3 is set. When using the internal 256-byte SRAM for the input buffer, it is recommended that $\overline{\text{REQ}}$ be monitored rather than the BALE_LIM and BALF_LIM interrupts.

BALF_LIM, buffer almost full limit, 14:8, 7:0 (6B-6Ah)

Sets the almost full limit for the input buffer. Values may be from 0000h to 6600h for DRAM (0000h to 003Dh for SRAM) and specifies the number of 32-bit words in the input buffer before INTR bit 4 is set.

BUFF, input buffer word counter, 14:8, 7:0 (13-12h)

Contains the amount of data being held in the input buffer in 32-bit words. Updated after every 32-bit data write to the input. (The input buffer refers to either the internal 256-byte SRAM or the optional DRAM.)

CRC_ECM, CRC error handling, 1:0 (2Ah)

00 = CRC detection is disabled.
01 = Mute on CRC error
10 = Repeat last valid frame. Repeat once if layer 2, three times if layer 1, mute thereafter. Valid with external memory only.
11 = Skip invalid frame

DATAIN, audio data input register, 7:0 (18h)

The audio data input register is used only if data is input in memory-mapped mode.

DIF, 18-bit data in front register, (6Fh)

Specifies where 18-bit PCM data output is located with respect to LRCLK and SCLK (see Figure 9 and Figure 10).

0 = Data is in the back or last 18 SCLKs.
1 = Data is in the front or first 18 SCLKs.

DMPH, deemphasis mode,1:0 (46h)

00 = None
01 = 50 /15 microseconds
10 = Reserved
11 = CCITT J.17

DRAM_EXT, memory status, (3Eh)

0 = Integral 256-byte SRAM only is being used for the input buffer.
1 = External DRAM memory only is being used for the input buffer. This bit is set by the 'AV110 during power up when external DRAM is present.

FREE_FORM, free format frame length, 10:8, 7:0 (15-14h)

Frame length in free format decoding. Should be set to 0 if length is unknown.

HEADER, frame header, 31:24, 23:16, 15:8, 7:0 (61-60-5F-5Eh)

Contains the frame header currently being decoded. This register is updated only when corresponding interrupt is enabled and the contents are retained until the register MSB has been read.

INTR, interrupt request register, 15:8, 7:0 (1B-1Ah)

BIT NO.	FUNCTION	SEE NOTE
15-12	Not used	—
11	Set when SRC is detected.	2
10	Set when deemphasis is changed.	3
9	Set when the sampling frequency is changed.	3
8	Set on PCM output buffer underflow	3
7	Set when ancillary data is full. Inhibits further placement of ancillary data into the FIFO until the data is read .	2
6	Set when ancillary data is registered.	3
5	Set when CRC error is detected.	3
4	Set when the input buffer is over the BALF_LIM.	3
3	Set when the input buffer is below the BALE_LIM.	3
2	Set when a valid PTS has been registered.	2
1	Set when a valid header has been registered.	2
0	Set upon a change in the synchronization status	2

NOTES: 1. Cleared when the interrupt request register is read or upon $\overline{\text{RESET}}$. This bit is **not** cleared by a RESTART.
2. Cleared when the corresponding data register is read or upon $\overline{\text{RESET}}$ or RESTART. These interrupts must be cleared for additional interrupts (of this type) to occur.
3. Cleared when the interrupt request register is read or upon $\overline{\text{RESET}}$ or RESTART.

INTR_EN, interrupt enable register, 15:8, 7:0 (1D-1Ch)

A 1 in any bit position will enable the corresponding bit in the INTR register.

IRC, internal reference clock, 32, 31:24, 23:16, 15:8, 7:0 (7C-7B-7A-79-78h)

Contains the value of the internal reference clock. This register is updated every time an SRC is detected (after an IRC_LOAD) provided the SRC interrupt is enabled in register INTR_EN.

IRC_CNT, internal reference counter register, 32, 31:24, 23:16, 15:8, 7:0 (58-57-56-55-54h)

This register contains the present internal reference count and is updated continuously by the CLK90 input.

IRC_LOAD, load internal reference clock, (7Eh)

0 = No action on IRC
1 = IRC counter is loaded with the decoded system reference clock (SRC) value. IRC_LOAD is then reset.

LATENCY, decoder latency selection, (3Ch)

0 = Low latency, less than 10 ms
1 = High latency, more than one frame time. High latency has more robust synchronization detection than low latency.This mode is provided to allow for the detection of a possible loss of synchronization prior to decoding each frame. (Synchronization look ahead). High latency is valid only with external DRAM.

MUTE, muting, (30h)

Enables the output of muted PCM data. Muting is enabled if *either* this register or the $\overline{\text{MUTE}}$ input line is asserted. Muting does not affect the audio decoding process.

0 = PCM data not muted
1 = PCM data muted

PCM_DIV, divider value, 5:0 (6Eh)

Sets the PCMCLK divider value to an integer in the range of 1 to 32.

PCM_18, output precision select, (16h)

0 = 16-bit PCM output
1 = 18-bit PCM output

PCM_FS, sampling rate, 1:0 (44h)

00 = 44.1 kHz
01 = 48 kHz
10 = 32 kHz
11 = Reserved

PCM_ORD, output order select, (38h)

0 = Most significant bit output first
1 = Least significant bit output first

PLAY, output decoded audio data, (2Eh)

Enables the output of decoded audio data. Output is enabled only if *both* this register and the $\overline{\text{PLAY}}$ input line are asserted. Does not affect the output of muted audio. When both $\overline{\text{PLAY}}$ and $\overline{\text{MUTE}}$ are deasserted, outputs SCLK and LRCLK stop switching and PCMDATA is forced low.

0 = Don't play
1 = Play

PTS, presentation time stamp, 32, 31:24, 23:16, 15:8, 7:0 (66-65-64-63-62h)

Contains the PTS associated with the frame currently being decoded. If the corresponding PTS interrupt is enabled, the contents are retained until the register MSB is read.

REPEAT, repeat next audio frame, (34h)

The decoder repeats the next audio frame and resets the REPEAT register. If external memory (DRAM) is not present, a muted frame is inserted. A zero should be written to this register during initialization.

0 = No repeat
1 = Repeat

RESET, reset decoder, (40h)

Resets the decoder. Equivalent to the assertion of the $\overline{\text{RESET}}$ input except that the MUTE and PLAY registers are not affected. Resets the interrupt register, locates and sizes external memory, flushes all data buffers, and then clears the reset register. A pin RESET is required after powerup.

0 = No reset, do not write this value
1 = Reset

RESTART, flush data buffers, (42h)

Flushes all data buffers. Has no effect on control registers, does not test memory, and does not clear the EOS interrupt request register bit. Upon completion, RESTART is cleared by the 'AV110.

0 = No restart
1 = Restart

SRC (32:0), system reference clock, 32, 31:24, 23:16, 15:8, 7:0 (76-75-74-73-72h)

Contains the value of the system reference clock. This register is updated every time an SRC is detected, provided the respective interrupt is enabled in register INTR_EN.

SIN_EN, serial input enable, (70h)

0 = Parallel data Input
1 = Serial data Input

SKIP, skip next audio frame, (32h)

The decoder skips (ignores) the next audio frame and resets the SKIP register. A zero should be written to this register during initialization.

0 = No skip
1 = Skip

STR_SEL, input configuration, 1:0 (36h)

00 = MPEG audio stream
01 = MPEG packet stream
10 = MPEG system stream
11 = Audio bypass

SYNC_ECM, synchronization error handling, 1:0 (2Ch)

00 = Ignore error
01 = Mute on synchronization error
10 = Repeat last valid frame. Repeat once if layer 2, three times if layer 1, mute thereafter. Valid with external memory only.
11 = Skip invalid frame

SYNC_LCK, good synchronization words, 1:0 (28h)

Contains the number of additional good-synchronization words to be found, after the first good-synchronization word, before changing to the locked state.

SYNC_ST, synchronization status, 1:0 (26h)

00 = Unlocked
10 = Attempting to recover lost synchronization
11 = Locked
This register is updated during each synchronization cycle.

VERSION, version number, 7:0 (6Dh)

Contains the version number of the ’AV110 being read.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 4)	–0.5 V to 6 V
Input voltage range, V_I, any input	–0.5 V to (V_{CC} + 0.5 V)
Output voltage range, V_O, any output	–0.5 V to (V_{CC} + 0.5 V)
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±20 mA
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 4: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		V_{CC} + 0.5	V
V_{IL}	Low-level input voltage		– 0.5		0.8	V
V_{OH}	High-level output voltage, $\overline{IRQOD}$				5.25	V
I_{OH}	High-level output current, any output except $\overline{IRQOD}$	and TDO			– 8	mA
		TDO			– 2	
I_{OL}	Low-level output current, any output	except TDO			8	mA
		TDO			2	
f_{clock}	Clock frequency	OSCIN	22		27	MHz
		$\overline{DSTRB}$ byte-parallel input mode			1.9	
		$\overline{DSTRB}$ bit-serial input mode			15	
		PCMCLK			48	
dt/dv	Input transition (rise or fall), any input		0		10	ns/V
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage, any output except $\overline{IRQOD}$	and TDO	V_{CC} = 4.75 V,	I_{OH} = – 8 mA	3.7			V
		TDO	V_{CC} = 4.75 V,	I_{OH} = – 2 mA	3			
V_{OL}	Low-level output voltage	except TDO	V_{CC} = 4.75 V,	I_{OL} = 8 mA			0.5	V
		TDO	V_{CC} = 4.75 V,	I_{OL} = 2 mA			0.5	
I_{OH}	High-level output current, $\overline{IRQOD}$		V_{CC} = 4.75 V,	V_{OH} = 5.25 V			10	µA
I_I	Input current		V_{CC} = 5.25 V,	V_I = V_{CC} or 0			±1	µA
I_{OZ}	Off-state output current		V_{CC} = 5.25 V,	V_O = V_{CC} or 0			±5	µA
I_O	Output current, TDI, TMS, $\overline{TRST}$, and TDO		V_O = 0			– 325	– 400	µA
			V_O = V_{CC} – 1.5 V			– 150	– 250	
I_{CC}	Supply current, operating		V_{CC} = 5.25 V	OSCIN = 24 MHz		105	180	mA
C_i	Input capacitance§		f = 1 MHz			8		pF
C_o	Output capacitance§		f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the capacitance at an input, output, or I/O terminal.

timing requirements over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)†

cycle times

		FIGURE	MIN	MAX	UNIT
t_{c1}	Write	4	100		ns
t_{c2}	Read	4	100		ns

pulse durations

		FIGURE	MIN	MAX	UNIT
t_{w1}	$\overline{\text{DSTRB}}$ low	2, 3	25		ns
t_{w2}	$\overline{\text{DCS}}$ low	4	25		ns
t_{w3}	$\overline{\text{DCS}}$ high	4	25		ns
t_{w4}	$\overline{\text{RESET}}$ low	6	200		ns

setup times

		FIGURE	MIN	MAX	UNIT
t_{su1}	$\overline{\text{REQ}}$ output low before $\overline{\text{DSTRB}}\downarrow$ or $\overline{\text{DCS}}\downarrow$	2, 3, 4	25		ns
t_{su2}	SIN before $\overline{\text{DSTRB}}\uparrow$	2	25		ns
t_{su3}	SDATA before $\overline{\text{DSTRB}}\uparrow$	3	25		ns
t_{su4}	R/$\overline{\text{W}}$ before $\overline{\text{DCS}}\downarrow$	4	25		ns
t_{su5}	SADDR before $\overline{\text{DCS}}\downarrow$	4	25		ns
t_{su6}	SDATA before $\overline{\text{DCS}}\uparrow$	4	25		ns
t_{su7}	$\overline{\text{WAIT}}$ output high before $\overline{\text{DCS}}\uparrow$	4	0		ns
t_{su8}	$\overline{\text{DCS}}$ high before $\overline{\text{DSTRB}}$ low	5	50		ns
t_{su9}	$\overline{\text{DSTRB}}$ high before $\overline{\text{DCS}}$ low	5	50		ns

hold times

		FIGURE	MIN	MAX	UNIT
t_{h1}	SIN after $\overline{\text{DSTRB}}$	2	5		ns
t_{h2}	SDATA after $\overline{\text{DSTRB}}\uparrow$	3	3		ns
t_{h3}	R/$\overline{\text{W}}$ after $\overline{\text{DCS}}\downarrow$	4	5		ns
t_{h4}	SADDR after $\overline{\text{DCS}}\downarrow$	4	5		ns
t_{h5}	SDATA after $\overline{\text{DSC}}\uparrow$	4	5		ns

† See Parameter Measurement Information for load circuit, voltage waveforms, and timing diagrams.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)†

propagation delay times

		FIGURE	MIN	MAX	UNIT
t_{pd1}	$\overline{DSTRB}\uparrow$ or $\overline{DCS}\uparrow$ to $\overline{REQ}$	3, 4		250	ns
t_{pd2}	$\overline{DCS}\downarrow$ to $\overline{WAIT}$ high	4		510	ns
t_{pd3}	OSCIN$\uparrow$ to DMPHx	—		35	ns
t_{pd4}	OSCIN$\uparrow$ to FSx	—		35	ns
t_{pd5}	OSCIN$\uparrow$ to PTS	—		35	ns
t_{pd6}	OSCIN$\uparrow$ to $\overline{BOF}$	—		35	ns
t_{pd7}	OSCIN$\uparrow$ to $\overline{IRQ}$	—		35	ns
t_{pd8}	OSCIN$\uparrow$ to $\overline{REQ}$ low	—		35	ns
t_{pd9}	OSCIN$\uparrow$ to SDATA	—		35	ns
t_{pd10}	OSCIN$\uparrow$ to WAIT high	—		35	ns
t_{pd11}	PCMCLK to SCLK	—		40	ns
t_{pd12}	PCMCLK to PCMDATA	—		40	ns
t_{pd13}	PCMCLK to LRCLK	—		40	ns

delay time relationships

		FIGURE	MIN	MAX	UNIT
t_{d1}	SDATA output before $\overline{WAIT}\uparrow$	4	5		ns
t_{d2}	$\overline{BOF}\downarrow$ to $\overline{BOF}\uparrow$ (pulse)	6	100		ns
t_{d3}	$\overline{IRQ}\downarrow$ to $\overline{IRQ}\uparrow$ (pulse)	6	100		ns
t_{d4}	$\overline{PTS}\downarrow$ to $\overline{PTS}\uparrow$ (pulse)	6	1000		ns
t_{d5}	PCMDATA after SCLK$\downarrow$	7		40	ns
t_{d6}	LRCLK after SCLK$\downarrow$	7		40	ns

enable times

		FIGURE	MIN	MAX	UNIT
t_{en1}	$\overline{DCS}\downarrow$ to SDATA	4	40	505	ns
t_{en2}	$\overline{DCS}\downarrow$ to $\overline{WAIT}$ low	4		20	ns

disable times

		FIGURE	MIN	MAX	UNIT
t_{dis1}	$\overline{DCS}\uparrow$ to SDATA	4		20	ns
t_{dis2}	$\overline{DCS}\uparrow$ to $\overline{WAIT}$	4		20	ns

† See Parameter Measurement Information for load circuit, voltage waveforms, and timing diagrams.

DRAM interface

		ALT. SYMBOL	FIGURE	MIN	MAX	UNIT
$t_{c(P)}$	Cycle time, page mode read or write	t_{PC}	15, 16	65		ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	15, 16	60		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	15, 16	15		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	15, 16	30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (refresh cycle)	t_{CSR}	17	15		ns
$t_{d(RCLH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (refresh cycle)	t_{CHR}	17	40		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (refresh cycle)	t_{RPC}	17	10		ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address	t_{RAD}	15, 16	25		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	15, 16	115		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	t_{RCD}	15, 16	30		ns
$t_{h(CA)}$	Hold time, column address after $\overline{CAS}$ low	t_{CAH}	15, 16	25		ns
$t_{h(CHrd)}$	Hold time, $\overline{W}$ high after $\overline{CAS}$ high, read	t_{RCH}	15	10		ns
$t_{h(CLW)}$	Hold time, $\overline{W}$ low after $\overline{CAS}$ low, write	t_{WCH}	16	25		ns
$t_{h(D)}$	Hold time, D3–D0 after $\overline{CAS}$ low	t_{DH}	16	25		ns
$t_{h(RA)}$	Hold time, row address, after $\overline{RAS}$ low	t_{RAH}	15, 16	20		ns
$t_{h(RCLA)}$	Hold time, column address, after $\overline{RAS}$ low	t_{AR}	15, 16	90		ns
$t_{h(RHrd)}$	Hold time, $\overline{W}$ high after $\overline{RAS}$ high, read	t_{RRH}	15	10		ns
$t_{h(RLD)}$	Hold time, D3–D0 after $\overline{RAS}$ low	t_{DHR}	16	90		ns
$t_{h(CCLA)}$	Hold time, from $\overline{CAS}$ precharge, $\overline{RAS}$	t_{RHCP}	15	60		ns
$t_{h(RO)}$	Hold time, $\overline{RAS}$ low after $\overline{OE}$ low	t_{ROH}	15	40		ns
t_{rf}	Refresh time interval	t_{REF}			6	ms
$t_{su(CA)}$	Setup time, column address before $\overline{CAS}$ low	t_{ASC}	15, 16	10		ns
$t_{su(D)}$	Setup time, D3–D0 before $\overline{W}$ low	t_{DS}	16	10		ns
$t_{su(RA)}$	Setup time, row address before $\overline{RAS}$ low	t_{ASR}	15, 16	1		ns
$t_{su(rd)}$	Setup time, $\overline{W}$ high before $\overline{CAS}$ low, read	t_{RCS}	15	10		ns
$t_{su(WCH)}$	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	t_{CWL}	16	30		ns
$t_{su(WCL)}$	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	t_{WCS}	16	10		ns
$t_{su(WRH)}$	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	t_{RWL}	16	30		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	15, 16	20		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	15, 16	30		ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge)	t_{RP}	15, 16, 17	90		ns
$t_{w(RL)P}$	Pulse duration, $\overline{RAS}$ low, page-mode	t_{RASP}	15, 16	200		ns
$t_{w(WL)}$	Pulse duration, write	t_{WP}	16	60		ns

requirements for fast page-mode DRAM (specified by DRAM manufacturer)

		ALT. SYMBOL	FIGURE	MIN	MAX	UNIT
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}	15		25	ns
$t_{a(CA)}$	Access time from column address	t_{CAA}	15		50	ns
$t_{a(O)}$	Access time from $\overline{OE}$ low	t_{OEA}	15		30	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low	t_{RAC}	15		100	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	t_{OFF}	15	0	25	ns
$t_{dis(O)}$	Output disable time after $\overline{OE}$ high	t_{OEZ}	15	0	25	ns

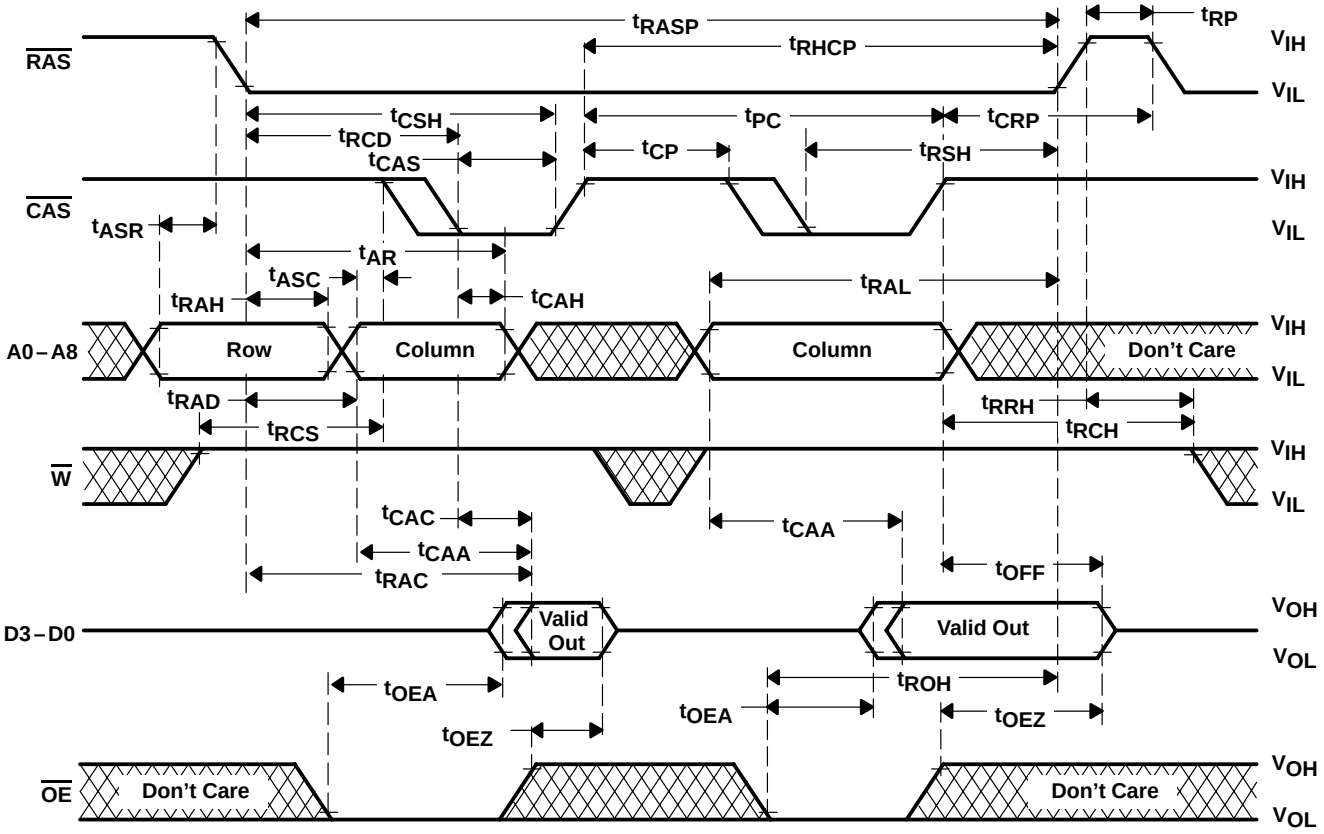


Figure 15. Enhanced Page-Mode Read Cycle Timing

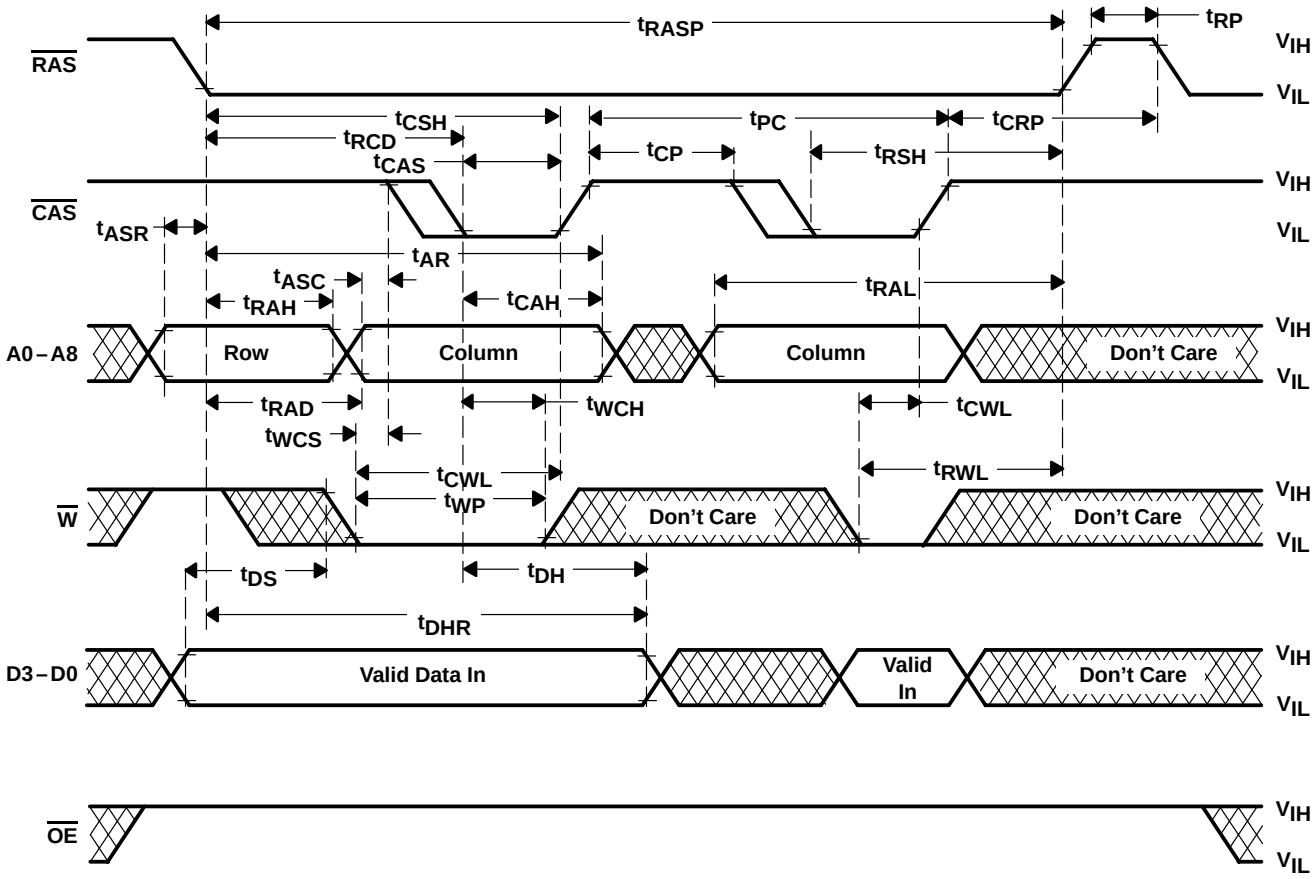


Figure 16. Enhanced Page-Mode Write Cycle Timing

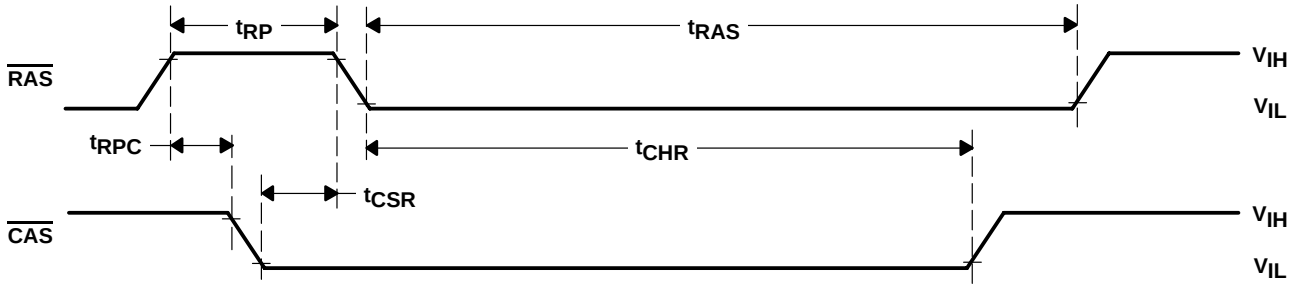


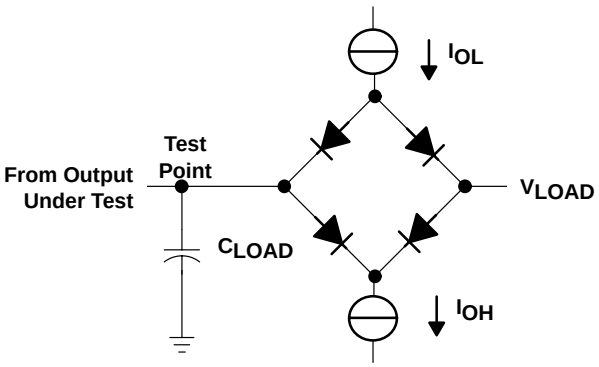
Figure 17. Automatic (CAS-before-RAS) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

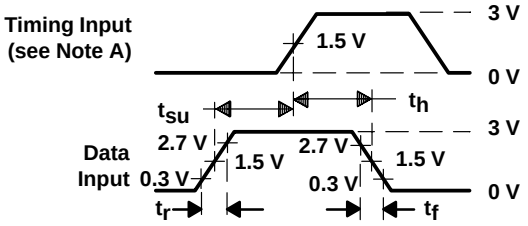
TIMING PARAMETERS		C_{LOAD}† (pF)	I_{OL} (mA)	I_{OH} (mA)	V_{LOAD} (V)
t_{en}	t_{PZH}	65	8	– 8	0
	t_{PZL}				3
t_{dis}	t_{PHZ}	65	8	– 8	1.5
	t_{PLZ}				
t_{pd}, t_d		65	8	– 8	‡

† C_{LOAD} includes the typical load circuit distributed capacitance.

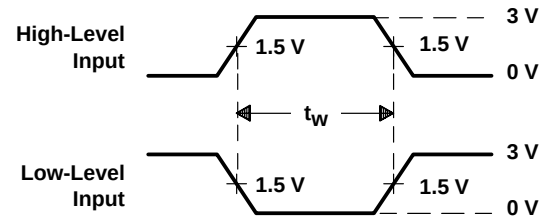
‡ $\frac{V_{LOAD} - V_{OL}}{I_{OL}}$ = 50 Ω, where V_{OL} = 0.6 V, I_{OL} = 8 mA



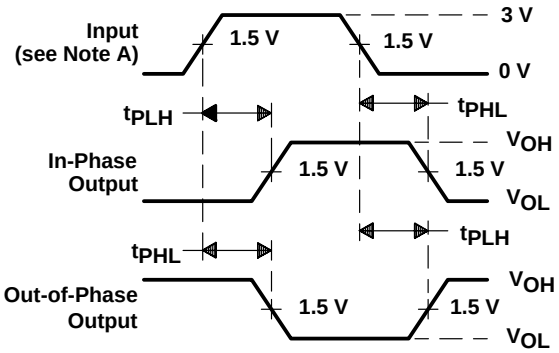
LOAD CIRCUIT



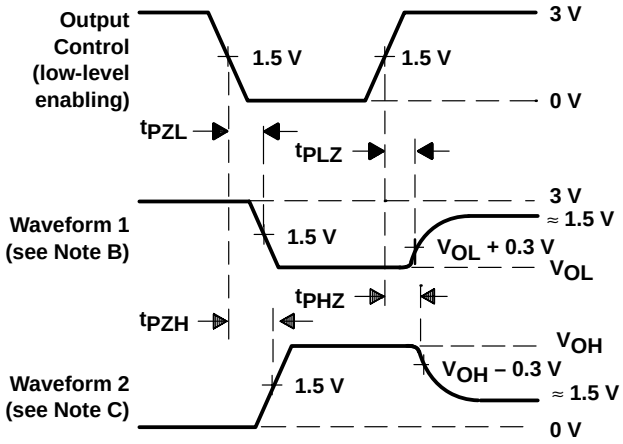
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



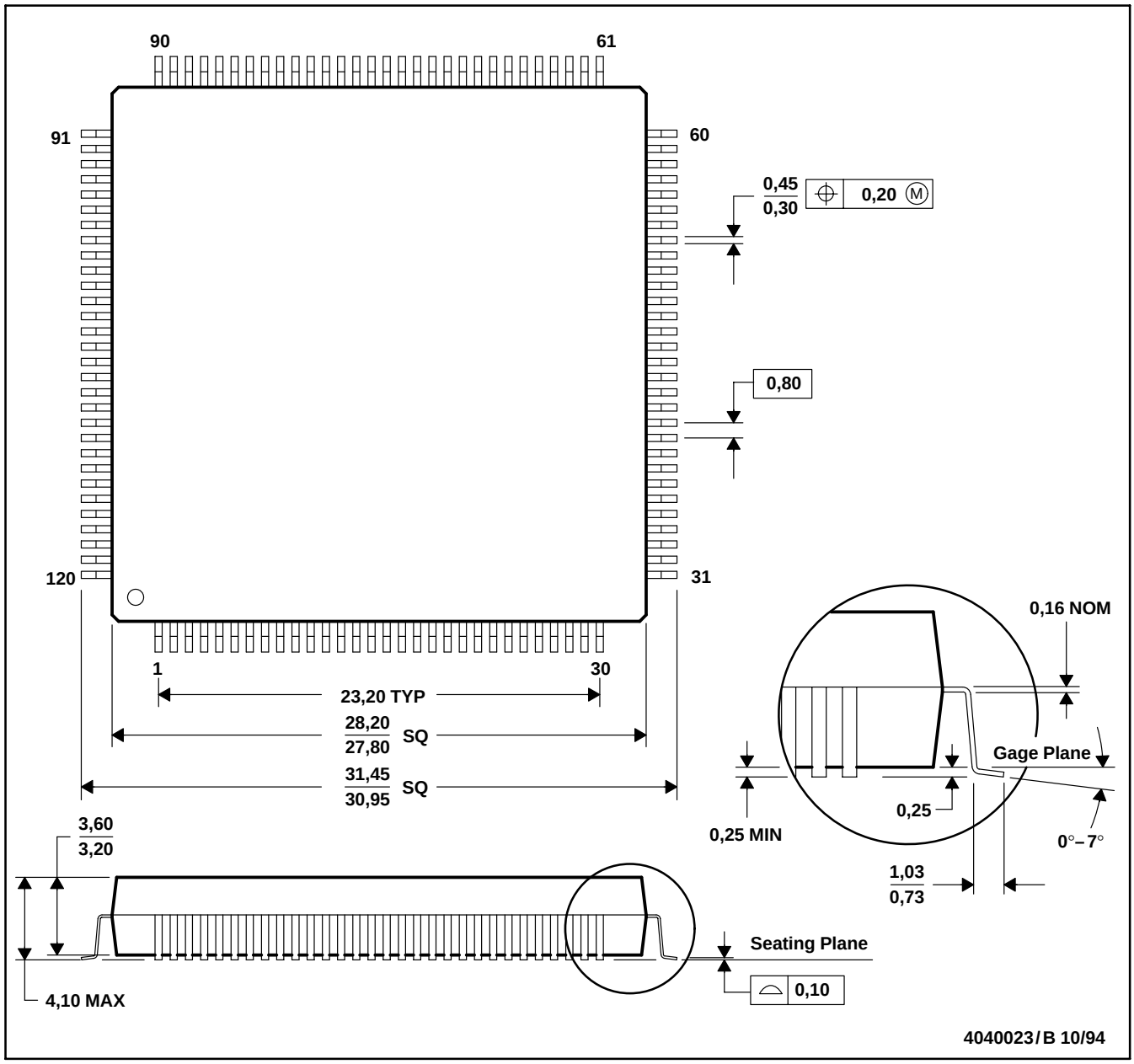
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by pulse generators having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, $t_r \le 6$ ns, $t_f \le 6$ ns.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
C. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. For t_{PLZ} and t_{PHZ}, V_{OL} and V_{OH} are measured values.

Figure 18. Load Circuit and Voltage Waveforms

MECHANICAL DATA

PBM (S-PQFP-G120) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-022

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