- **TMS320C2x CPU Source-Code Compatible**
- **Source Code is Upward Compatible to the TMS320C5x Family of DSPs**
- **35-ns Instruction Cycle Time (28.6 Million Instructions Per Second (MIPS)) at 5-V Operation**
- **50-ns Instruction Cycle Time (20 MIPS) at 3-V Operation**
- **T320C2xLP Core Includes:**
  - **T320C2xLP CPU**
  - **544 Words by 16 Bits of Internal Dual-Access RAM (DARAM)**
  - **Logic Interface**
  - **Memory Interface**
  - **Phase-Locked Loop (PLL)**
  - **Test and Emulation Logic**
- **Power-Down (IDLE) Mode**
- **Input Clock Options**
  - **Multiply-by-One**
  - **Multiply-by-One-and-One-Half**
  - **Multiply-by-Two**
  - **Multiply-by-Three**
  - **Multiply-by-Four**
  - **Divide-by-Two**
- **On-Chip Scan-Based Emulation (IEEE Standard 1149.1† Boundary-Scan Logic)**
- **Low Power Dissipation**
  - **1.9 mA/MIPS at 5-V Operation**
  - **1.1 mA/MIPS at 3-V Operation**
- **The T320C2xLP Core Is Designed Using Static Logic**
  - **All Logic And Buses are Latched Each Cycle**
  - **Logic Can Be Run at Any Clock Frequency**
  - **Clock Frequency can be Slowed or Even Stopped to Lower the Power Requirements During Off-Peak Task Management**
  - **Suitable for Battery-Operated Applications**

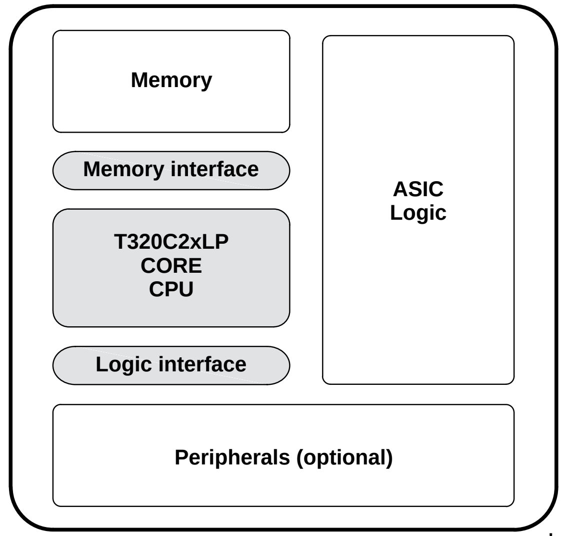

Figure 1. Typical Configuration of a cDSP‡

- **Memory Options**
  - **Single-Access RAM (SARAM)**
  - **DARAM**
  - **ROM**
  - **FLASH**
  - **Compiled RAM**
  - **Compiled ROM**
- **Peripheral Options**
  - **Complete Library of Logic and Analog Peripherals Targeted for the Hard Disk Drive, Wireless Communications, Automotive, and Multimedia Markets**
  - **Customer-Designed ASIC Logic**
- **Harvard Architecture—CPU Addresses Three Memory Spaces**
  - **Program Memory—Up to 64K Words by 16 Bits**
  - **Data Memory—64K Words by 16 Bits of Local Data Memory and 32K Words by 16 Bits of Global Data Memory**
  - **I/O Ports—64K Words by 16 Bits**
- **T320C2xLP Core is Designed Specifically for the Texas Instruments (TI™) ASIC Library**
  - **Fully Process Compatible With the TGC 2000 CMOS Gate-Array and TSC2000 Standard-Cell ASIC Libraries**
  - **Simulation Models are Available**

† IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture.
‡ Only the shaded components in Figure 1 are described in this data sheet.
cDSP and TI are trademarks of Texas Instruments Incorporated.

description

The T320C2xLP cDSP core is a member of the TI line of customizable digital signal processors (cDSPs). cDSPs provide a simple and effective method for reducing a system by merging TI's digital signal processors with TI application-specific integrated circuit (ASIC) gate-array or standard cell products. TI's ASIC design environment enables logic designers to combine custom logic with cDSP cores, other digital hardware macros, and linear hardware macros. This enables the designer to reduce part or all of a system design to a single device to improve performance and reliability while reducing system cost, hardware size, and power consumption.

The T320C2xLP core is a high-performance cDSP designed specifically for use as a hardware macro for integration with ASIC logic. It is process-compatible with the TGC/TSC 2000 ASIC libraries, providing maximum performance with minimal power consumption. The T320C2xLP's power requirements are minimized by its static logic design - all logic and buses are latched each cycle, allowing the clock frequency to be slowed or stopped to lower power consumption.

The T320C2xLP core consists of the T320C2xLP core CPU and two interface buses: a memory bus and a logic-interface bus. The memory bus interfaces to the ROM, RAM, flash memory, or EPROM required for a specific application. The logic bus interfaces to customer-designed ASIC logic, including on-chip or external ASIC logic and peripherals.

Like all TI '320 series DSPs, the T320C2xLP is implemented in a Harvard architecture, which uses multiple memory spaces to enable instruction and data fetches to be performed in parallel, allowing single-cycle instructions. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over three separate address/data buses. The buses and the necessary bus-control signals are included in the memory interface.

port diagram