Abridged Version

Silicon Systems®

A Texas Instruments Company

SSI 32C9810

Ultra SCSI Interface Controller
260 Mbit/s, Headerless Support

Prototype

July 1997

DESCRIPTION

The SSI 32C9810 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an Ultra SCSI disk drive. The SSI 32C9810 architecture includes an advanced and highly automated Ultra SCSI (Fast-20) Interface with a maximum host transfer rate of 40 MB/s, a fully integrated Buffer Manager with a 16-bit wide memory interface supporting concurrent full speed transfers on both disk and host interfaces, a high performance Disk Formatter with an 8-bit wide NRZ channel interface with maximum disk transfer rate of 260 Mbit/s and headerless operation, programmable Reed-Solomon ECC Logic supporting up to 5 bursts of correction and an embedded 8-bit RISC engine called the Queue Transmogrifier. The SSI 32C9810 maximizes Ultra SCSI performance while minimizing processor intervention.

The highly automated ECC Logic is guaranteed to correct all correctable errors in real time and provides programmable 144-bit to 272-bit Reed-Solomon ECC capability. It is programmable to either 3-burst or 5-burst correction and it can correct up to 120-bit bursts.

The SSI 32C9810 is one of the latest in a product line of sophisticated interface controllers, and its unique headerless scheme increases drive storage capacity. The Silicon Systems Interface Controller family is shown in Figure 1. All members are based on a common architecture, which allows reusability of major portions of firmware. Other Silicon Systems interface controllers include the SSI 32C9210 headerless ATA-3 Interface Controller, with a maximum host transfer rate of 16.6 MB/s and a maximum disk transfer rate of 200 Mbit/s.

The high level of integration within the SSI 32C9810 provides a major reduction in parts count when building an Ultra SCSI drive system. The SSI 32C9810 may be combined with the following components to create a complete, cost-efficient, high performance disk drive solution:

- SSI 32R2110R preamplifier
- SSI 32P4910 or 32P4920 PRML read channel (8/9)
- SSI 32H6826 servo/spindle controller or SSI 32H6840 with integrated DSP
- Processor
- Buffer memory DRAM

FEATURES

SCSI BUS INTERFACE

- **Full SCSI-2 and SCSI-3 compatibility**
- **Direct bus interface logic with on-chip 48 mA SCSI tolerant drivers**
- **Driver slew rate control and active negation**
- **Synchronous transfer rates up to 40 MB/s (FAST-20 or Ultra SCSI)**
- **Asynchronous transfer rates up to 10 MB/s**
- **Parity generation and checking**
- **8-bit or 16-bit SCSI arbitration**
- **Programmable offsets up to 15 words**
- **Control signals for external differential transceivers (160-pin package)**
- **Separate selection and transfer automation**
- **Automatic disconnection and reconnection from SCSI bus**
- **Hardware support for tagged command queuing**
- **Per initiator control; period, offset, and width**
- **Level 1 and Level 2 automatic SCSI configuration (SCAM) support**
- **Auto command mode (ACM) SCSI state machines perform high level SCSI sequences without processor intervention**

(continued)

FEATURES (continued)

- Hardware support for automatic queuing
- Automatic SCSI CDB size determination
- Sixteen words of data FIFO between SCSI Interface and Buffer Manager

QUEUE TRANSMOGRIFIER

- 8-bit embedded RISC engine
- Acceleration of SCSI queues
- LBA to PDA conversion
- Allows less powerful, less expensive processor

BUFFER MANAGER

- Supports up to 8 MB dynamic RAM (DRAM)
- High performance word-wide (16-bit) buffer data bus
- Separate host, disk, and processor buffer address pointers
- Flexible buffer segmentation which supports read caching, write caching, and extended read and write operations
- Supports extended data output (EDO) or fast page mode DRAMs
- 75 MB/s buffer bandwidth

DISK FORMATTER

- Unique headerless operation
- 4-bit/8-bit NRZ interface
- Automatic multiple sector data transfers
- Disk transfer rate support up to 260 MB/s
- Sector sizes of N • (512 + 2 • K) bytes where N = 1…8 and K = 0…7

ECC LOGIC

- Programmable 144-bit to 272-bit Reed-Solomon ECC
- No rotational delay required to perform corrections
- Guaranteed to correct all correctable errors in real time
- Programmable to 3 or 5 bursts
- Can correct up to 120-bit bursts
- “On-the-fly” transition from ECC generating/checking to reading/writing

PROCESSOR INTERFACE

- Supports both multiplexed or non-multiplexed address and data bus modes
- Supports many processors including most Intel® and Motorola® processors, and Texas Instruments TMS320C2xx DSPs
- Host and disk interrupts may be separate on two pins, or combined on a single pin

CLOCK TIMING GENERATOR

- Two on-chip frequency synthesizers for generating buffer timing and SCSI clocks from a common crystal oscillator or TTL clock
- Standby and sleep modes supported

OTHER FEATURES

- Available in 144-lead or 160-lead QFP and TQFP packages

BLOCK DIAGRAM