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SSI 32P4938A
PR4ML Read Channel with 16/17 ENDEC w/Thermal Asperity Suppression

December 1997

DESCRIPTION

The part is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Partial Response Class 4 (PR4) read channel for zoned recording hard disk drive systems with data rates from 80 to 240 Mbit/s.

Functional blocks include a bi-directional serial port, an automatic gain control amplifier, a programmable filter, an offset canceller, a peak detecting pulse qualifier, an adaptive transversal filter, a Viterbi qualifier for maximum likelihood detection, a 16/17 GCR ENDEC, a data synchronizer, a time base generator, and thermal asperity detector and suppression circuits.

The part requires a single +5 V power supply. The part utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which results in a high performance device with low power consumption.

FEATURES

GENERAL

- **Register programmable data rates from 80 to 240 Mbit/s**
- **Sampled data read channel with Viterbi qualification**
- **Programmable filter for PR4 equalization**
- **Five tap transversal filter with adaptive PR4 equalization**
- **16/17 GCR ENDEC for a 6% increase in code efficiency vs. 8/9**
- **Data Scrambler/Descrambler**
- **Presettable Precoder state**
- **Programmable write precompensation**
- **Register programmable power management (<10 mW power down mode)**
- **4 bit nibble and byte wide bi-directional NRZ data interfaces**
- **8-bit direct write and read mode automatically configured for RCLK = VCO/8**
- **Serial Interface port to read from and write to internal program storage registers**
- **Single power supply (5 V ± 10%)**
- **Small package footprint: 100-lead FTQFP**

AUTOMATIC GAIN CONTROL

- **Dual mode AGC, continuous time during acquisition, sampled during data reads**
- **Separate AGC level storage pins for data and servo**
- **Dual rate attack and decay charge pump for rapid AGC recovery in continuous time mode**
- **Programmable, symmetric, charge pump currents for data reads in sampled mode**
- **Charge pump currents track programmable data rate during data reads**
- **Low drift AGC hold circuitry**
- **Low-Z circuitry at AGC input provides for rapid external coupling capacitor recovery**
- **AGC Amplifier squelch during Low-Z**
- **Wide bandwidth amplitude feedback circuit to allow improved stability of AGC level vs. frequency**
- **Programmable AGC controls**
  - **Separate external input pins for AGC hold, fast recovery, and Low-Z control**

  or
  - **Internal Low-Z and fast recovery timing for rapid transient recovery and AGC acquisition. Timing set with external resistors (2). Ultra fast decay current set with external resistor.**

(continued)

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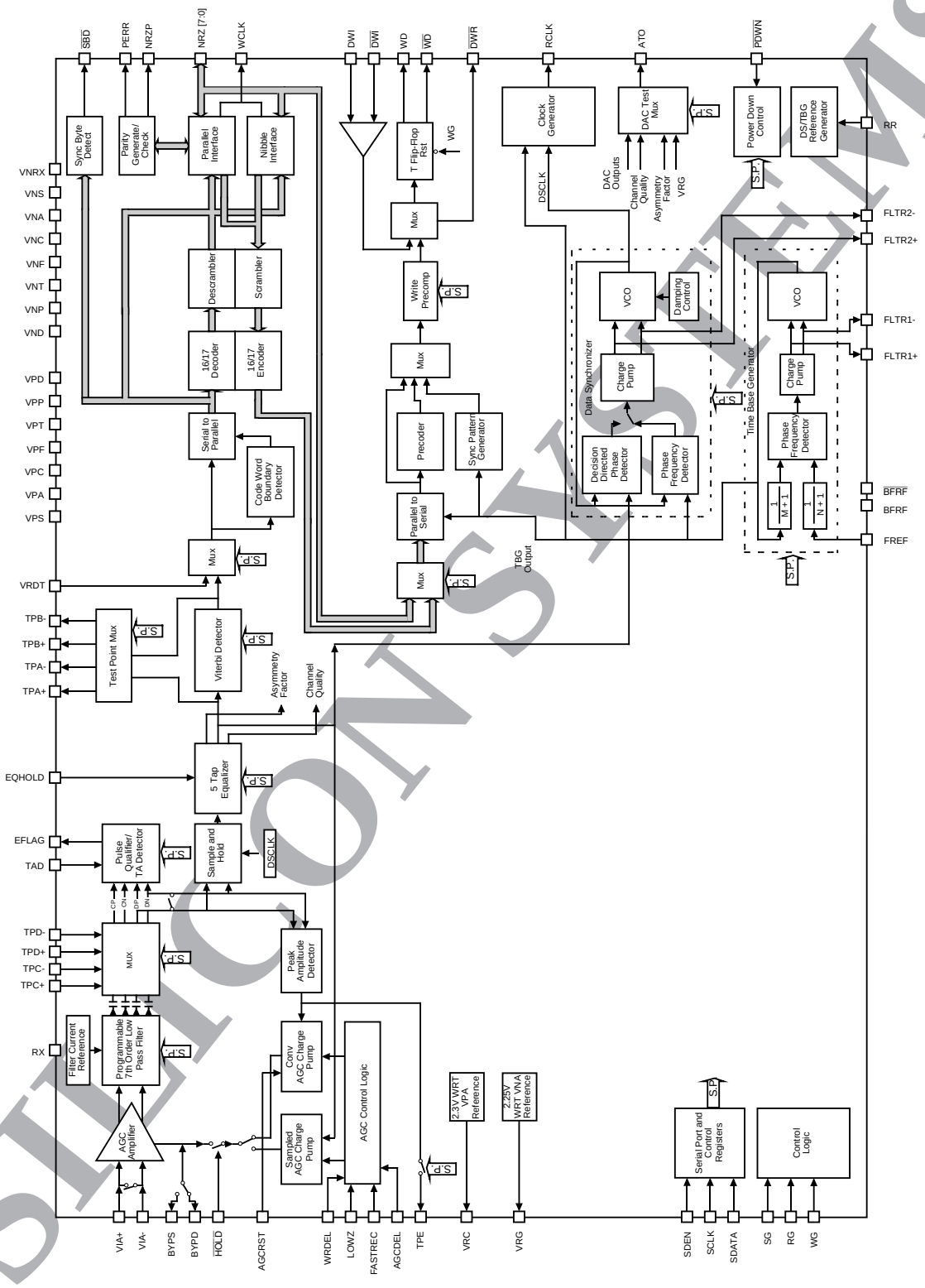
BLOCK DIAGRAM



FEATURES (continued)

FILTER/EQUALIZER

- Programmable, 7-pole, continuous time filter with asymmetrical zeros provides:
- Channel filter and pulse slimming equalization for coarse equalization to PR4
- Programmable cutoff frequency from 10 to 64 MHz
- Programmable boost/equalization of 0 to 13 dB
- Programmable “zeros” equalization provides time asymmetry compensation
- 0.6 ns group delay variation from 0.3 Fc to Fc with Fc = 64 MHz
- Low-Z switch for fast offset recovery at the filter output
- No external coupling capacitors required
- DC offset compensation provided at the filter output
- Three or five tap transversal filter for fine equalization to PR4
  - Self adapting symmetric inner taps
  - Programmable symmetric outer taps with 4 bits of resolution
- Equalization hold input
- Km 1 voltage preset
- “Zeros” channel quality output
- Asymmetry factor output

PULSE QUALIFICATION

- Sampled Viterbi qualification of signal equalized to PR4
- Register programmable window qualification peak detector during VCO sync field

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 255 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 16/17 GCR ENDEC
- Register programmable to 240 Mbit/s
- Fast acquisition, sampled data phase locked loop
- Decision directed clock recovery from data samples
- Adaptive clock recovery thresholds
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- 4-bit nibble and byte wide NRZ data interfaces
- Time base tracking, programmable write precompensation
- Differential PECL write data output
- Integrated sync word detection, single word or dual (“or” type)
- Surface defect scan mode
- Force frame capability for forcing frame and sync word detect
- Channel quailty monitor circuitry with digital feedback of the quality of the equalized samples
- Direct read mode

THERMAL ASPERITY DETECTION AND SUPPRESSION

- Internal TA detector monitors the DP/DN output from the continuous time filter for the occurrence of thermal asperities
- Hi-Y input modulation to rapidly attenuate offset due to a TA
- Hi-Y input conductance is automatically scaled to the programmed Data Rate
- AGC and PLL hold may be automatically triggered by a TA event
- Error flag output is dynamically generated to indicate TA-corrupted NRZ data
- $\overline{\text{TAD}}$ input pin allows use of an external TA event detector
- Positive and negative detection