Silicon Systems®
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SSI 32P4918B
PR4ML Read Channel with 8/9 ENDEC and Area Detect Servo

Preproduction

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DESCRIPTION

The SSI 32P4918B is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Partial Response Class 4 (PR4) read channel for zoned recording hard disk drive systems with data rates from 60 to 180 Mbit/s.

Functional blocks include a bi-directional serial port, an automatic gain control amplifier, a programmable filter, an offset canceller, a peak detecting pulse qualifier, an adaptive transversal filter, a Viterbi qualifier for maximum likelihood detection, a 8/9 GCR ENDEC, a data synchronizer, a time base generator, an integrating servo demodulator, a thermal asperity detector and suppression circuit, and a channel quality monitor.

The part requires a single +5 V power supply. The SSI 32P4918B utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which results in a high performance device with low power consumption.

FEATURES

GENERAL

- **Register programmable data rates from 60 to 180 Mbit/s**
- **Sampled data read channel with Viterbi qualification**
- **Programmable filter for PR4 equalization**
- **Five tap transversal filter with adaptive PR4 equalization**
- **8/9 GCR ENDEC**
- **Data scrambler/descrambler**
- **Presettable precoder state**
- **Programmable write precompensation**
- **Register programmable power management (<10 mW power down mode)**
- **4 bit nibble and byte wide bi-directional NRZ data interfaces**
- **8-bit direct write mode automatically configured for RCLK = VCO/8**
- **Serial interface port to read from and write to internal program storage registers**
- **Single power supply (5 V ± 10%)**
- **Small package footprint: 100-Lead FTQFP**
- **Digital channel quality monitor**
- **IO map capability**
- **Area detect servo w/dibit detector**
- **Thermal asperity suppression**
- **Multi-level write precomp**

AUTOMATIC GAIN CONTROL

- **Dual mode AGC, continuous time during acquisition, sampled during data reads**
- **Separate AGC level storage pins for data and servo**
- **Dual rate attack and decay charge pump for rapid AGC recovery in continuous time mode**
- **Programmable, symmetric, charge pump currents for data reads in sampled mode**
- **Charge pump currents track programmable data rate during data reads**
- **Low drift AGC hold circuitry**
- **Low-Z circuitry at AGC input provides for rapid external coupling capacitor recovery**
- **AGC Amplifier squelch during Low-Z**
- **Wide bandwidth amplitude feedback circuit to allow improved stability of AGC level vs. frequency**
- **Programmable AGC controls**
  - **Separate external input pins for AGC hold, fast recovery, and Low-Z control or**
  - **Internal Low-Z and fast recovery timing for rapid transient recovery and AGC acquisition. Timing set with external resistors (2). Ultra fast decay current set with external resistor.**
- **Bit to turn off fast attack current**

(continued)

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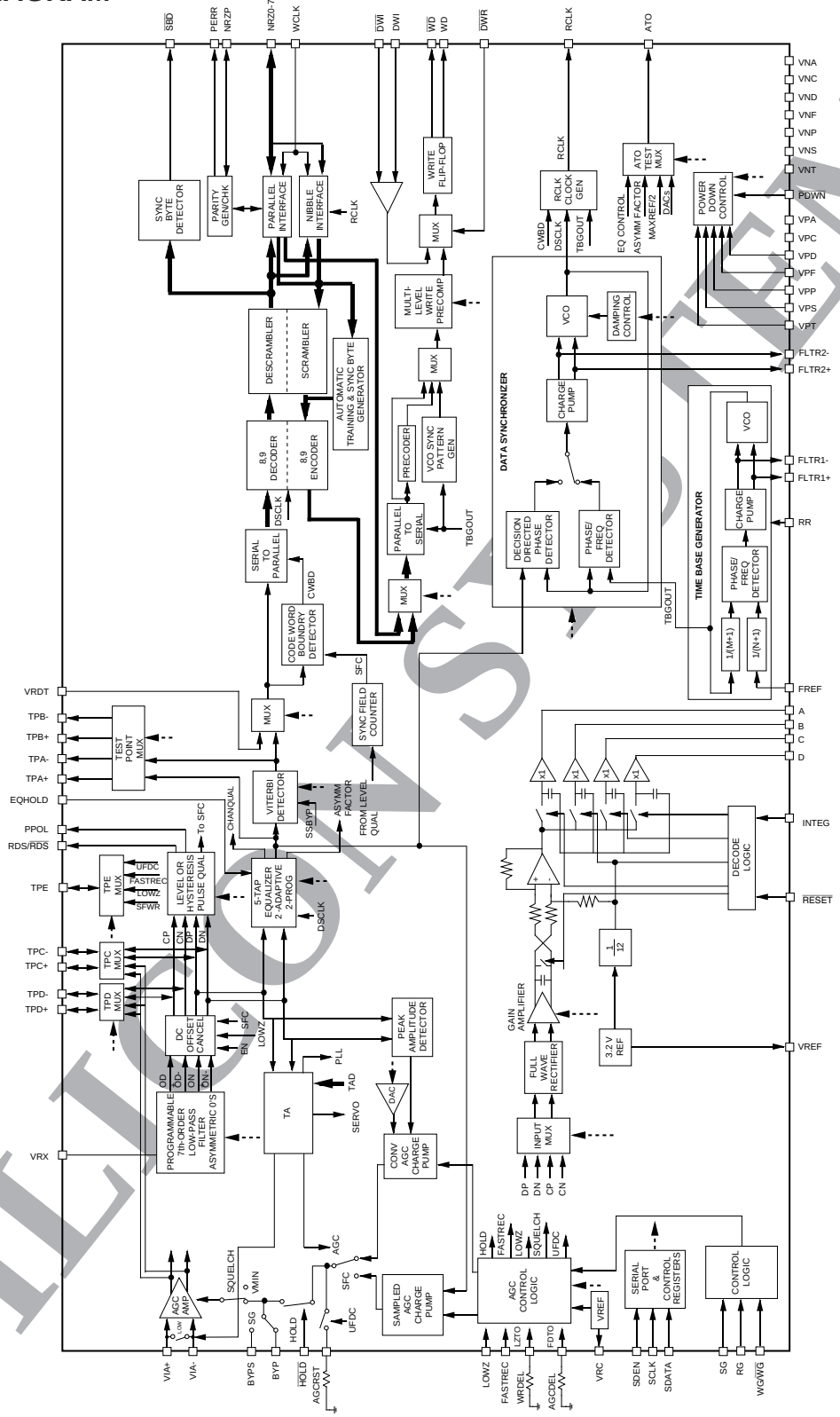
BLOCK DIAGRAM



FEATURES (continued)

FILTER/EQUALIZER

- Programmable, 7-pole, continuous time filter with asymmetrical zeros provides:
  - Channel filter and pulse slimming equalization for coarse equalization to PR4
  - Programmable cutoff frequency from 5 to 50 MHz
  - Programmable boost/equalization of 0 to 13 dB
- Programmable "zeros" equalization provides time asymmetry compensation
- ±3% group delay variation from 0.3 Fc to Fc with Fc = 50 MHz
- Low-Z switch for fast offset recovery at the filter output
- No external coupling capacitors required
- DC offset compensation provided at the filter output
- Three or five tap transversal filter for fine equalization to PR4
  - Self adapting symmetric inner taps
  - Programmable symmetric outer taps with 4 bits of resolution
- Equalization hold input
- "Zeros" channel quality output
- Asymmetry factor output

PULSE QUALIFICATION

- Sampled Viterbi qualification of signal equalized to PR4
- Register programmable hysteresis or window qualification peak detector for servo reads, positive and negative thresholds are independently programmable
- Dibit detect mode with programmable transition interval period available at RDS
- Selectable RDS pulse width for servo grey code reads
- RDS and PPOL outputs are disabled during burst capture to reduce noise generation

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 202.5 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 8/9 GCR ENDEC
- Register programmable to 180 Mbit/s
- Fast acquisition, sampled data phase locked loop
- Decision directed clock recovery from data samples
- Adaptive clock recovery thresholds
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- 4-bit nibble and byte wide NRZ data interfaces
- Time base tracking, programmable multi-level write precompensation
- Differential PECL write data output
- Semi-auto training and sync byte generation available for single sync byte operation
- Surface defect scan mode
- KM1 preset function allows the adaptive equalizer training time to be reduced
- Force frame function allows data to be recovered even if the framing bytes are damaged
- Force sync byte function allows data to be recovered if sync bytes are damaged
- Programmable separation of sync bytes
- Channel quality monitor circuitry allows for digital feedback of the quality of the equalized samples

SERVO

- Separate, automatically selected, registers for servo Fc, boost, and threshold
- Wide bandwidth, high precision full-wave rectifier is optimized for low-level linearity
- Integrator circuit has an auto-zero function to actively remove any DC offsets
- 3 bits of fine gain control to accommodate a wide range of pulse densities into the area detector

SERVO (continued)

- Programmable AGC gain in servo mode (1 bit)
- 4-burst servo capture with A, B, C, D outputs
- Internal hold capacitors
- Servo calibration output available

THERMAL ASPERITY DETECTION AND SUPPRESSION

- Internal TA detector monitors the DP/DN output from the continuous time filter for the occurrence of thermal asperities, both positive and negative events can be detected
- Thermal asperity threshold is independently selectable for Servo and non-Servo modes of operation
- Hi-Y input modulation to rapidly attenuate offset due to a TA
- AGC and PLL hold may be automatically triggered by a TA event
- $\overline{\text{TAD}}$ input pin allows use of an external TA event detector