Silicon Systems®
A Texas Instruments Company

SSI 32P4915B
PRML Read Channel with PR4, 8/9 ENDEC, 4-Burst Servo

Prototype

March 1997

DESCRIPTION

The SSI 32P4915B is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Partial Response Class 4 (PR4) read channel for zoned recording hard disk drive systems with data rates from 47 to 140 Mbit/s. Functional blocks include AGC, programmable filter, adaptive transversal filter, Viterbi qualifier, 8,9 GCR ENDEC, data synchronizer, time base generator, and 4-burst servo. Programmable functions such as data rate, filter cutoff, filter boost, etc., are controlled by writing to the Serial Port Registers so no external component changes are required to change zones. The part requires a single +5 V power supply. The SSI 32P4915B utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

GENERAL

- **Register programmable data rates from 47 to 140 Mbit/s**
- **Sampled data read channel with Viterbi qualification**
- **Programmable filter for PR4 equalization**
- **5-tap transversal filter with adaptive PR4 equalization**
- **8,9 GCR ENDEC**
- **Data scrambler/descrambler**
- **Presettable precoder state**
- **Programmable write precompensation**
- **Low operating power (1.1 W typical at 5 V)**
- **Register programmable power management (< 5 mW power-down mode)**
- **4-bit nibble and byte wide bi-directional NRZ data interfaces**
- **I/O mapping and In circuit test**
- **8-bit direct write mode automatically configured for RCLK = VCO/8**
- **Thermal asperity detection and suppression**
- **Bi-directional serial interface port for access to internal program storage registers (read and write capability)**
- **Single power supply (5 V ± 10%)**
- **Small footprint 100-Lead FTQFP**

AUTOMATIC GAIN CONTROL

- **Dual mode AGC, analog during acquisition, sampled during data reads**
- **Separate AGC level storage pins for data and servo**
- **Dual rate attack and decay charge pump for rapid AGC recovery (analog)**
- **Programmable, symmetric, charge pump currents for data reads (sampled)**
- **Charge pump currents track programmable data rate during data reads (sampled)**
- **Low drift AGC hold circuitry**
- **Low-Z circuitry at AGC input provides for rapid external coupling capacitor recovery**
- **AGC amplifier squelch during Low-Z**
- **Wide bandwidth, precision full-wave rectifier**
- **Programmable AGC controls**
  - **Separate external input pins for AGC hold, fast recovery, and Low-Z control**

  or

  - **Internal Low-Z and fast decay timing for rapid transient recovery and AGC acquisition. Timing set with external resistors (2). Ultra fast decay current set with external resistor. AGC input impedance vs LOWZ = 5:1.**
- **2-bit DAC to control AGC voltage in servo mode between 1.1 V and 1.4 V**

SSI 32P4915B
PRML Read Channel with
PR4, 8/9 ENDEC, 4-Burst Servo

BLOCK DIAGRAM