Silicon Systems®
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SSI 32P4904
PRML Read Channel with PR4, 8/9 ENDEC, FWR Servo

May 1996

DESCRIPTION

The SSI 32P4904 is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Partial Response Class 4 (PR4) read channel for zoned recording hard disk drive systems with data rates from 24 to 80 Mbit/s.

Functional blocks include AGC, programmable filter, adaptive transversal filter, Viterbi qualifier, 8,9 GCR ENDEC, data synchronizer, time base generator, and FWR servo.

Programmable functions such as data rate, filter cutoff, filter boost, etc. are controlled by writing to the serial port registers so no external component changes are required to change zones. The part requires a single +5V power supply.

The SSI 32P4904 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

GENERAL

- **Register programmable data rates from 24 to 80 Mbit/s**
- **Sampled data read channel with Viterbi qualification**
- **Programmable filter for PR4 equalization**
- **3-tap transversal filter for adaptive PR4 equalization**
- **8/9 GCR ENDEC**
- **Data scrambler/descrambler**
- **Programmable write precompensation**
- **Low operating power (0.75W typical at 5V)**
- **Register programmable power management**
- **Presettable precoder state**
- **Register programmable WG polarity**
- **Dual bit and byte wide bi-directional NRZ data interfaces**
- **Serial interface port for access to internal program storage registers**
- **Single power supply (5V ±10%)**
- **Small footprint 100-Lead TQFP and 100-Lead QFP packages**

AUTOMATIC GAIN CONTROL

- **Dual mode AGC, analog during acquisition, sampled during read data**
- **Separate AGC level storage pins for data and servo**
- **Dual rate attack and decay charge pump for rapid AGC recovery**
- **Programmable, symmetric, charge pump currents during read data**
- **Charge pump currents track programmable data rate**
- **Low drift AGC hold circuitry**
- **Low-Z input switch**
- **AGC hold, fast recovery, and AGC input impedance control signals**
- **Wide bandwidth, precision full-wave rectifier**

FILTER/EQUALIZER

- **Programmable, 7-pole, continuous time filter provides:**
  - **Channel filter and pulse slimming equalization for equalization to PR4**
  - **Programmable cutoff frequency, 3 to 24 MHz**
  - **Programmable boost/equalization, 0 to 12.75 dB**
  - **±0.6 ns group delay variation from 0.2 f_c to f_c, with f_c = 24 MHz**
  - **Minimizes size and power**
  - **Low-Z input switch**
- **3-tap self adapting transversal filter for fine equalization to PR4**
- **No external components required**

(continued)

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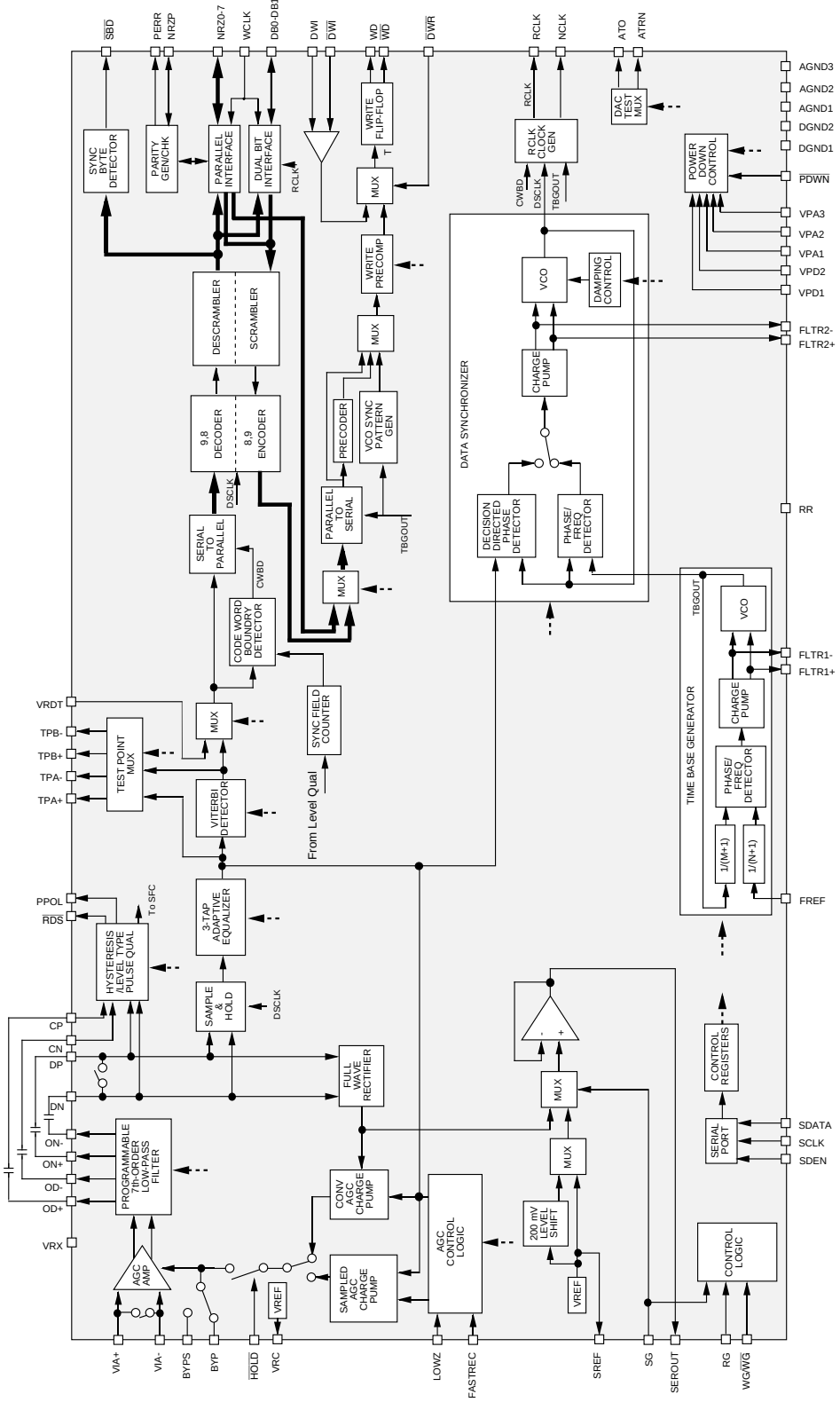
BLOCK DIAGRAM



FEATURES (continued)

PULSE QUALIFICATION

- Sampled Viterbi qualification of signal equalized to PR4
- Register selection between dual level pulse qualifier or hysteresis qualifier for servo reads

TIME BASE GENERATOR

- Less than 1% frequency resolution
- Up to 90 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 8,9 GCR ENDEC
- Register programmable to 80 Mbit/s operation
- Fast acquisition, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Adaptive (+) and (-) clock recovery thresholds for use with asymmetrical amplitude signals (e.g. from MR heads)
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- Dual bit and byte wide NRZ data interfaces
- Time base tracking, programmable write precompensation
- Differential PECL write data output
- Integrated sync byte detection

SERVO

- Wide bandwidth, precision full-wave rectifier
- Buffered FWR analog servo output with selectable reference voltage
- Separate, automatically selected, registers for servo fc, boost, and threshold
- Compatible with SSI 32H6521 Embedded Servo Controller

FUNCTIONAL DESCRIPTION

The SSI 32P4904 implements a complete high performance PR4 read channel, including an AGC, programmable filter/equalizer, adaptive transversal filter, Viterbi pulse qualifier, time base generator, data separator with 8,9 ENDEC and scrambler/descrambler, and FWR servo, that supports data rates up to 80 Mbit/s.

A serial port is provided to write control data to the 16 internal program storage registers.

AGC CIRCUIT DESCRIPTION

The automatic gain control (AGC) circuit is used to maintain a constant signal amplitude at the input of the pulse detector while the input to the amplifier varies. The circuit consists of a loop that includes the AGC amplifier and charge pump, the programmable continuous time filter, and the precision wide band full wave rectifier. Depending on whether the read is of servo or data type, the specific blocks utilized in the loop are slightly different. Both loop paths are fully differential to minimize susceptibility to noise.

During servo reads the loop consists of the AGC amplifier with a continuous dual rate charge pump, the programmable continuous time filter, and the precision wide band full wave rectifier. The gain of the AGC amplifier is controlled by the voltage stored on the BYPS hold capacitor (C_{BYPS}). The dual rate charge pump drives C_{BYPS} with currents that drive the differential voltage at DP/DN to 1.4 Vp-pd. Attack currents lower the V_{BYPS} which reduces the amplifier gain. The dual rate attack charge pump is included for fast transient recovery. The normal AGC attack current in servo mode is 150 µA. When the signal exceeds 125% of the nominal signal level, the attack current is increased by a factor of 8. The nominal decay current is 8.3 µA, and increases by a factor of 8 when the FASTREC input is high. In this mode, transients that produce low gain will recover more rapidly with the fast decay current, while transients that produce high gain will put the circuit in the fast attack recovery mode.