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DESCRIPTION

The SSI 32P4810 is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire E²PR4 1,7 code read channel for zoned recording hard disk drive systems with data rates from 50 to 160 Mbit/s.

Functional blocks include AGC, programmable filter, maximum likelihood (ML) detector, 1,7 ENDEC, data synchronizer, time base generator, servo data detector, and 4-burst servo.

Programmable functions such as data rate, filter cutoff, filter boost, etc. are controlled by writing to the serial port registers so no external component changes are required to change zones.

1,7 RLL code operation is used to reduce the magnetic media flux transitions per inch and the write current rise time requirements.

FEATURES

GENERAL

- Register programmable data rates from 50 to 160 Mbit/s
- Sampled data read channel with maximum likelihood (ML) detector
- Programmable filter with asymmetrical zeros to compensate pulse asymmetry
- 1,7 RLL ENDEC
- Data scrambler/descrambler
- Low operating power (0.95 W typical at 5 V)
- Register programmable power management (<10 mW power down mode)
- 4/8 bit NRZ data interfaces
- Serial interface port for access to internal program storage registers
- Single power supply (5 V \pm 10%)
- Small footprint 100-lead FTQFP package

AUTOMATIC GAIN CONTROL

- Dual mode AGC, continuous time during acquisition, sampled during data reads
- Separate AGC level storage pins for data and servo
- Dual rate attack and decay charge pump for rapid AGC recovery
- Programmable, symmetric, charge pump currents for data reads
- Charge pump currents track programmable data rate during data reads
- Low drift AGC hold circuitry
- Automatic AGC fast recovery and input low-z modes with programmable time durations
- Wide bandwidth, precision full-wave rectifier
- Optional internal timing disable and AGC direct control pins: LOWZ, FASTREC, $\overline{\text{HOLD}}$
- 3-bit DAC to control AGC voltage in servo mode between 0.8 and 1.5 V

(continued)

SSI 32P4810

E²PRML Read Channel with 1,7 ENDEC, 4-Burst Servo (A,B,C,D)

FEATURES (continued)

FILTER/EQUALIZER

- Programmable, 7-pole, continuous time filter with asymmetrical zeros provides:
 - Channel filter and pulse slimming equalization for equalization to E²PR4
 - Programmable cutoff frequency from 5 to 43 MHz
 - Programmable boost/equalization of 0 to 16 dB
 - Programmable asymmetrical zeros equalization to correct pulse shape asymmetry
- Internal AC-coupling with fast offset recovery at Filter outputs

PULSE QUALIFICATION

- Sampled maximum likelihood data detector with fixed E²PR4 target detection.
- With white gaussian noise, within 0.5 dB of ideal viterbi detector at user density of 2
- Register programmable qualification thresholds for servo reads
- Selectable hysteresis or window qualification modes for servo reads

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 240 MHz frequency output
- Independent M and N divide-by registers

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 1,7 RLL ENDEC
- Register programmable to 160 Mbit/s operation
- Fast acquisition, zero phase restart, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects

- 4/8-bit NRZ data interface
- Data rate tracking, programmable write precompensation for non-linear transition shift
- Differential PECL write data output with power reduction
- Integrated dual byte sync detection
- Programmable offset to compensate for MR head asymmetry.

SERVO

- 4-burst servo capture with A, B, C, D outputs
- Internal hold capacitors
- Soft landing charge pump architecture with programmable charge pump current
- Separate, automatically selected, registers for servo Fc, boost, group delay equalization and threshold
- Wide bandwidth, precision full-wave rectifier with programmable offset to compensate for MR head asymmetry.
- $\overline{\text{RDS}}$ and PPOL outputs for servo timing support

THERMAL ASPERITY DETECTION/ CORRECTION

- Analog front end thermal asperity detection and correction circuits
- Digital outputs for thermal asperity detection and NRZ data error flag

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BLOCK DIAGRAM

