Silicon Systems®
A Texas Instruments Company

SSI 32P4752
Read Channel with 1,7 ENDEC, 4-burst Servo

January 1996

DESCRIPTION

The SSI 32P4752 devices are high performance BiCMOS single chip read channel ICs that contain all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. Functional blocks include the pulse detector, programmable filter, 4-burst servo capture, time base generator, and data separator with 1,7 RLL ENDEC. Data rates from 18 to 64 Mbit/s can be programmed using an internal DAC whose reference current is set by a single external resistor. For reduced clocking speeds, the 32P4752 employs a dual-bit parallel interface to the controller.

Programmable functions of the SSI 32P4752 devices are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 32P4752 utilize an advanced BiCMOS process technology along/ with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

GENERAL:

- **DAC controlled programmable data rates from 18 to 64 Mbit/s**
- **Complete zoned recording application support**
- **Low power operation < 600 mW typical at 5V**
- **Bi-directional serial port for register access**
- **Register programmable power management (sleep mode <0.5 mA)**
- **Power supply range (4.5 to 5.5V)**
- **Small footprint 64-lead TQFP package**

PULSE DETECTOR:

- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low Drift AGC hold circuitry**
- **Temperature compensated, exponential control AGC**
- **Wide bandwidth, high precision full-wave rectifier**

(continued)

BLOCK DIAGRAM