Silicon Systems®
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SSI 32P4742/4742A
Read Channel with 1,7 ENDEC, 4-burst Servo

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DESCRIPTION

The SSI 32P4742/4742A devices are high performance BiCMOS single chip read channel ICs that contain all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. Functional blocks include the pulse detector, programmable filter, 4-burst servo capture, time base generator, and data separator with 1,7 RLL ENDEC. Data rates from 16 to 48 Mbit/s can be programmed using an internal DAC whose reference current is set by a single external resistor. For reduced clocking speeds, the 32P4742/4742A employs a dual-bit parallel interface to the controller.

Programmable functions of the SSI 32P4742/4742A devices are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 32P4742/4742A utilize an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

GENERAL:

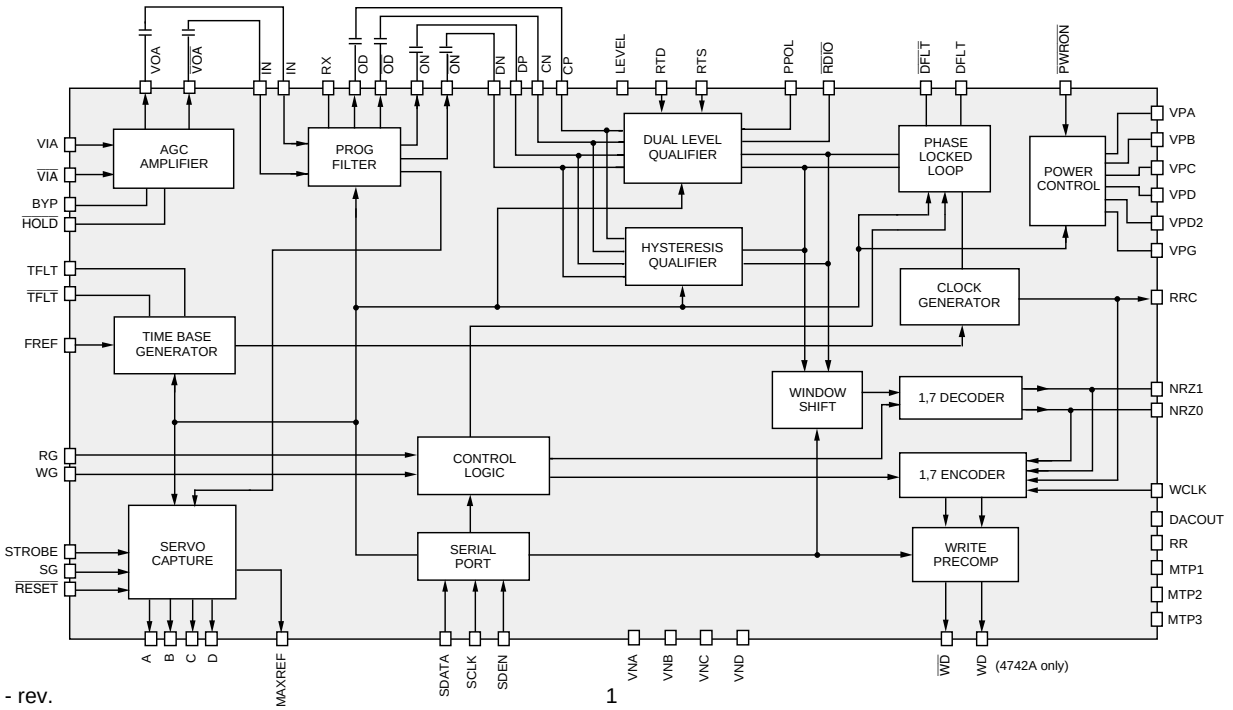
- **DAC controlled programmable data rates from 16 to 48 Mbit/s**
- **Complete zoned recording application support**
- **Low power operation < 500 mW typical at 5V**
- **Bi-directional serial port for register access**
- **Register programmable power management (sleep mode <0.5 mA)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 64-lead TQFP package**

PULSE DETECTOR:

- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low Drift AGC hold circuitry**
- **Temperature compensated, exponential control AGC**
- **Wide bandwidth, high precision full-wave rectifier**
- **Dual mode pulse qualification circuitry (user selectable)**
- **CMOS $\overline{\text{RDIO}}$ signal output for servo timing support**
- **Internal LOW-Z and fast decay timing**
- **0.8 ns max. pulse pairing at 48 Mbit/s using a 18 MHz sine wave input**

(continued)

BLOCK DIAGRAM



FEATURES (continued)

SERVO CAPTURE:

- 4-burst servo capture with A, B, C, D outputs
- Internal hold capacitors
- Separate registers for fc and V_{TH} during servo mode
- 4-bit DAC for servo AGC level control (0.9 to 1.2 Vp-p)

PROGRAMMABLE FILTER:

- Programmable cutoff frequency of 6 to 18 MHz
- Programmable boost/equalization of 0 to 13 dB
- Matched normal and differentiated outputs
- ± 15% fc accuracy
- ± 2% maximum group delay variation to fc
- Less than 1.5% total harmonic distortion
- Low-Z input switch
- No external filter components required

TIME BASE GENERATOR:

- Better than 1% frequency resolution
- Up to 75 MHz frequency output
- Independent M and N divide-by registers
- VCO center frequency matched to data synchronizer VCO

DATA SEPARATOR:

- Fast acquisition phase lock loop with zero phase restart technique
- Dual-bit NRZ interface
- Integrated 1,7 RLL Encoder/Decoder
- Programmable decode window symmetry control via serial port
  - Window shift control (4-bit)
  - Includes delayed read data and VCO clock monitor points
- Programmable early/late write precomp (3-Bits each)
- TTL write data output - 32P4742
- Differential PECL write data output - 32P4742A
- Hard sector operation
- VCO and Synchronized Read Data test points

FUNCTIONAL DESCRIPTION

The SSI 32P4742/4742A implement a high performance complete read channel, including pulse detector, 4-burst servo capture, programmable active filter, time base generator, and data separator with 1,7 RLL ENDEC, at data rates up to 48 Mbit/s.

PULSE DETECTOR CIRCUIT DESCRIPTION

The pulse detector, in conjunction with the programmable filter, provides all the data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide band variable gain amplifier; a wide bandwidth, high precision fullwave rectifier; and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

AGC CIRCUIT

The gain of the AGC amplifier is controlled by the voltage (V_{BYP}) stored on the BYP hold capacitor (C_{BYP}), Figure 1. A dual rate charge pump drives C_{BYP} with currents that depend on the instantaneous differential voltage at the DP/DN pins. Attack currents lower V_{BYP} which reduces the amplifier gain, while decay currents increase V_{BYP} which increases the amplifier gain. When the signal at DP/DN is greater than 100% of the programmed AGC level, the nominal attack current of 0.21 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, a fast attack current of nine (9) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 5 µA increases the amplifier gain when the signal at DP/DN is less than the programmed AGC level. The large ratio (0.21 mA:5 µA) of the nominal attack and nominal decay currents enables the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A fast decay current mode is provided by setting bit 7 of the CAR to “0,” to allow the AGC gain to be rapidly increased to reduce the recovery time between mode switches.