Silicon Systems®
A Texas Instruments Company

SSI 32P4730
Read Channel with 1,7 ENDEC, 4-burst Servo

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DESCRIPTION

The SSI 32P4730 device is a high performance BiCMOS single chip read channel IC that contains all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. Functional blocks include the pulse detector, programmable filter, 4-burst servo capture, time base generator, and data separator with 1,7 RLL ENDEC. Data rates can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 32P4730 device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 32P4730 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

GENERAL

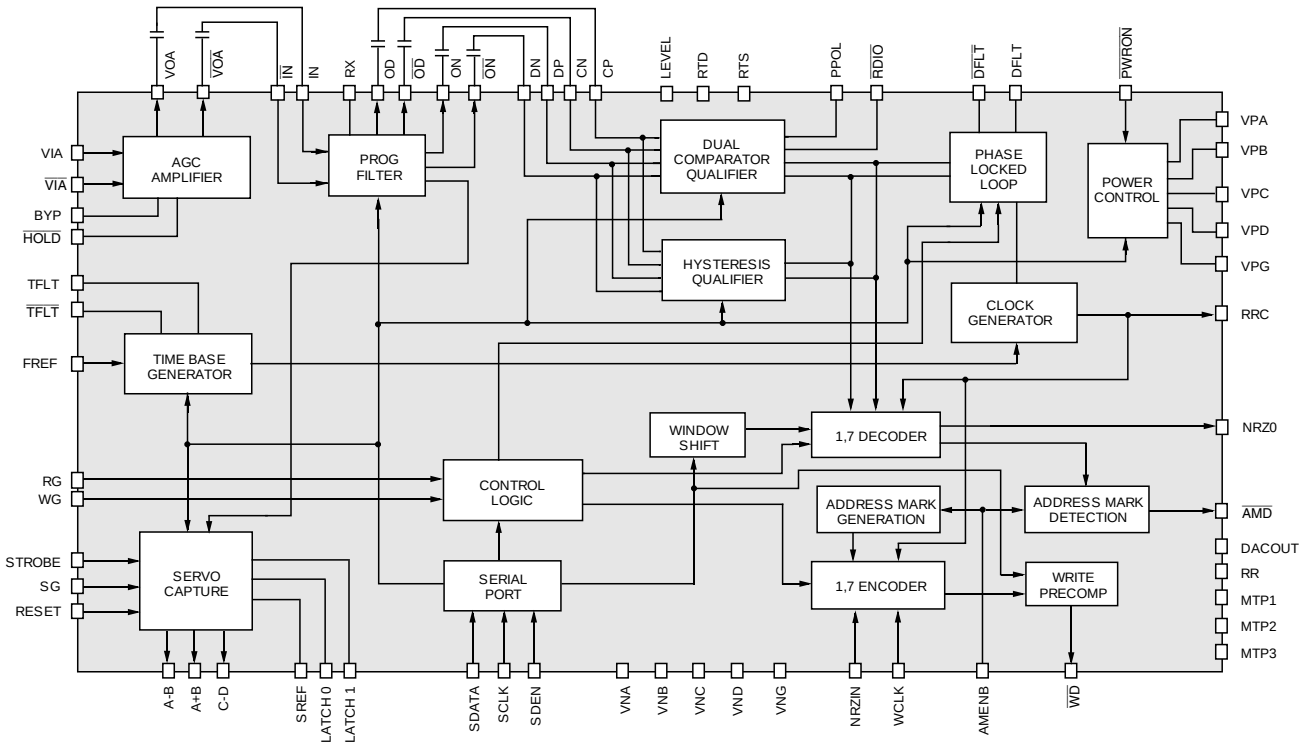
- **DAC controlled programmable data rates**
  - 8 to 27.3 Mbit/s
- **Complete zoned recording application support**
- **Low power operation -**
  400 mW typical @ 5V and 27.3 Mbit/s
- **Bi-directional serial port for register access**
- **Register programmable power management (sleep mode < 0.5 mA)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 64-lead TQFP package**

PULSE DETECTOR

- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low Drift AGC hold circuitry**
- **Temperature compensated, exponential control AGC**

(continued)

BLOCK DIAGRAM



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FEATURES (continued)

- Wide bandwidth, high precision full-wave rectifier
- Dual mode pulse qualification circuitry (user selectable)
- Programmable voltage qualification threshold level
- CMOS $\overline{\text{RDIO}}$ signal output for servo timing support
- Internal LOW-Z and fast decay timing
- 0.8 ns max. pulse pairing

SERVO CAPTURE

- 4-burst servo capture with A-B, C-D, A+B outputs
- Internal hold capacitors
- Programmable charge current (4-bit DAC)
- Separate registers for FC and VTH during servo mode
- 4-bit DAC for AGC level control (0.75 to 1 Vp-p)

PROGRAMMABLE FILTER

- Programmable cutoff frequency 3 to 9 MHz
- Programmable boost/equalization of 0 to 13 dB
- Matched normal and differentiated outputs
- ± 15% *f*c accuracy
- ± 2% maximum group delay variation
- Less than 1% total harmonic distortion
- Low-Z input switch
- No external filter components required

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 81.8 MHz frequency output
- Independent M and N divide-by registers
- VCO center frequency matched to data synchronizer VCO

DATA SEPARATOR

- Fast acquisition phase lock loop with zero phase restart technique
- Integrated 1,7 RLL Encoder/Decoder
- Fully integrated data separator
  - No external delay lines or active devices required
  - No external active PLL components required
- Programmable decode window symmetry control via serial port
  - Window shift control ± 34.5% (4-bit)
  - Includes delayed read data and VCO clock monitor points
- Programmable early/late write precomp (3-Bits each)
- Hard and soft sector operation
- VCO and Synchronized Read Data test points

FUNCTIONAL DESCRIPTION

The SSI 32P4730 implements a high performance complete read channel, including pulse detector, 4-burst servo capture, programmable active filter, time base generator, and data separator with 1,7 RLL ENDEC, at data rates up to 27.3 Mbit/s.

PULSE DETECTOR CIRCUIT DESCRIPTION

The pulse detector, in conjunction with the programmable filter, provides all the data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide band variable gain amplifier; a wide bandwidth, high precision fullwave rectifier; and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

AGC CIRCUIT

The gain of the AGC amplifier is controlled by the voltage (V_{BYP}) stored on the BYP hold capacitor (C_{BYP}), Figure 1. A dual rate charge pump drives C_{BYP} with currents that depend on the instantaneous differential voltage at the DP/DN pins. Attack currents lower V_{BYP} which reduces the amplifier gain, while decay currents increase V_{BYP} which increases the amplifier gain. When the signal at DP/DN is greater than 100% of the programmed AGC level, the nominal attack current of 0.21 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, a fast attack current of nine (9) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 5 μA acts to increase the amplifier gain when the signal at DP/DN is less than the programmed AGC level. The large ratio (0.21 mA:5 μA) of the nominal attack and nominal decay currents enables the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A fast decay current mode is provided to allow the AGC gain to be rapidly increased to reduce the recovery time between mode switches.