

# SSI 32P4130

## EPRML Read Channel w/16/17's ENDEC, 4-Burst Area Detect Servo (A, B, C, D)

**Prototype**

January 1998

### DESCRIPTION

The SSI 32P4130 is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Extended Partial Response Class 4(EPR4) 16/17's code read channel for zoned recording hard disk drive systems with data rates from 33.7 to 135 Mbit/s.

Functional blocks include AGC, programmable filter, adaptive transversal filter, Viterbi qualifier, 16/17's GCR ENDEC, data synchronizer, time base generator, servo data detector, and 4-burst servo.

Programmable functions such as data rate, filter cutoff, filter boost, etc., are controlled by writing to the serial port registers so no external component changes are required to change zones.

The SSI 32P4130 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

### FEATURES

- Register programmable data rates from 30 to 135 Mbit/s
- Sampled data read channel with Viterbi qualification
- Programmable filter for PR4 equalization
- Five tap transversal filter with adaptive or programmable tap weight
- 16/17's [0,6,8] GCR ENDEC
- Data scrambler/descrambler
- Programmable three level write precomp
- Low operating power (0.9 W typical at 5 V)
- Register programmable power management (<5 mW power down mode)
- Byte wide bi-directional NRZ data interface
- Serial interface port for access to internal program storage registers
- Single power supply (5 V  $\pm$  10%)
- Small footprint 64-Lead TQFP package

### AUTOMATIC GAIN CONTROL

- Dual mode AGC, continuous time during acquisition, sampled during data reads
- Separate AGC level storage pins for data and servo
- Dual rate attack and decay charge pump for rapid AGC recovery
- Programmable, symmetric, charge pump currents for data reads
- Charge pump currents track programmable data rate during data reads
- Low drift AGC hold circuitry
- Automatic AGC fast recovery and input low-z modes with programmable time durations
- Wide bandwidth, precision full-wave rectifier
- Optional internal timing disable and AGC direct control pins: LOW-Z, FASTREC, HOLD
- 2-bit DAC to control AGC voltage in servo mode between 1.1 and 1.4 V

### FILTER/EQUALIZER

- Programmable, 7-pole, continuous time filter with asymmetrical zeros provides:
  - Channel filter and pulse slimming equalization for equalization to PR4
  - Programmable cutoff frequency from 5 to 36 MHz
  - Programmable boost/equalization of 0 to 15 dB
  - Programmable asymmetrical zeros equalization to correct pulse shape asymmetry
- Five tap transversal filter provides:
  - Fine equalization to PR4
  - Self adapting symmetric tap coefficients
  - Presettable symmetric tap coefficients
- Additional (1+D) equalization to meet EPR4 target
- Low Z switch for fast offset recovery at the filter output

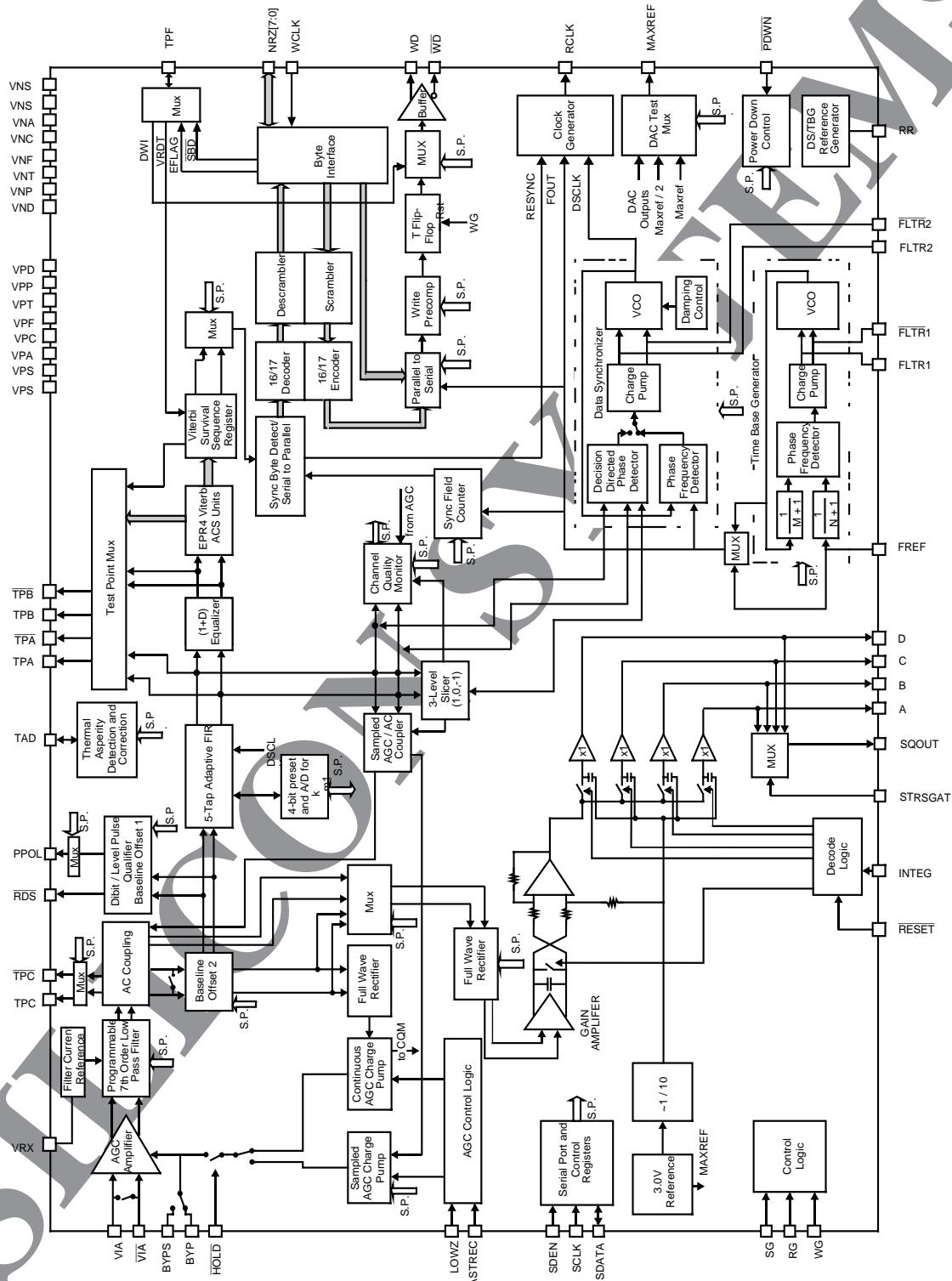
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### 4-Burst Area Detect Servo (A, B, C, D)

#### BLOCK DIAGRAM



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### **FILTER/EQUALIZER** (continued)

- Equalizer hold input
- Amplitude asymmetry factor output
- Low Z switch for fast offset recovery at the filter output, on chip direct coupling at input and output to eliminate external AC-coupling

### **PULSE QUALIFICATION**

- Sampled Viterbi qualification of signal equalized to EPR4
- Register programmable qualification thresholds for servo reads
- Selectable hysteresis or window qualification modes for servo reads
- Selectable dibit or pulse detect qualification modes for servo reads
- Programmable baseline offset for amplitude asymmetry compensation

### **ERROR MEASUREMENT**

- Digital channel quality monitor

### **TIME BASE GENERATOR**

- Better than 1% frequency resolution
- Up to 135 • 17/16 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

### **DATA SEPARATOR**

- Fully integrated data separator includes data synchronizer and 16/17's GCR ENDEC
- Register programmable to 135 Mbit/s operation
- Fast acquisition, sampled data phase lock loop
- Decision directed clock recovery from data samples

- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- 8-bit NRZ data interface
- Time base tracking, programmable write precompensation for non-linear transition shift
- Differential PECL write data output with power reduction
- Integrated sync byte detection, single byte or dual
- Programmable offset to compensate for MR head asymmetry
- Surface defect scan mode

### **SERVO**

- 4-burst soft landing servo with A, B, C, D outputs
- Internal hold capacitors
- Separate, automatically selected, registers for servo Fc, boost, and threshold
- Wide bandwidth, precision full-wave rectifier with programmable offset to compensate for MR head asymmetry
- Servo calibration outputs
- Programmable baseline offset
- RDS and PPOL outputs for servo data recovery

### **THERMAL ASPERITY DETECTION/CORRECTION**

- Analog front end thermal asperity detection and correction circuits
- Digital outputs for thermal asperity detection and error flag
- AGC and PLL hold over thermal asperity with programmable duration
- Programmable high admittance over thermal asperity

**Prototype:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems reserves the right to make changes in specifications at any time without notice. Accordingly, the reader is cautioned to verify that the data sheet is current before placing orders.

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