Silicon Systems®
A Texas Instruments Company

SSI 32P4101A
EPRML Read Channel w/16/17's ENDEC, 4-Burst Servo (A, B, C, D)

Prototype

September 1997

DESCRIPTION

The SSI 32P4101A is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Extended Partial Response Class 4(EPR4) 16/17's code read channel for zoned recording hard disk drive systems with data rates from 50 to 200 Mbit/s.

Functional blocks include AGC, programmable filter, adaptive transversal filter, Viterbi qualifier, 16/17's GCR ENDEC, data synchronizer, time base generator, servo data detector, and 4-burst servo.

Programmable functions such as data rate, filter cutoff, filter boost, etc., are controlled by writing to the serial port registers so no external component changes are required to change zones.

The SSI 32P4101A utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

- **Register programmable data rates from 50 to 200 Mbit/s**
- **Sampled data read channel with Viterbi qualification**
- **Programmable filter for PR4 equalization**
- **Five tap transversal filter with adaptive PR4 equalization**
- **16/17's [0,6,8] GCR ENDEC**
- **Data scrambler/descrambler**
- **Presettable precoder state**
- **Low operating power (TBDmW typical at 5 V)**
- **Register programmable power management (<5 mW power down mode)**
- **8 bit NRZ data interface**
- **8-bit direct write and read modes automatically configured for RCLK = VCO/8**
- **Serial interface port for access to internal program storage registers**
- **Single power supply (5 V ± 10%)**
- **Small footprint 100-Lead TQFP package**

AUTOMATIC GAIN CONTROL

- **Dual mode AGC, continuous time during acquisition, sampled during data reads**
- **Separate AGC level storage pins for data and servo**
- **Dual rate attack and decay charge pump for rapid AGC recovery**
- **Programmable, symmetric, charge pump currents for data reads**
- **Charge pump currents track programmable data rate during data reads**
- **Low drift AGC hold circuitry**
- **Automatic AGC fast recovery and input low-z modes with programmable time durations**
- **Wide bandwidth, precision full-wave rectifier**
- **Optional internal timing disable and AGC direct control pins: LOW-Z, FASTREC, $\overline{\text{HOLD}}$**
- **2-bit DAC to control AGC voltage in servo mode between 1.1 and 1.4 V**

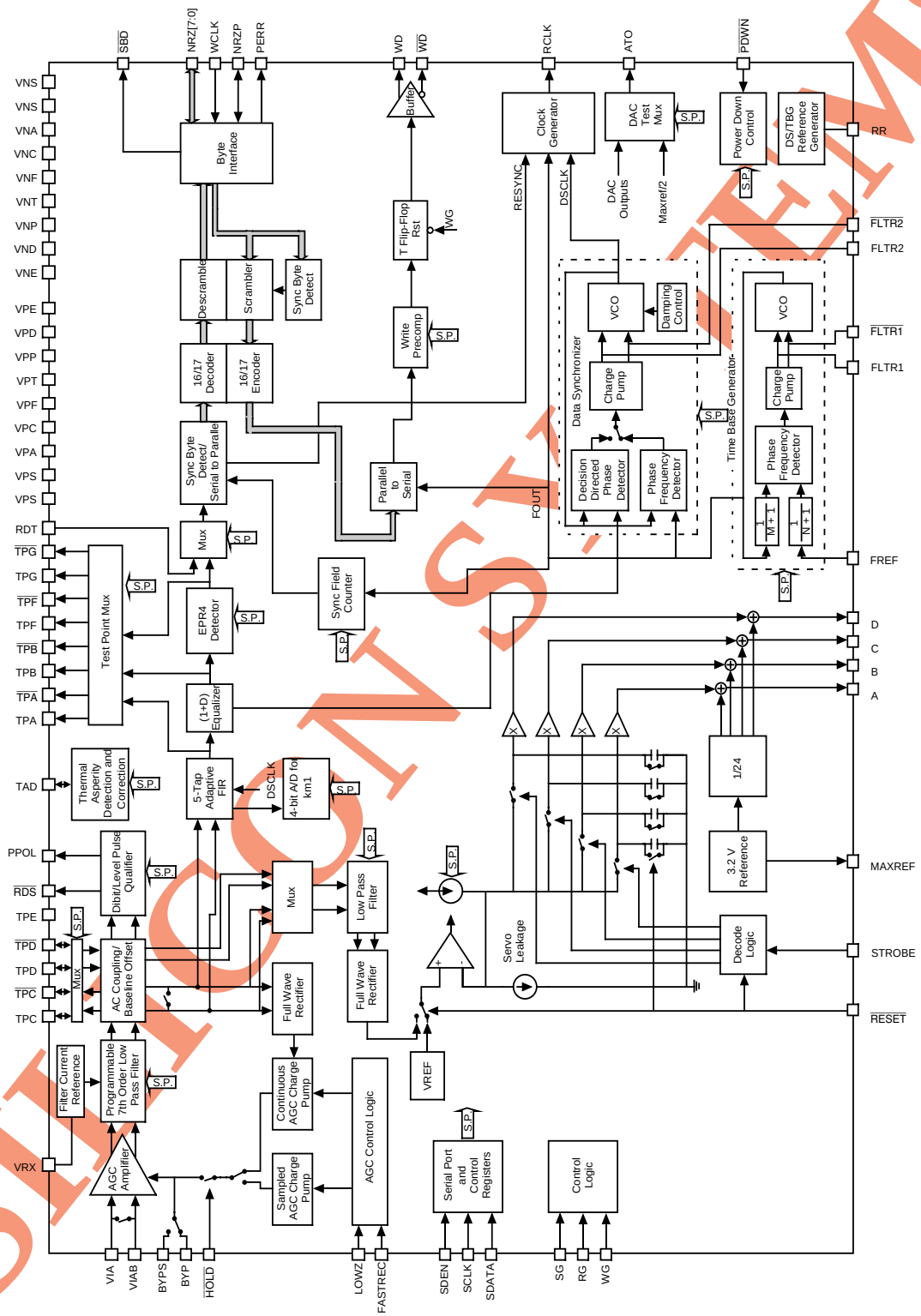
FILTER/EQUALIZER

- **Programmable, 7-pole, continuous time filter with asymmetrical zeros provides:**
  - **Channel filter and pulse slimming equalization for equalization to PR4**
  - **Programmable cutoff frequency from 5 to 56 MHz**
  - **Programmable boost/equalization of 0 to 15 dB**
  - **Programmable asymmetrical zeros equalization to correct pulse shape asymmetry**
- **Five tap transversal filter provides:**
  - **Fine equalization to PR4**
  - **Self adapting symmetric tap coefficients**
  - **Presettable symmetric tap coefficients**
- **Additional (1+D) equalization to meet EPR4 target**
- **Low Z switch for fast offset recovery at the filter output**

(continued)

SSI 32P4101A
EPRML Read Channel w/16/17's ENDEC, 4-Burst Servo (A, B, C, D)

BLOCK DIAGRAM



FILTER/EQUALIZER (continued)

- Equalizer hold input
- Amplitude asymmetry factor output
- Internal AC-coupling

PULSE QUALIFICATION

- Sampled Viterbi qualification of signal equalized to EPR4
- Register programmable qualification thresholds for servo reads
- Selectable hysteresis or window qualification modes for servo reads
- Selectable dibit or pulse detect qualification modes for servo reads
- Programmable baseline offset for amplitude assymetry compensation

ERROR MEASUREMENT

- Digital channel quality monitor

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 212.5 MHz frequency output
- Independent M and N divide-by registers

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 16/17's GCR ENDEC
- Register programmable to 200 Mbit/s operation
- Fast acquisition, sampled data phase lock loop
- Decision directed clock recovery from sampled PR4 target
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- 8-bit NRZ data interface
- Data rate tracking, programmable write precompensation for non-linear transition shift
- Differential PECL write data output with power reduction
- Integrated sync byte detection, single byte or dual ("or" type)
- Programmable offset to compensate for MR head asymmetry
- Surface defect scan mode

SERVO

- 4-burst soft landing servo with A, B, C, D outputs
- Internal hold capacitors
- Separate, automatically selected, registers for servo Fc, boost, and threshold
- Wide bandwidth, precision full-wave rectifier with programmable offset to compensate for MR head asymmetry
- Servo calibration outputs
- Programmable baseline offset
- RDS and PPOL outputs for servo data recovery

THERMAL ASPERITY DETECTION/CORRECTION

- Analog front end thermal asperity detection and correction circuits
- Digital outputs for thermal asperity detection and error flag
- AGC and PLL hold over thermal asperity
- Programmable high admittance over thermal asperity

Prototype: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems reserves the right to make changes in specifications at any time without notice. Accordingly, the reader is cautioned to verify that the data sheet is current before placing orders.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914