Silicon Systems®
A Texas Instruments Company

SSI 36C3950
PCMCIA-ATA/IDE
Flash Drive Controller
Prototype

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DESCRIPTION

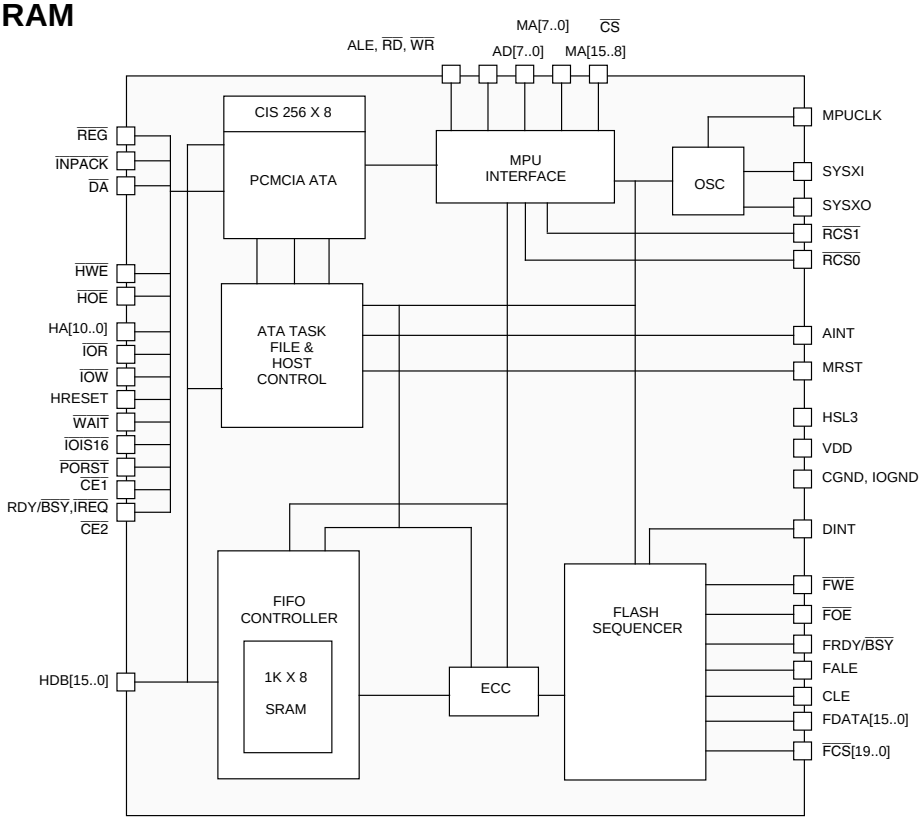
The SSI 36C3950 ATA FLASH Controller is a CMOS monolithic integrated circuit housed in a 144-lead TQFP package, and integrates the major portions of the hardware required to support up to 40 flash memory devices. Capabilites include compatibility with IDE-ATA interface, host transfer rates up to 16.6 MB/s, and Flash transfer rates up to 20 MB/s. The device utilizes only a small 64 K SRAM for Flash file management, and employs a BCH code for on-the-fly correction of up to 3 bits for each 256 bytes of data. Probability of uncorrectable error is 10^{-15} , and 10^{-20} for undetectable errors. The device supports operation in both 5 V and 3.3 V, and supports both Toshiba and Samsung NAND types of flash memory devices.

FEATURES

- **Supports Toshiba/Samsung NAND flash memory**
- **PCMCIA-ATA/IDE-ATA compatible host interface**
- **Bootable with IDE-ATA Interface**
- **Supports up to 40 flash memory devices**
- **Host transfer rates up to 16.6 MB/s**
- **Flash transfer rates up to 20 MB/s**
- **Data error correction able to correct up to 3 random bits for each 256 bytes of data**
- **Buffer transfer in PIO modes**

(continued)

BLOCK DIAGRAM



FEATURES (continued)

ATA HOST INTERFACE

- Host transfer rates up to 16.6 MB/s (ATA PIO Mode 4 timings)
- High current (12 mA at 5 V) drivers for direct connection to the bus
- Automatic BUSY, $\overline{\text{IREQ}}$, and DRQ protocol
- Supports multi-sector transfers without microprocessor intervention
- Automatic wake up from power-down on host reset or command write
- Programmable wait state insertion

FLASH CONTROLLER

- Advanced programmable sequencer
- Generates control signals, data, address bus, and chip select to flash devices
- Fast data transfer in both directions between Flash memory devices and FIFO controller
- Programmable retry counter
- Power down mode
- Supports 16 Mbit and 32 Mbit Samsung and Toshiba flash devices

FIFO CONTROLLER

- Controls two ping-pong sector buffer data RAM
- Buffer RAMs can handle 8 or 16-bit read/write independent from each other
- High speed data transfer between data FIFO, host, or flash sequencer

ERROR CORRECTION LOGIC

- Error correction up to 3 bits in each 256 bytes of data
- Data ECC probability of miscorrection better than 10^{-15} (assuming bit error rate of 10^{-5})
- Undetectable error rate better than 10^{-20}
- Automatic on-the-fly, in-buffer error correction
- Total hardware solution will take only 26 us to correct 3 errors

MICROPROCESSOR

- High speed register access
- Programmable wait state insertion
- Support multiplexed microprocessor (Intel 80C51/ 80C188)
- Supports wait stated or polled buffer data access
- Supports 64 kBytes of SRAM for flash management
- On-chip oscillator for generating buffer timing from 40 MHz crystal, or external clock
- Power-down mode

OTHER FEATURES

- Dual voltage (3.3 or 5 V) input receivers maintain TTL input levels based on the power supply value
- Standard TTL input and output levels maintained with 3 - 3.6, 4.5 - 5.5 V
- Input receivers may be dormant in sleep mode
- Available in 144-lead TQFP package