Silicon Systems®

A Texas Instruments Company

SSI 33P3733A

8-26.5 Mbit/s Read Channel w/Pit Mark Pulse Qualifier

February 1996

DESCRIPTION

The SSI 33P3733A device is a high performance BiCMOS single chip read channel IC that contains all the functions needed to implement a complete zoned recording read channel for magneto-optical (MO) drive systems. Functional blocks include the pulse detector, programmable filter, time base generator, and data synchronizer. MO data rates from 8 to 26.5 Mbit/s for (1,7) code, 6 to 20 Mbit/s for (2,7) code can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 33P3733A device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 33P3733A utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

FEATURES

- **Programmable MO data rate of 8 to 26.5 Mbit/s for (1,7) code, 6 to 20 Mbit/s for (2,7) code, internal DAC controlled**
- **Complete zoned recording application support**
- **Low-power operation (375 mW typical @ 5V)**
- **Bi-directional serial port for register access**
- **Register programmable power management (sleep mode <5 mW)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 64-lead TQFP package**

PULSE DETECTOR

- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low Drift AGC hold circuitry**
- **Temperature compensated, exponential control AGC**
- **Wide bandwidth, high precision full-wave rectifier**
- **Programmable LEVEL pin time constant with separate MO data and emboss registers**
- **Separate MO data and emboss AGC levels (4-bit DAC)**
- **Pulse qualification circuitry is provided for Pit Mark detection**
- **Internal fast decay timing**
- **External $\overline{\text{LOW\_Z}}$ control pin**
- **0.5 ns max. pulse pairing with sine wave input**

PROGRAMMABLE FILTER

- **Programmable cutoff frequency of 4 to 12 MHz**
- **Programmable boost/equalization of 0 to 13 dB**
- **Matched normal and differentiated outputs**
- **$\pm$ 15% *f*c accuracy**
- **$\pm$ 3% maximum group delay variation**
- **Less than 1.5% total harmonic distortion**
- **Low-Z input switch controlled by $\overline{\text{LOW\_Z}}$ pin**
- **No external filter components required**

TIME BASE GENERATOR

- **Better than 1% frequency resolution**
- **Up to 75 MHz frequency output**
- **Independent divide-by M and N registers**
- **VCO center frequency matched to data synchronizer VCO**
- **VCO (FOUT) output available independent of the mode**

DATA SEPARATOR

- **Fast acquisition phase lock loop with zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines, active devices, or active PLL components required**
- **Programmable decode window symmetry control via serial port**
  - **Window shift control $\pm$ 30% (4-bit)**
  - **Includes delayed read MO data and VCO clock monitor points**

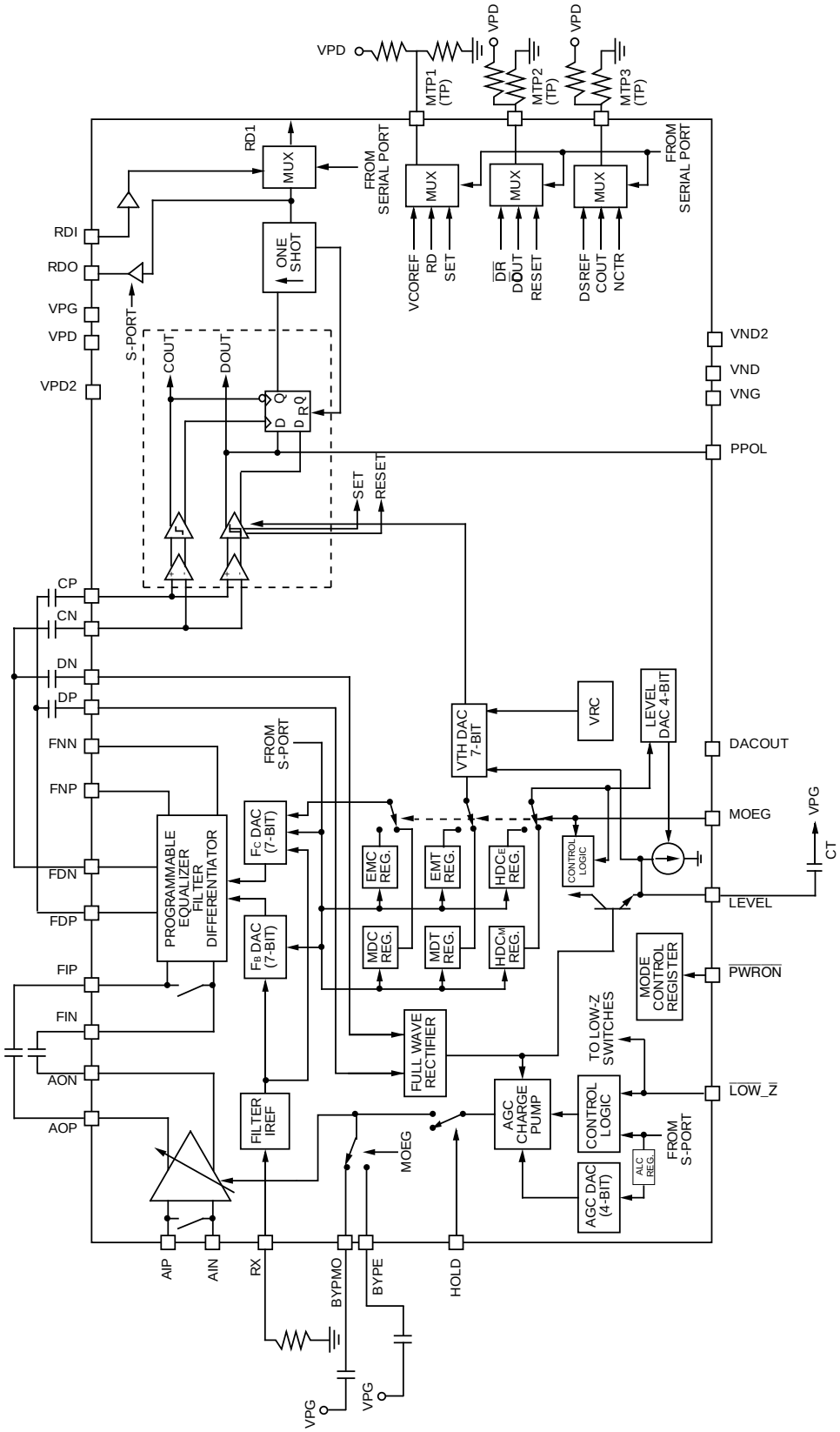

FIGURE 1A: Block Diagram, Front End

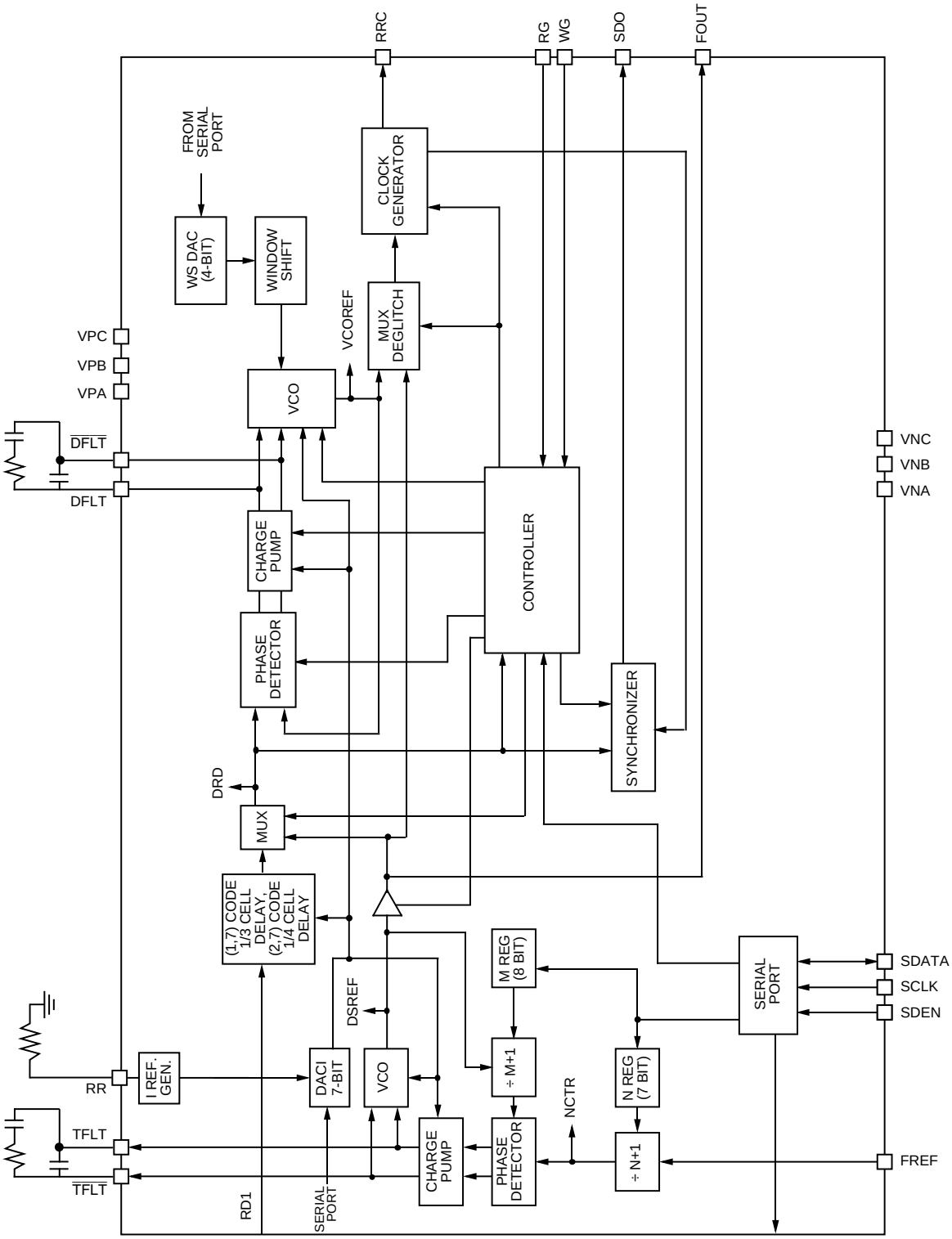

FIGURE 1B: Block Diagram, Back End