

August 1997

## DESCRIPTION

The SSI 33P3720A device is a high performance BiCMOS single chip analog front-end IC that contains the servo functions, RF attenuator, AGC and programmable equalizer/filter for a DVD drive system, and an auto laser power control circuit. Programmable functions of the SSI 33P3720A are controlled through a bi-directional serial port and banks of internal registers.

## FEATURES

### GENERAL

- Supports AGC and equalizer/filter up to DVD 3x speed and down to CD 1x speed
- Low power operation (350 mW typical @ 5 V)
- Bi-directional serial port register access
- Register programmed power management (sleep mode < 5 mW)
- Power supply range (4.5 to 5.5 V)
- Small footprint 64-Lead TQFP package

### SERVO

- 20 MHz bandwidth for the differential phase tracking error detection circuit (DPD)
- 130 kHz bandwidth for the focus, 80 kHz bandwidth for the DPP, 3 beam tracking error detection circuits
- Input programmable gain control amplifier (max: +20 dB, 3-bit resolution)
- Servo algebra signals used for optical alignment, seeking, focusing, and track following
- Pull-in signal output
- Mirror signal output
- Tracking error signal output
- 3 beam tracking error detection for CD
- 1 beam differential phase tracking error detection for DVD
- 3 beam differential push-pull tracking error detection for DVD-RAM
- Focusing error signal output
- Tilt servo control circuit

### CHANNEL

- 30 MHz bandwidth
- Programmable attenuator (min: -24 dB, 4-bit resolution)
- Fast attack/decay mode for rapid AGC recovery
- Low drift AGC hold circuitry
- Temperature compensated, exponential control AGC
- External AGC HOLD control pin
- Supports two ranges of programmable cutoff frequency: 4 to 16 MHz, 1 to 8 MHz
- Programmable boost/equalization of 0 to 12 dB
- Single-ended normal outputs for pulse qualification
- Differential normal signal outputs
- (20% Fc accuracy (Fc = 1 to 8 MHz)
- (15% Fc accuracy (Fc = 4 to 16 MHz)
- Less than 2% total harmonic distortion
- No external filter components required

### AUTO LASER POWER CONTROL

- Supports power mode selection

### FIGURE 1A: Block Diagram

The block diagram illustrates the architecture of a receiver system, showing the flow of signals from input to output and the control logic. Key components and their interconnections include:

- RF Inputs:** RFP and RFN are connected to the ATT (Automatic Tuning Tuner) block.
- Control Signals:** IDSEL, PWRON, and LOW\_Z are used to control various parts of the system, including the ATT and the AGC.
- AGC (Automatic Gain Control):** Multiple AGC blocks are used to control the gain of different stages, including the SUM Amp, DIFF Amp, and the final output stage.
- Filtering and Equalization:** The PROGRAMMABLE EQUALIZER FILTER and the FULL WAVE RECTIFIER are used to filter and rectify the received signals.
- Summing and Differencing:** The SUM Amp and DIFF Amp are used to sum and difference the signals from different channels.
- Gain Control:** Multiple GCA (Gain Control Amplifier) blocks are used to control the gain of different stages, including the SUM Amp, DIFF Amp, and the final output stage.
- Output and Control:** The system is controlled by various inputs like IDSEL, PWRON, and LOW\_Z. The output is connected to a DAC (Digital-to-Analog Converter) and a MUX (Multiplexer).

The diagram is watermarked with "SILICON" and "SILICON".

# SSI 33P3720A

## DVD Analog Front-End with DPD, DPP and 3 Beam Error Detection

FIGURE 1B: Block Diagram

