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## DESCRIPTION

The SSI 33P3720 device is a high performance BiCMOS single chip analog front-end IC that contains the servo functions, RF attenuator, AGC and programmable equalizer/filter for a DVD drive system, and an auto laser power control circuit. Programmable functions of the SSI 33P3720 are controlled through a bi-directional serial port and banks of internal registers.

## FEATURES

### GENERAL

- Supports AGC and equalizer/filter up to DVD 3x speed and down to CD 1x speed
- Low power operation (350 mW typical @ 5 V)
- Bi-directional serial port register access
- Register programmed power management (sleep mode < 5 mW)
- Power supply range (4.5 to 5.5 V)
- Small footprint 64-Lead TQFP package

### SERVO

- 20 MHz bandwidth for the differential phase tracking error detection circuit (DPD)
- 130 kHz bandwidth for the focus, 80 kHz bandwidth for the DPP, 3 beam tracking error detection circuits
- Input programmable gain control amplifier (max: +20 dB, 3-bit resolution)
- Servo algebra signals used for optical alignment, seeking, focusing, and track following
- Pull-in signal output
- Mirror signal output
- Tracking error signal output
- 3 beam tracking error detection for CD
- 1 beam differential phase tracking error detection for DVD
- 3 beam differential push-pull tracking error detection for DVD-RAM
- Focusing error signal output
- Tilt servo control circuit

### CHANNEL

- 30 MHz bandwidth
- Programmable attenuator (min: -24 dB, 4-bit resolution)
- Fast attack/decay mode for rapid AGC recovery
- Low drift AGC hold circuitry
- Temperature compensated, exponential control AGC
- External AGC HOLD control pin
- Supports two ranges of programmable cutoff frequency: 4 to 16 MHz, 1 to 8 MHz
- Programmable boost/equalization of 0 to 12 dB
- Single-ended normal outputs for pulse qualification
- Differential normal signal outputs
- (20% Fc accuracy (Fc = 1 to 8 MHz)
- (15% Fc accuracy (Fc = 4 to 16 MHz)
- Less than 2% total harmonic distortion
- No external filter components required

### AUTO LASER POWER CONTROL

- Supports power mode selection

### FIGURE 1A: Block Diagram

The block diagram illustrates the architecture of a receiver system, showing the flow of signals from input to output through various processing blocks. Key components and their interconnections include:

- RF Front-End:** Receives RF signals (RFP, RFN) and processes them through an ATT (Attenuator) and AGC (Automatic Gain Control) stages. It also includes a PROGRAMMABLE EQUALIZER FILTER and a FULL WAVE RECTIFIER.
- Baseband Processor:** Processes the baseband signals through a SUM Amp. and various GCA (Gain Control Amplifier) and LPF (Low Pass Filter) blocks. It includes a DAC (Digital-to-Analog Converter) and a GCA (Gain Control Amplifier) for offset adjustment.
- Video Processor:** Processes video signals through a DIFF. Amp. (Differential Amplifier) and various GCA and LPF blocks. It includes a DAC (Digital-to-Analog Converter) and a GCA (Gain Control Amplifier) for offset adjustment.
- Audio Processor:** Processes audio signals through a PHASE DETECTOR and various GCA and LPF blocks. It includes a DAC (Digital-to-Analog Converter) and a GCA (Gain Control Amplifier) for offset adjustment.
- Control and Monitoring:** Includes various control signals like IDSEL, PWRON, LOW\_Z, and monitoring signals like RX, FE, PI, HOLD2, BYP2, PP, TE, DVD-ROM.

The diagram is a detailed representation of the system's internal components and their interconnections, showing the flow of signals from input to output through various processing blocks.

# SSI 33P3720

## DVD Analog Front-End with DPD, DPP and 3 Beam Error Detection

FIGURE 1B: Block Diagram

