Silicon Systems®
A Texas Instruments Company

SSI 33P3705
E²PR4ML Read Channel with 1,7 ENDEC, Data Resync Capability

Prototype

February 1998

DESCRIPTION

The SSI 33P3705 is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire E²PR4 1,7 code read channel for zoned recording Magneto-Optical disk drive systems with data rates from 30 to 120 Mbit/s.

Functional blocks include AGC, programmable Filter/Pre-Differentiator, Maximum Likelihood (ML) Detector, 1,7 ENDEC, data synchronizer, time base generator, servo data detector, and data resync logic.

Programmable functions such as data rate, filter cutoff, filter boost, etc. are controlled by writing to the serial port registers so no external component changes are required to change zones. A programmable noise generator is included so that the channel can be optimized using BER testing.

1,7 RLL code operation is used to reduce the magnetic media flux transitions per inch and the write current rise time requirements. The SSI 33P3705 architecture can be extended for use at data rates up to 160 Mbit/s for future applications.

FEATURES

GENERAL

- **Register programmable data rates from 30 to 120 Mbit/s**
- **Sampled data read channel with Maximum Likelihood (ML) Detector**
- **Programmable filter with asymmetrical zeros to compensate pulse asymmetry**
- **PreDifferentiator in signal path accommodates standard Magneto-Optical interface**
- **1,7 RLL ENDEC**
- **Data Scrambler/Descrambler**
- **Low operating power (0.95 W typical at 5 V)**
- **Register programmable power management (<5 mW power down mode)**
- **8 bit NRZ data interface**
- **Serial interface port for access to internal program storage registers**
- **Single power supply (5 V ± 10%)**
- **Small footprint 100-lead TQFP package**

AUTOMATIC GAIN CONTROL

- **Dual mode AGC, continuous time during acquisition, sampled during data reads**
- **Separate AGC level storage pins for data and servo**
- **Dual rate attack and decay charge pump for rapid AGC recovery**
- **Programmable, symmetric, charge pump currents for data reads**
- **Charge pump currents track programmable data rate during data reads**
- **Low drift AGC hold circuitry**
- **Automatic AGC fast recovery and input low-z modes with programmable time durations**
- **Programmable input impedance provides for selectable attenuation in data and servo modes**
- **Wide bandwidth, precision full-wave rectifier**
- **Optional internal timing disable and AGC direct control pins: LOWZ, FASTREC, $\overline{\text{HOLD}}$**

FILTER / PREDIFFERENTIATOR

- **Programmable, 7-pole, continuous time filter with asymmetrical zeros provides:**
  - **Channel filter and pulse slimming equalization for equalization to E²PR4**
  - **Programmable cutoff frequency from 5 to 35 MHz**
  - **Programmable boost /equalization of 0 to 16 dB**
  - **Programmable asymmetrical zeros equalization to correct pulse shape asymmetry**
- **Second-order Differentiator embedded in the Filter provides:**
  - **Conversion of MO interface waveforms to Lorentzian-like signal for E²PR4 equalization**
  - **Constant gain as a function of data rate**
- **Internal AC-coupling with fast offset recovery at Filter outputs**

(continued)

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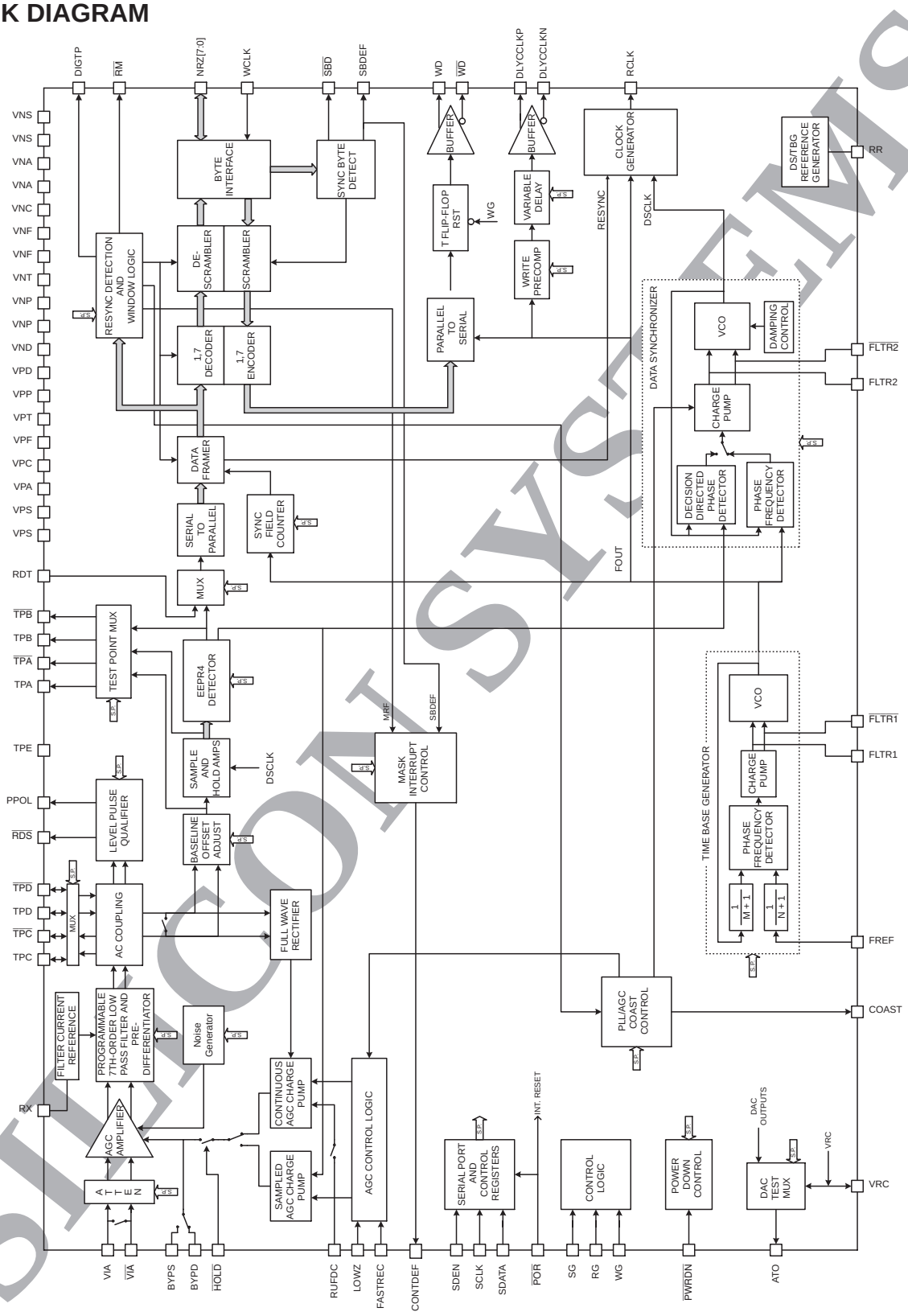
BLOCK DIAGRAM



FEATURES (continued)

PULSE QUALIFICATION

- Sampled Maximum Likelihood data detector with fixed E²PR4 target detection
- With white gaussian noise, within 0.5 dB of ideal Viterbi detector at user density of 2.0
- Register programmable qualification thresholds for servo reads
- Selectable hysteresis or window qualification modes for servo reads

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 180 MHz frequency output
- Independent M and N divide-by registers

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 1,7 RLL ENDEC
- Register programmable to 120 Mbit/s operation
- Fast acquisition, zero phase restart, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- 8-bit NRZ data interface
- Differential PECL programmable-delay code clock outputs for laser driver
- Programmable write precompensation of code clock for non-linear transition shift
- Differential PECL write data outputs with power reduction
- Programmable sync byte detection
- Programmable offset to compensate for head asymmetry

DATA RESYNC LOGIC

- Inserts one-byte resync pattern into every 15 bytes of user data in write mode
- Flags missing resyncs on readback for defect detection
- Defect location registers facilitate data recovery by Controller
- Defect recovery mode provided for loss of sync byte
- Programmable Controller Interrupt output for defect detection and recovery
- Programmable AGC / PLL coast mode to minimize defect-induced disturbances