Silicon Systems®
A Texas Instruments Company

SSI 33P3700
8-48 Mbit/s Magneto Optical Read Channel

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DESCRIPTION

The SSI 33P3700 device is a high performance BiCMOS single chip read channel IC that contains all the functions needed to implement a complete zoned recording read channel for magneto optical (MO) drive systems. Functional blocks include sum and difference amplifier, input attenuator, pulse detector, programmable filter, time base generator, and data synchronizer. MO data rates from 8 to 48 Mbit/s for (1,7) code, 6 to 36 Mbit/s for (2,7) code can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 33P3700 are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

FEATURES

- **Programmable MO/EMBOSS data rate of 8 to 48 Mbit/s for (1, 7RLL) code, 6 to 36 Mbit/s for (2, 7) code, internal DAC controlled**
- **Complete zoned recording application support**
- **Low-power operation (500 mW typical @ 5V)**
- **Bi-directional serial port register access**
- **Register programmable power management (sleep mode <5 mW)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 64-Lead TQFP package**

PULSE DETECTOR

- **Provides the head amplifiers difference for MO and sum for emboss signals**
- **Dual programmable attenuator (min-24 dB, 4-bit resolution) for MO and emboss data with Lo2w-Z switch and internal multiplexer**
- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low Drift AGC hold circuitry**
- **Temperature compensated, exponential control AGC**
- **Wide bandwidth, high precision full-wave rectifier**
- **Programmable LEVEL pin time constant with separate MO and emboss**
- **Separate MO and emboss AGC levels (4-bit DAC)**
- **Optimized pulse qualification circuitry for pit mark recording with input clip circuit**
- **Internal fast decay timing**
- **External $\overline{\text{LOW\_Z}}$ control pin**

PROGRAMMABLE FILTER

- **Programmable cutoff frequency of 4 to 24 MHz**
- **Programmable boost/equalization of 0 to 12 dB**
- **Matched normal and differentiated outputs**
- **$\pm$ 20% fc accuracy (fc = 4 to 8 MHz)**
  $\pm$ 15% fc accuracy (fc = 8 to 24 MHz)
- **$\pm$ 4% maximum group delay variation**
- **Less than 1.5% total harmonic distortion**
- **Low-Z input switch is controlled by $\overline{\text{LOW\_Z}}$ pin**
- **No external filter components required**

TIME BASE GENERATOR

- **Better than 1% frequency resolution**
- **Up to 75 MHz frequency output**
- **Independent divide-by M and N registers**
- **VCO center frequency matched to data synchronizer VCO**
- **VCO (FOUT) output available except during power down mode**

DATA SYNCHRONIZER

- **Fast acquisition phase lock loop with zero phase restart technique**
- **Fully integrated data synchronizer**
  - **No external delay lines, active devices, or active PLL components**
- **Programmable decode window symmetry control via serial port**
  - **Window shift control $\pm$ 30% (4-bit)**
  - **Includes delayed read MO/emboss data and VCO clock monitor points**
- **Separate Qualifier output (RDO) and data separator input (RDI)**

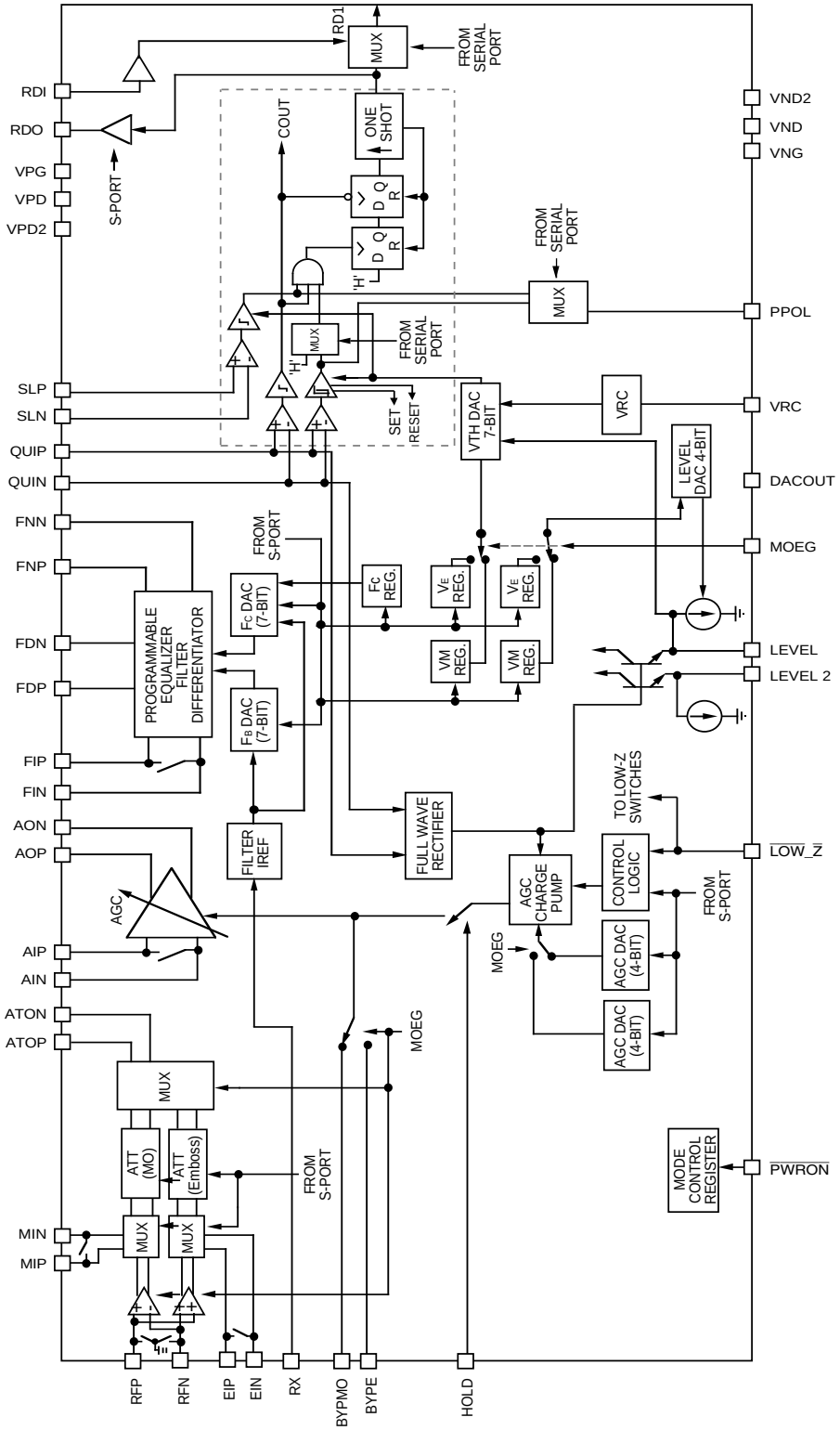

FIGURE 1A : Block Diagram - Front End

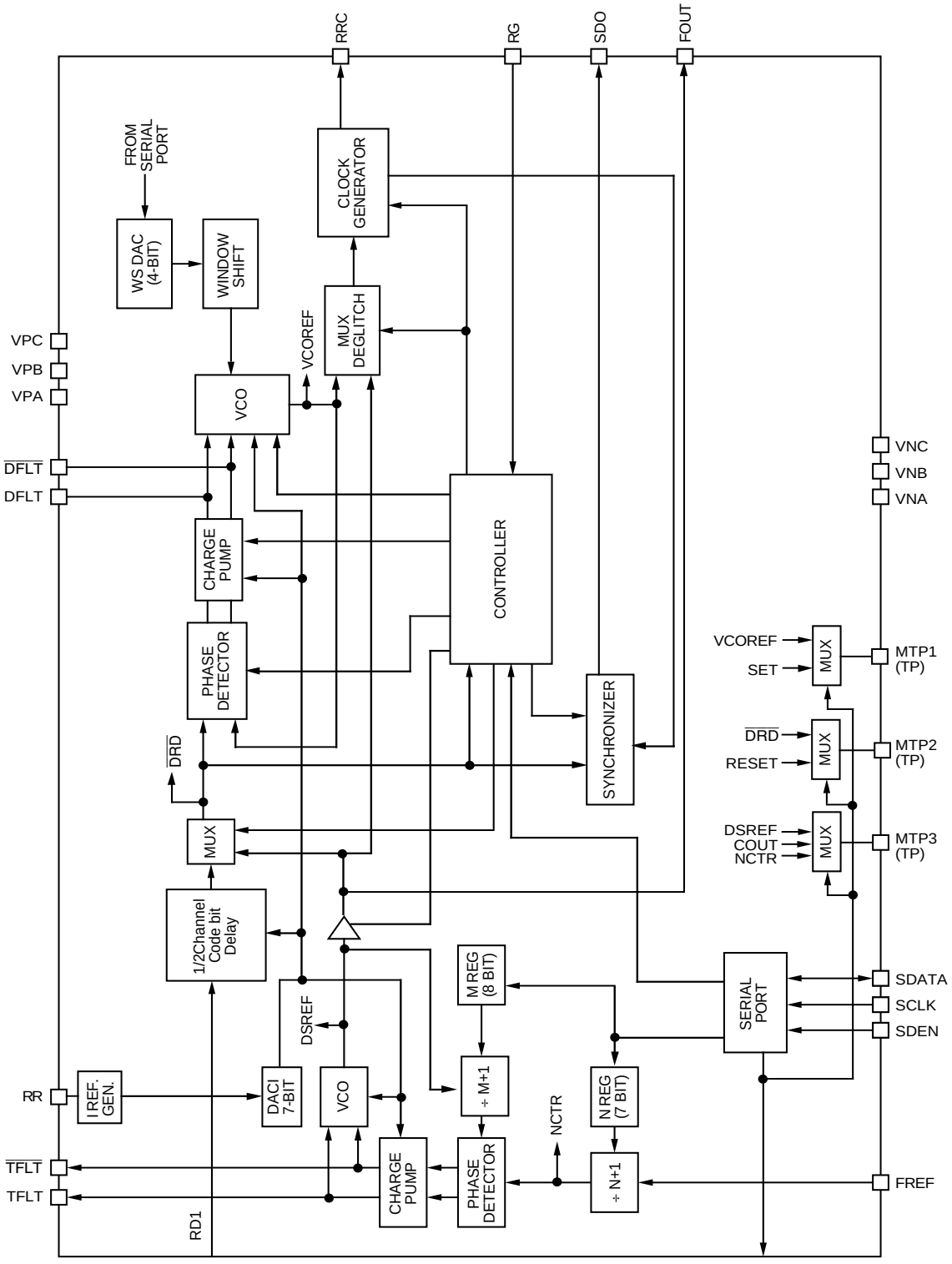

FIGURE 1B : Block Diagram -Back End